AS3930

Single Channel Low Frequency Wakeup Receiver

1 General Description

The AS3930 is a single-channel low power ASK receiver that is able to generate a wakeup upon detection of a data signal which uses a LF carrier frequency between 110 - 150 kHz. The integrated correlator can be used for detection of a programmable 16-bit wakeup pattern.

The AS3930 provides a digital RSSI value, it supports a programmable data rate and Manchester decoding with clock recovery. The AS3930 offers a real-time clock (RTC), which is either derived from a crystal oscillator or the internal RC oscillator.

The programmable features of AS3930 enable to optimize its settings for achieving a longer distance while retaining a reliable wakeup generation. The sensitivity level of AS3930 can be adjusted in presence of a strong field or in noisy environments.

The device is available in 16 pin TSSOP and QFN 4x4 16 LD packages.

2 Key Features

- Single channel ASK wakeup receiver
- Carrier frequency range 110 - 150 kHz
- Programmable wakeup pattern (16bits)
- Doubling of wakeup pattern supported
- Wakeup without pattern detection supported
- Wakeup sensitivity 100µVRMS (typ.)
- Adjustable sensitivity level
- Highly resistant to false wakeups
- False wakeup counter
- Periodical forced wakeup supported (1s – 2h)
- Low power listening modes
- Current consumption in listening mode 1.37 µA (typ.)
- Data rate adjustable from 0.5 - 4 kbps (Manchester)
- Manchester decoding with clock recovery
- Digital RSSI
- Dynamic range 64dB
- 5 bit RSSI step (2dB per step)
- RTC based on 32kHz XTAL, RC-OSC, or external clock
- Operating temperature range -40 to +85ºC
- Operating supply voltage 2.4 - 3.6V (TA = 25ºC)
- Bidirectional serial digital interface (SDI)
- Package option 16 pin TSSOP, QFN 4x4 16 LD

3 Applications

The AS3930 is ideal for Active RFID tags, real-time location systems, operator identification, access control, and wireless sensors.

Figure 1. AS3930 Typical Application Diagram with Crystal Oscillator

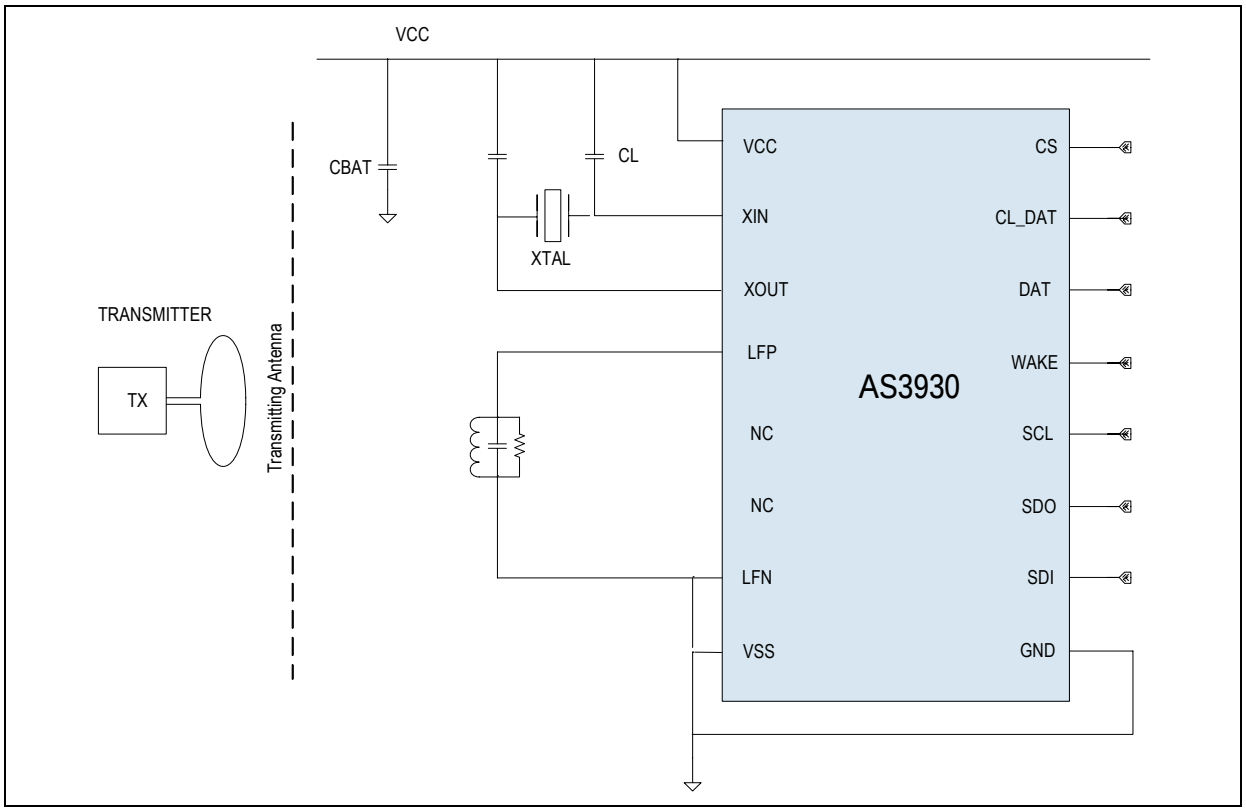


Figure 2. AS3930 Typical Application Diagram without Crystal Oscillator

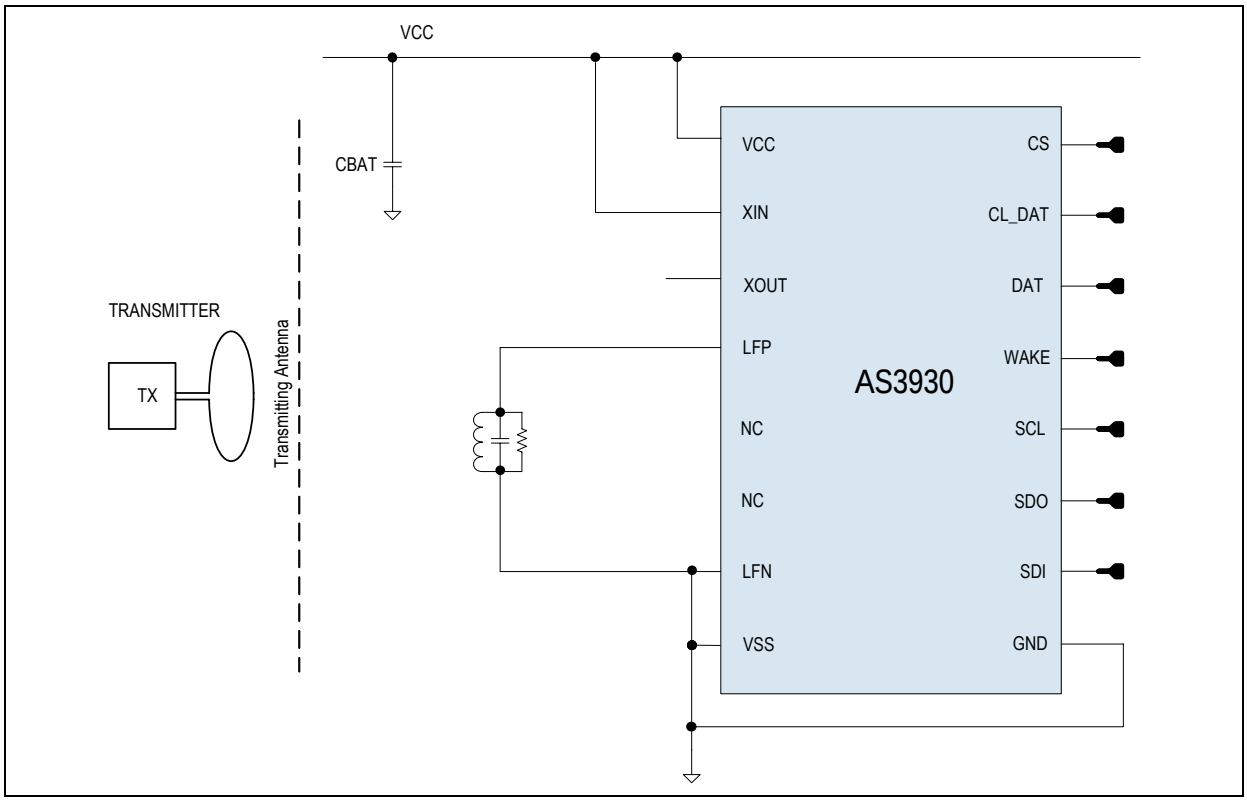
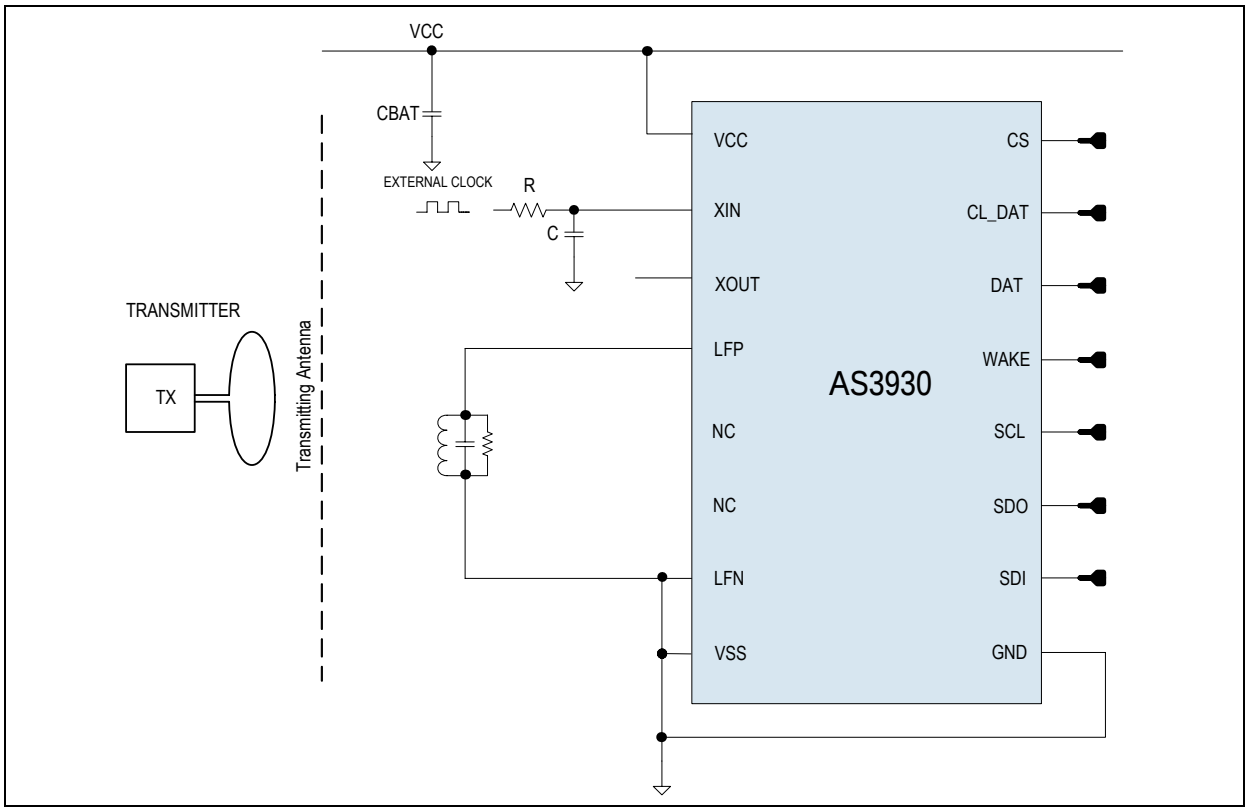


Figure 3. AS3930 Typical Application Diagram with Clock from External Source

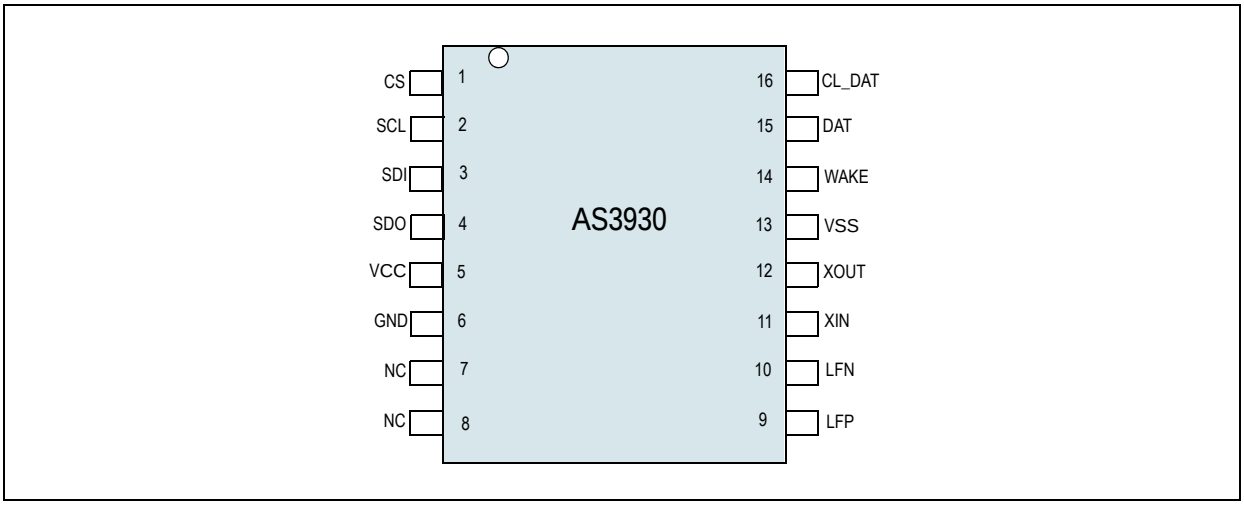


Contents

4 Pin Assignments

4.1 TSSOP Package

Figure 4. Pin Assignments 16 pin TSSOP Package



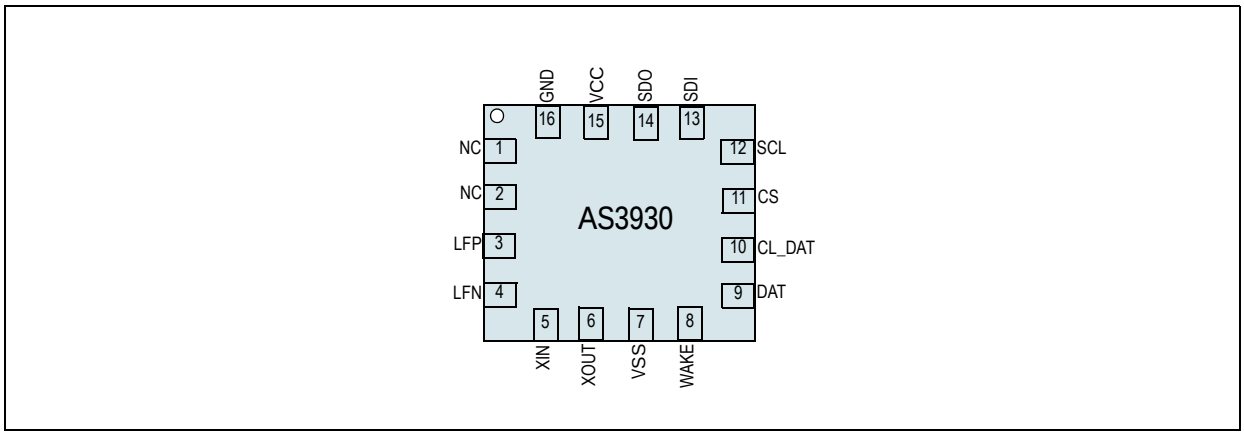
4.1.1 Pin Descriptions

Table 1. Pin Descriptions 16 pin TSSOP Package

Pin Name	Pin Number	Pin Type	Description
CS	1	DI	Chip select
SCL	2	DI	SDI interface clock
SDI	3	DI	SDI data input
SDO	4	DO_T	SDI data output (tristate when CS is low)
Vcc	5	S	Positive supply voltage
GND	6	S	Negative supply voltage
NC	7	Not Connected	
NC	8	Not Connected	
LFP	9	AIO	Input antenna
LFN	10	AIO	Antenna ground
XIN	11	AIO	Crystal oscillator input
XOUT	12	AIO	Crystal oscillator output
Vss	13	S	Substrate
WAKE	14	DO	Wakeup output IRQ
DAT	15	DO	Data output
CL_DAT	16	DO	Manchester recovered clock

4.2 QFN Package

Figure 5. Pin Assignments QFN 4x4 16 LD Package



4.2.1 Pin Descriptions

Table 2. Pin Descriptions QFN 4x4 16 LD Package

Pin Name	Pin Number	Pin Type	Description
NC	1		Not connected
NC	2		Not connected
LFP	3	AIO	Input antenna
LFN	4	AIO	Antenna ground
XIN	5	AIO	Crystal oscillator input
XOUT	6	AIO	Crystal oscillator output
Vss	7	S	Substrate
WAKE	8	DO	Wakeup output IRQ
DAT	9	DO	Data output
CL_DAT	10	DO	Manchester recovered clock
CS	11	DI	Chip select
SCL	12	DI	SDI interface clock
SDI	13	DI	SDI data input
SDO	14	DO_T	SDI data output (tristate when CS is low)
Vcc	15	S	Positive supply voltage
GND	16	S	Negative supply voltage

Note: PIN Types:

S: supply pad
AIO: analog I/O
DI: digital input
DO: digital output
DO_T: digital output / tristate

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 8 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
DC supply voltage (V_{DD})	-0.5	5	V	
Input pin voltage (V_{IN})	-0.5	5	V	
Input current (latch up immunity) (I_{SOURCE})	-100	100	mA	Norm: Jedec 78
Electrostatic discharge (ESD)	±2		kV	Norm: MIL 883 E method 3015 (HBM)
Total power dissipation (all supplies and outputs) (P_t)		0.07	mW	
Storage temperature (T_{strg})	-65	150	ºC	
Package body temperature (T_{body})		260	ºC	Norm: IPC/JEDEC J-STD-020C[1]
Humidity non-condensing	5	85	%	

1. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices”.

6 Electrical Characteristics

Table 4. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Operating Conditions						
AV_{DD}	Positive supply voltage		2.4		3.6	V
AV_{SS}	Negative supply voltage		0		0	V
T_{AMB}	Ambient temperature		-40		85	°C
DC/AC Characteristics for Digital Inputs and Outputs						
CMOS Input						
V_{IH}	High level input voltage		0.58 * V_{DD}	0.7 * V_{DD}	0.83 * V_{DD}	V
V_{IL}	Low level input voltage		0.125 * V_{DD}	0.2 * V_{DD}	0.3 * DVDD	V
I_{LEAK}	Input leakage current				100	nA
CMOS Output						
V_{OH}	High level output voltage	With a load current of 1mA	V_{DD} - 0.4			V
V_{OL}	Low level output voltage	With a load current of 1mA			V_{SS} + 0.4	V
C_L	Capacitive load	For a clock frequency of 1 MHz			400	pF
Tristate CMOS Output						
V_{OH}	High level output voltage	With a load current of 1mA	V_{DD} - 0.4			V
V_{OL}	Low level output voltage	With a load current of 1mA			V_{SS} + 0.4	V
I_{OZ}	Tristate leakage current	to DVDD and DVSS			100	nA

Table 5. Electrical System Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Input Characteristics						
Rin	Input Impedance	In case no antenna damper is set (R1<4>=0)		2		M Ω
Fmin	Minimum Input Frequency			110		kHz
Fmax	Maximum Input Frequency			150		kHz
Current Consumption						
IPWD	Power Down Mode			400	800	nA
ICHRC	Current Consumption in standard listening mode with channel active all the time and RC-oscillator as RTC			2.7		µA
ICHOORC	Current Consumption in ON/ OFF mode and RC-oscillator as RTC	11% Duty Cycle		1.37		µA
		50% Duty Cycle		2		
ICHXT	Current Consumption in standard listening mode and crystal oscillator as RTC			3.5	5.9	µA

Table 5. Electrical System Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IDATA	Current Consumption in Preamble detection / Pattern correlation / Data receiving mode (RC-oscillator)	With 125 kHz carrier frequency and 1 kbps data-rate. No load on the output pins.		5.3	9	µA
Input Sensitivity						
SENS	Input Sensitivity on all channels	With 125kHz carrier frequency, chip in default mode, 4 half bits burst + 4 symbols preamble and single preamble detection		100		µVrms
Channel Settling Time						
TSAMP	Amplifier settling time			250		µs
Crystal Oscillator						
FXTAL	Frequency	Crystal dependent		32.768		kHz
TXTAL	Start-up Time	Crystal dependent			1	s
IXTAL	Current consumption			1		µA
External Clock Source						
IEXTCL	Current consumption			1		µA
RC Oscillator						
FRCNCAL	Frequency	If no calibration is performed	27	32.768	42	kHz
FRCCAL32	Frequency	If calibration with 32.768 kHz reference signal is performed	31	32.768	34.5	kHz
FRCCALMAX	Frequency	Maximum achievable frequency after calibration		35		kHz
FRCCALMIN	Frequency	Minimum achievable frequency after calibration		30		kHz
TCALRC	Calibration time				65	Periods of reference clock
IRC	Current consumption			200		nA

7 Typical Operating Characteristics

Figure 6. Sensitivity over Voltage and Temperature

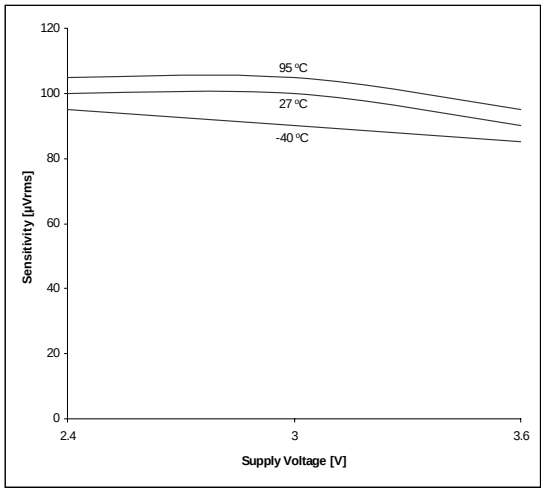


Figure 7. Sensitivity over RSSI

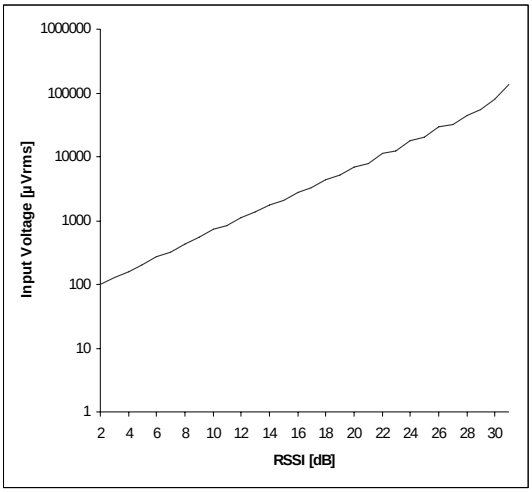


Figure 8. RC-Osc Frequency over Voltage (calibr.)

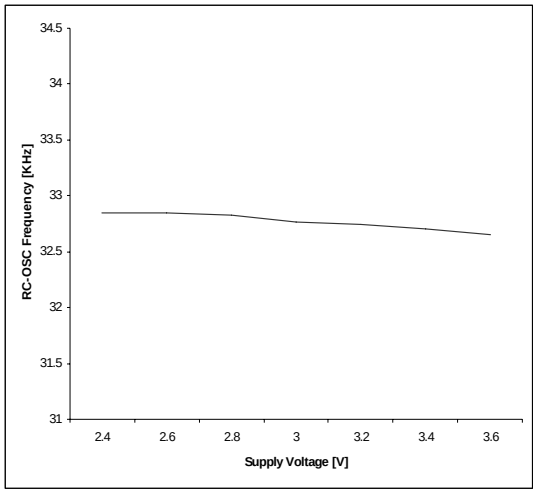
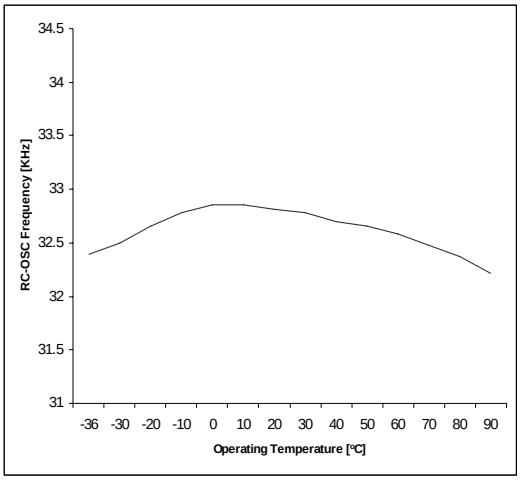


Figure 9. RC-Osc Frequency over Temperature (calibr.)



8 Detailed Description

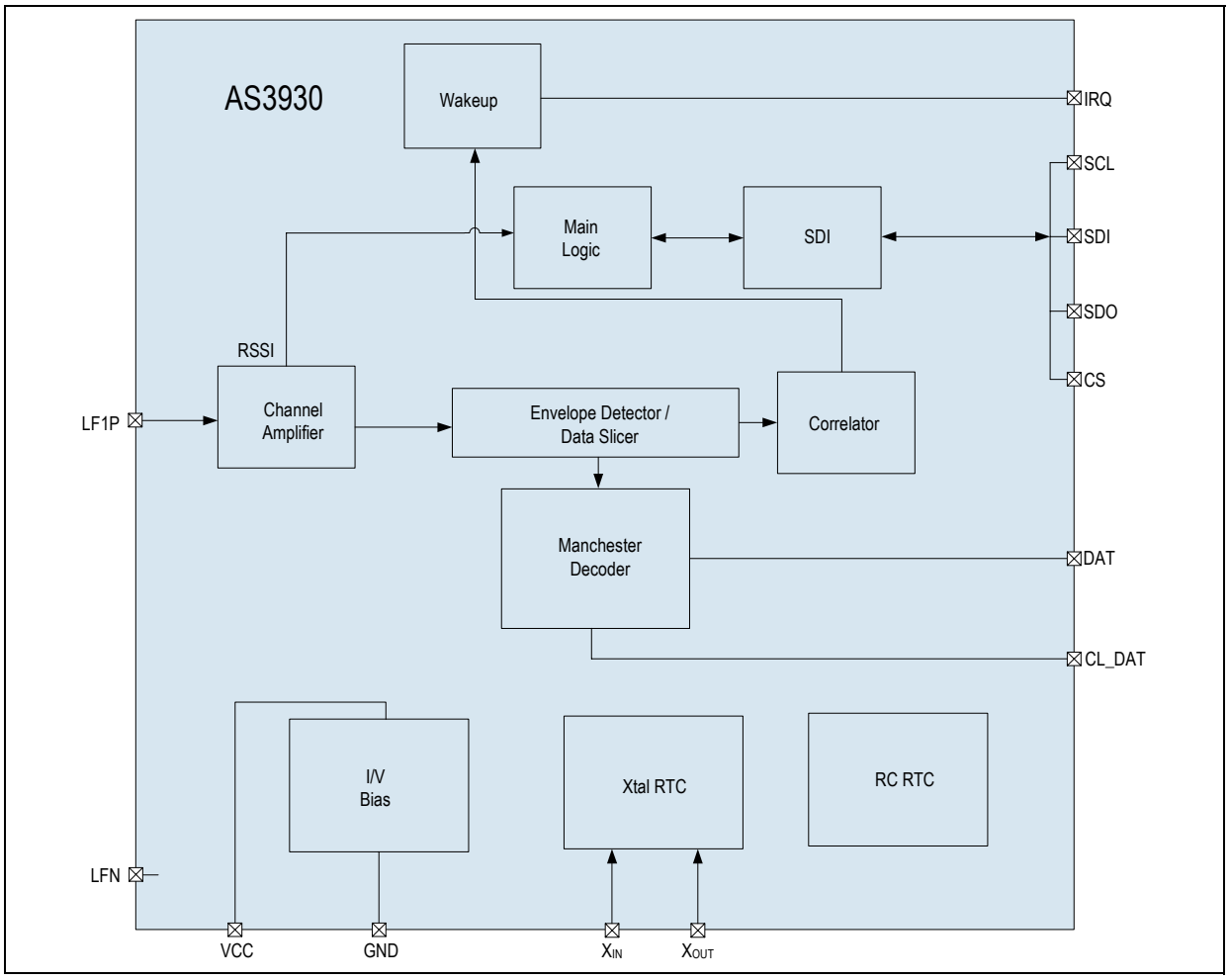
The AS3930 is a one-dimensional low power low-frequency wakeup receiver. The AS3930 is capable to detect the presence of an inductive coupled carrier and extract the envelope of the On-Off-Keying (OOK) modulated carrier. In case the carrier is Manchester coded the clock is recovered from the transmitted signal and the data can be correlated with a programmed pattern. If the detected pattern corresponds to the stored one, a wake-up signal (IRQ) is risen up. The pattern correlation can be bypassed in case and the wake-up detection is based only on the frequency detection.

The AS3930 is made up of a single receiving channel, one envelop detector, one data correlator, one Manchester decoder, 8 programmable registers with the main logic and a real time clock.

The digital logic can be accessed by an SDI. The real time clock can be based on a crystal oscillator or on an internal RC. In case internal RC is used to improve its accuracy a calibration can be performed.

8.1 Block Diagram

Figure 10. Block Diagram



AS3930 needs the following external components:

- Power supply capacitor - CBAT – 100 nF
- 32.768 kHz crystal with its two pulling capacitors – XTAL and CL (it is possible to omit these components if the internal RC oscillator is used instead of the crystal oscillator).
- Input LC resonator.

In case the internal RC-oscillator is used (no crystal oscillator is mounted), the pin XIN has to be connected to the supply, while pin XOUT should stay floating. Application diagrams with and without crystal are shown in Figure 1 and Figure 2

8.2 Operating modes

8.2.1 Power Down Mode

In Power Down Mode AS3930 is completely switched off. The typical current consumption is 400 nA.

8.2.2 Listening Mode

In listening mode only the channel amplifier and the RTC are running. In this mode the system detects the presence of a carrier. In case the carrier is detected the RSSI can be displayed.

Inside this mode it is possible to distinguish the following three sub modes:

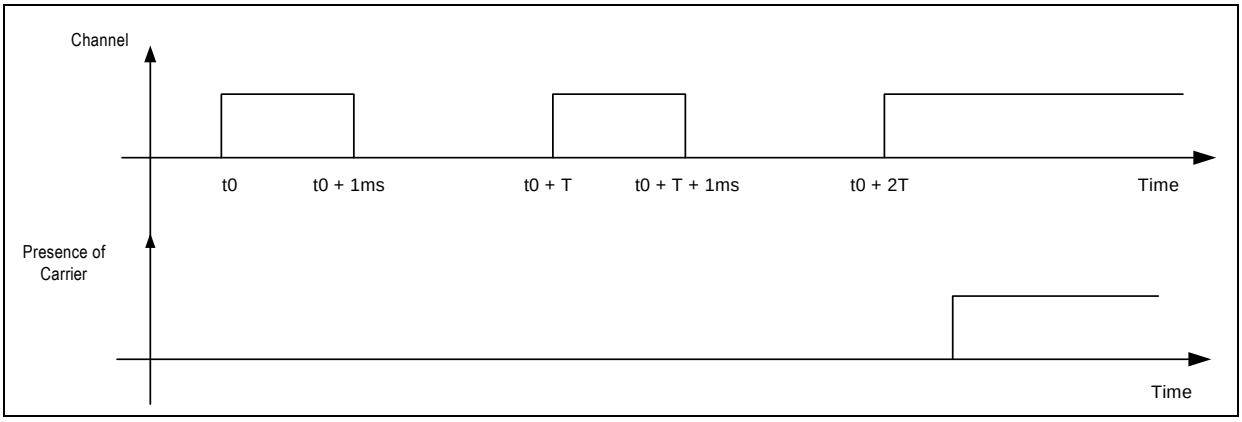
8.2.2.1 Standard Listening mode

The channel amplifier, capable to detect the presence of the carrier frequency, is active all the time.

8.2.2.2 ON/OFF mode (Low Power mode)

The channel amplifier is active for one millisecond to be than switched-off for a certain time. The OFF-time is programmable see **R4<7:6>**.

Figure 11. ON/OFF Mode



For both sub modes it is possible to enable a further feature called Artificial Wake-up. If the Artificial Wakeup is enabled the AS3930 produces an interrupt after a certain time regardless whether any activity is detected on the input. The period of the Artificial Wake-up is defined in the register R8<2:0>. The user can distinguish between Artificial Wake-up and Wake-up based on the field detection (frequency or pattern detection) since the Artificial Wake-up interrupt lasts only 128 µs. With this interrupt the microcontroller (µC) can get feedback on the surrounding environment (e.g. read the false wakeup register, see relator register R13<7:0>) and/or take actions in order to change the setup.

8.2.3 Preamble Detection / Pattern Correlation

The chip can go in to this mode after detecting a LF carrier only if the data correlator function is enabled see **R1<1>**. The correlator searches first for preamble frequency (constant frequency of Manchester clock defined according to bit-rate transmission) and then for data pattern.

If the pattern is matched the wake-up interrupt is displayed on the WAKE output and the chip goes in data receiving mode. If the pattern fails the internal wake-up is terminated and no IRQ is produced.

8.2.4 Data Receiving

The user can enable this mode allowing the pattern correlation or just on the base of the frequency detection. In this mode the chip can be retained as a normal OOK receiver. The data is provided on the DAT pin and in case the Manchester decoder is enabled see **R1<3>**, the recovered clock is present on the CL_DAT. It is possible to put the chip back to listening mode either with a direct command (CLEAR_WAKE (see Table 12)) or by using the timeout feature. This feature automatically sets the chip back to listening mode after a certain time defined in the **R7<7:5>**.

8.3 System and Block Specification

8.3.1 Main Logic and SDI

8.3.1.1 Register Table

Table 6. Register Table

	7	6	5	4	3	2	1	0
R0	n.a.		ON_OFF	Reserved			EN_A	PWD
R1	ABS_HY	AGC_TLIM	AGC_UD	ATT_ON	EN_MANCH	EN_PAT2	EN_WPAT	EN_RTC
R2	S_ABSH	W_PAT_T<1:0>		Reserved			S_WU1<1:0>	
R3	HY_20m	HY_POS	FS_SLC<2:0>			FS_ENV<2:0>		
R4	T_OFF<1:0>		R_VAL<1:0>		GR<3:0>			
R5	TS2<7:0>							
R6	TS1<7:0>							
R7	T_OUT<2:0>			T_HBIT<4:0>				
R8	n.a.					T_AUTO<2:0>		
R9	n.a.	Reserved						
R10	n.a.			RSSI1<4:0>				
R11	n.a.			RSSI3<4:0>				
R12	n.a.			RSSI2<4:0>				
R13	F_WAKE							

8.3.1.2 Register Table Description and Default Values

Table 7. Default Values of Registers

Register	Name	Type	Default Value	Description
R0<5>	ON_OFF	W	0	On/Off operation mode. (Duty-cycle defined in the register R4<7:6>)
R0<4>	MUX_123	W	0	Reserved (it is not allowed to set this bit to 1)
R0<3>	Reserved	W	1	Reserved
R0<2>	Reserved	W	1	Reserved
R0<1>	EN_A	W	1	Channel enable
R0<0>	PWD	W	0	Power down
R1<7>	ABS_HY	W	0	Data slicer absolute reference
R1<6>	AGC_TLIM	W	0	AGC acting only on the first carrier burst
R1<5>	AGC_UD	W	1	AGC operating in both direction (up-down)
R1<4>	ATT_ON	W	0	Antenna damper enable
R1<3>	EN_MANCH	W	0	Manchester decoder enable

Table 7. Default Values of Registers

Register	Name	Type	Default Value	Description	
R1<2>	EN_PAT2	W	0	Double wakeup pattern correlation	
R1<1>	EN_WPAT	W	1	Data correlation enable	
R1<0>	EN_RTC	W	1	Crystal oscillator enable	
R2<7>	S_ABSH	W	0	Data slicer threshold reduction	
R2<6:5>	W_PAT	W	00	Pattern correlation tolerance (see Table 19)	
R2<4:2>			000	Reserved	
R2<1:0>	S_WU1	W	00	Tolerance setting for the stage wakeup (see Table 13)	
R3<7>	HY_20m	W	0	Data slicer hysteresis if HY_20m = 0 then comparator hysteresis = 40mV if HY_20m = 1 then comparator hysteresis = 20mV	
R3<6>	HY_POS	W	0	Data slicer hysteresis only on positive edges (HY_POS=0, hysteresis on both edges, HY_POS=1, hysteresis only on positive edges)	
R3<5:3>	FS_SCL	W	100	Data slices time constant (see Table 17)	
R3<2:0>	FS_ENV	W	000	Envelop detector time constant (see Table 16)	
R4<7:6>	T_OFF	W	00	Off time in ON/OFF operation mode	
				T_OFF=00	1ms
				T_OFF=01	2ms
				T_OFF=10	4ms
				T_OFF=11	8ms
R4<5:4>	D_RES	W	01	Antenna damping resistor (see Table 15)	
R4<3:0>	GR	W	0000	Gain reduction (see Table 14)	
R5<7:0>	TS2	W	01101001	2nd Byte of wakeup pattern	
R6<7:0>	TS1	W	10010110	1st Byte of wakeup pattern	
R7<7:5>	T_OUT	W	000	Automatic time-out (see Table 20)	
R7<4:0>	T_HBIT	W	01011	Bit rate definition (see Table 18)	
R8<2:0>	T_AUTO	W	000	Artificial wake-up	
				T_AUTO=000	No artificial wake-up
				T_AUTO=001	1 sec
				T_AUTO=010	5 sec
				T_AUTO=011	20 sec
				T_AUTO=100	2 min
				T_AUTO=101	15min
				T_AUTO=110	1 hour
				T_AUTO=111	2 hour
R9<6:0>			000000	Reserved	
R10<4:0>	RSSI	R		RSSI channel	
R11<4:0>				Reserved	

Table 7. Default Values of Registers

Register	Name	Type	Default Value	Description
R12<4:0>				Reserved
R13<7:0>	F_WAK	WR		False wakeup register

8.3.1.3 Serial Data Interface (SDI)

This 4-wire interface is used by the Microcontroller (µC) to program the AS3930. The maximum clock operation frequency of the SDI is 2 MHz.

Table 8. Serial Data Interface (SDI) pins

Name	Signal	Signal Level	Description
CS	Digital Input with pull down	CMOS	Chip Select
SDI	Digital Input with pull down	CMOS	Serial Data input for writing registers, data to transmit and/or writing addresses to select readable register
SDO	Digital Output	CMOS	Serial Data output for received data or read value of selected registers
SCLK	Digital Input with pull down	CMOS	Clock for serial data read and write

Note: SDO is set to tristate if CS is low. In this way more than one device can communicate on the same SDO bus.

SDI Command Structure

To program the SDI the CS signal has to go high. A SDI command is made up by a two bytes serial command and the data is sampled on the falling edge of SCLK. The Table 9 shows how the command looks like, from the MSB (B15) to LSB (B0). The command stream has to be sent to the SDI from the MSB (B15) to the LSB (B0).

Table 9. SDI Command Structure

Mode		Register address / Direct Command						Register Data							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

The first two bits (B15 and B14) define the operating mode. There are three modes available (write, read, direct command) plus one spare (not used), as shown in Table 10.

Table 10. SDI Command Structure

B15	B14	Mode
0	0	WRITE
0	1	READ
1	0	NOT ALLOWED
1	1	DIRECT COMMAND

In case a write or read command happens the next 5 bits (B13 to B9) define the register address which has to be written respectively read, as shown in Table 11.

Table 11. SDI Command Structure

B13	B12	B11	B10	B9	B8	Read/Write register
0	0	0	0	0	0	R0
0	0	0	0	0	1	R1
0	0	0	0	1	0	R2
0	0	0	0	1	1	R3

Table 11. SDI Command Structure

B13	B12	B11	B10	B9	B8	Read/Write register
0	0	0	1	0	0	R4
0	0	0	1	0	1	R5
0	0	0	1	1	0	R6
0	0	0	1	1	1	R7
0	0	1	0	0	0	R8
0	0	1	0	0	1	R9
0	0	1	0	1	0	R10
0	0	1	0	1	1	R11
0	0	1	1	0	0	R12
0	0	1	1	0	1	R13

The last 8 bits are the data that has to be written respectively read. A CS toggle high-low-high terminates the command mode.

If a direct command is sent (B15-B14=11) the bits from B13 to B9 defines the direct command while the last 8 bits are omitted. The Table 12 shows all possible direct commands:

Table 12. List of Direct Commands

COMMAND_MODE	B13	B12	B11	B10	B9	B8
clear_wake	0	0	0	0	0	0
reset_RSSI	0	0	0	0	0	1
trim_osc	0	0	0	0	1	0
clear_false	0	0	0	0	1	1
preset_default	0	0	0	1	0	0

All direct commands are explained below:

- clear_wake: clears the wake state of the chip. In case the chip has woken up (WAKE pin is high) the chip is set back to listening mode
- reset_RSSI: resets the RSSI measurement.
- trim_osc: starts the trimming procedure of the internal RC oscillator (see Figure 21)
- clear_false: resets the false wakeup register (R13=00)
- preset_default: sets all register in the default mode, as shown in Figure 7

Note: In order to get the AS3930 work properly after sending the preset_default direct command, it is mandatory to write the R0<3:2>=00

Writing of Data to Addressable Registers (WRITE Mode)

The SDI is sampled at the falling edge of CLK (as shown in the following diagrams).

A CS toggling high-low-high indicates the end of the WRITE command after register has been written. The following example shows a write command.

Figure 12. Writing of a single Byte (falling edge sampling)

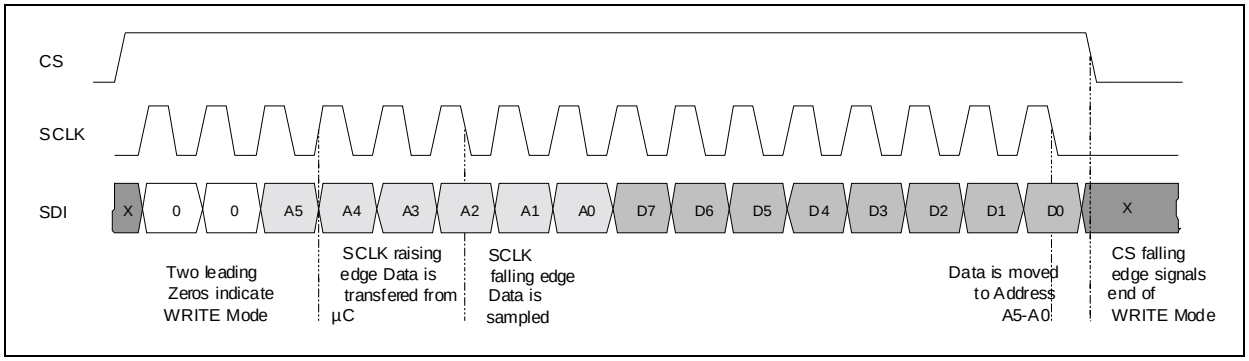
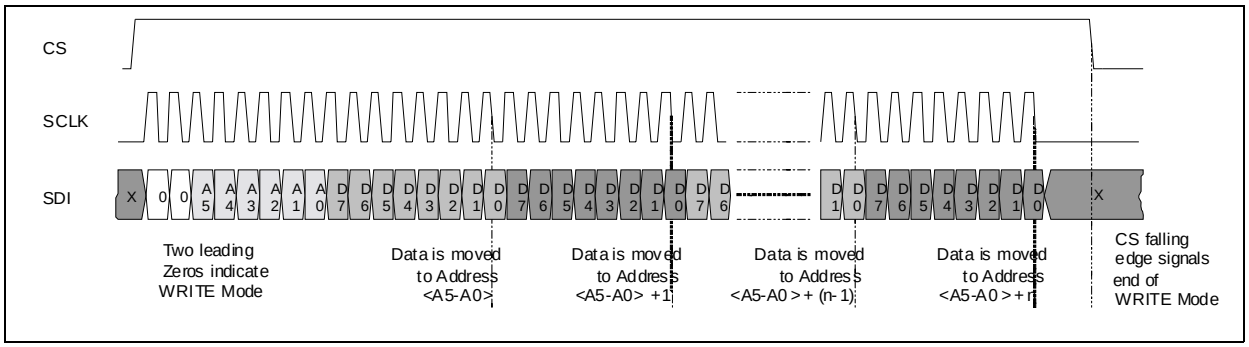


Figure 13. Writing of Register Data with auto-incrementing Address



Reading of Data from Addressable Registers (READ Mode)

Once the address has been sent through SDI, the data can be fed through the SDO pin out to the microcontroller.

A CS LOW toggling high-low-high has to be performed after finishing the read mode session, in order to indicate the end of the READ command and prepare the Interface to the next command control Byte.

To transfer bytes from consecutive addresses, SDI master has to keep the CS signal high and the SCLK clock has to be active as long as data need to be read.

Figure 14. Reading of a single Register Byte

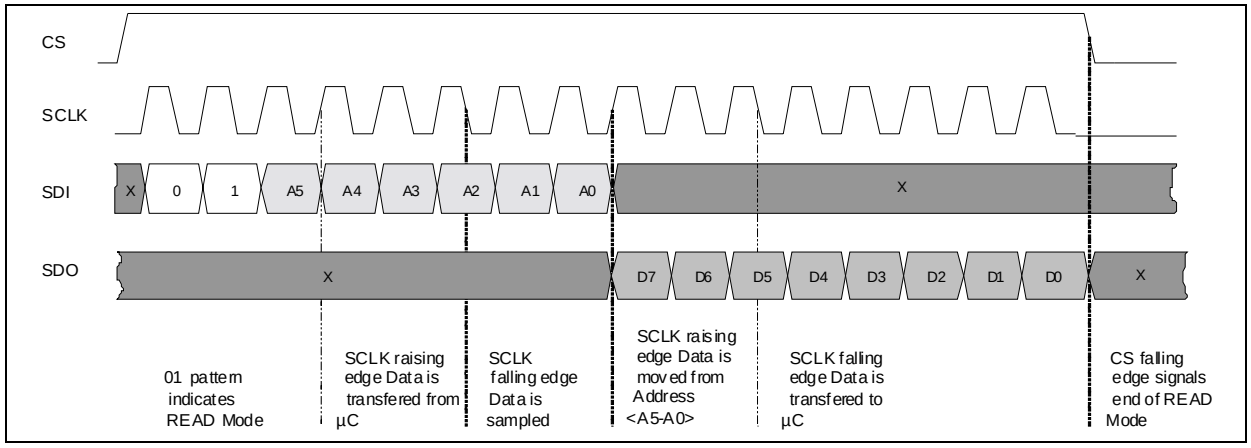
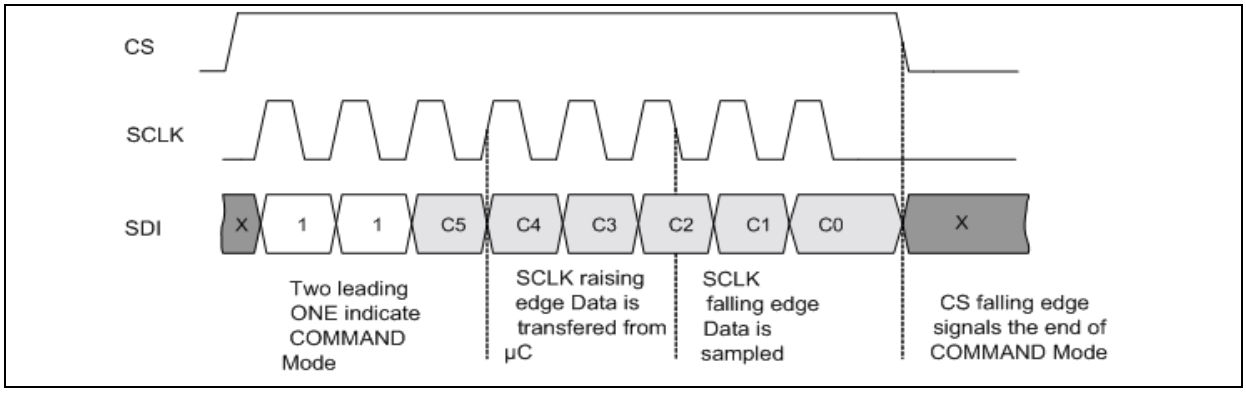


Figure 15. Send Direct COMMAND Byte



8.4 Channel Amplifier and Frequency Detector

The channel amplifier consists of a variable gain amplifier (VGA), an automatic gain control, and a frequency detector. The latter detects the presence of a carrier. As soon as the carrier is detected the AGC is enabled, the gain of the VGA is reduced and set to the right value and the RSSI can be displayed.

8.4.1 Frequency Detector / AGC

The frequency detection uses the RTC as time base. In case the internal RC oscillator is used as RTC, it must be calibrated, but the calibration is guaranteed for a 32.768 kHz crystal oscillator only. The frequency detection criteria can be tighter or more relaxed according to the setup described in R2<1:0>(see Table 13).

Table 13. Tolerance settings for Wakeup

R2<1>	R2<0>	Tolerance
0	0	relaxed
0	1	tighter (medium)
1	0	stringent
1	1	Reserved

The AGC can operate in two modes:

- AGC down only (R1<5>=0)
- AGC up and down (R1<5>=1)

As soon as the AGC starts to operate, the gain in the VGA is set to maximum. If the AGC down only mode is selected, the AGC can only decrease the gain. Since the RSSI is directly derived from the VGA gain, the system holds the RSSI peak.

When the AGC up and down mode is selected, the RSSI can follow the input signal strength variation in both directions.

Regardless which AGC operation mode is used, the AGC needs maximum 35 carrier periods to settle.

The RSSI is stored in the register R10<4:0>.

Both AGC modes (only down or down and up) can also operate with time limitation. This option allows AGC operation only in time slot of 256µs following the internal wake-up. Then the AGC (RSSI) is frozen till the wake-up or RSSI reset occurs.

The RSSI is reset either with the direct command 'clear_wakeup' or 'reset_RSSI'. The 'reset_RSSI' command resets only the AGC setting but does not terminate wake-up condition. This means that if the signal is still present the new AGC setting (RSSI) will appear not later than 300µs (35 LF carrier periods) after the command was received. The AGC setting is reset if for duration of 3 Manchester half symbols no carrier is detected. If the wake-up IRQ is cleared the chip will go back to listening mode.

In case the maximum amplification at the beginning is a drawback (e.g. in noisy environment) it is possible to set a smaller starting gain on the amplifier, according to the Table 14. In this way it is possible to reduce the false frequency detection.

Table 14. Bit setting of Gain Reduction

R4<3>	R4<2>	R4<1>	R4<0>	Gain reduction
0	0	0	0	no gain reduction
0	0	0	1	n.a.
0	0	1	0 or 1	n.a.
0	1	0	0 or 1	-4dB
0	1	1	0 or 1	-8dB
1	0	0	0 or 1	-12dB
1	0	1	0 or 1	-16dB
1	1	0	0 or 1	-20dB
1	1	1	0 or 1	-24dB

8.4.2 Antenna Damper

The antenna damper allows the chip to deal with higher field strength, it is enabled by register R1<4>. It consists of shunt resistors which degrade the quality factor of the resonator by reducing the signal at the input of the amplifier. In this way the resonator sees a smaller parallel resistance (in the band of interest) which degrades its quality factor in order to increase the linear range of the channel amplifier (the amplifier doesn't saturate in presence of bigger signals). Table 15 shows the bit setup.

Table 15. Antenna Damper Bit Setup

R4<5>	R4<4>	Shunt resistor (parallel to the resonator at 125 kHz)
0	0	1 kΩ
0	1	3 kΩ
1	0	9 kΩ
1	1	27 kΩ

8.5 Demodulator / Data Slicer

The performance of the demodulator can be optimized according to bit rate and preamble length as described in Table 16 and Table 17.

Table 16. Bit setup for Envelop Detector for Different Symbol Rates

R3<2>	R3<1>	R3<0>	Symbol rate [Manchester symbols/s]
0	0	0	4096
0	0	1	2184
0	1	0	1490
0	1	1	1130
1	0	0	910
1	0	1	762
1	1	0	655
1	1	1	512

If the bit rate gets higher, the time constant in the envelop detector must be set to a smaller value, this means that higher noise is injected because of the wider band. The next table is a rough indication of how the envelop detector looks like for different bit rates. By using proper data slicer settings it is possible to improve the noise immunity paying the penalty of a longer preamble. In fact if the data slicer has a bigger time constant it is possible to reject more noise, but every time a transmission occurs, the data slicer need time to settle. This settling time will influence the length of the preamble. Table 17 gives a correlation between data slicer setup and minimum required preamble length.

Table 17. Bit setup for Data Slicer for Different Preamble Length

R3<5>	R3<4>	R3<3>	Minimum preamble length [ms]
0	0	0	0.8
0	0	1	1.15
0	1	0	1.55
0	1	1	1.9
1	0	0	2.3
1	0	1	2.65
1	1	0	3
1	1	1	3.5

Note: These times are minimum required, but it is recommended to prolong the preamble.

The comparator of the data slicer can work only with positive or with symmetrical threshold (R3<6>). In addition the threshold can be 20 or 40 mV (R3<7>)

In case the length of the preamble is an issue the data slicer can also work with an absolute threshold (R1<7>). In this case the bits R3<2:0> would not influence the performance. It is even possible to reduce the absolute threshold in case the environment is not particularly noisy (R2<7>).

8.6 Correlator

After frequency detection the data correlation is only performed if the correlator is enabled (R1<1>=1).

The data correlation consists of checking the presence of a preamble (ON/OFF modulated carrier) followed by a certain pattern.

After the frequency detection the correlator waits 16 bits (see bit rate definition in Table 18) and if no preamble is detected the chip is set back to listening mode and the false-wakeup register (R13<7:0>) is incremented by one.

To get started with the pattern correlation the correlator needs to detect at least 4 bits of the preamble (ON/OFF modulated carrier).

The bit duration is defined in the register R7<4:0> according to the Table 18 as function of the Real Time Clock (RTC) periods.

Table 18. Bit Rate Setup

R7<4>	R7<3>	R7<2>	R7<1>	R7<0>	Bit duration in RTC clock periods	Bit rate (bits/s)	Symbol rate (Manchester symbols/s)
0	0	0	1	1	4	8192	4096
0	0	1	0	0	5	6552	3276
0	0	1	0	1	6	5460	2730
0	0	1	1	0	7	4680	2340
0	0	1	1	1	8	4096	2048
0	1	0	0	0	9	3640	1820
0	1	0	0	1	10	3276	1638
0	1	0	1	0	11	2978	1489
0	1	0	1	1	12	2730	1365
0	1	1	0	0	13	2520	1260
0	1	1	0	1	14	2340	1170

Table 18. Bit Rate Setup

R7<4>	R7<3>	R7<2>	R7<1>	R7<0>	Bit duration in RTC clock periods	Bit rate (bits/s)	Symbol rate (Manchester symbols/s)
0	1	1	1	0	15	2184	1092
0	1	1	1	1	16	2048	1024
1	0	0	0	0	17	1926	963
1	0	0	0	1	18	1820	910
1	0	0	1	0	19	1724	862
1	0	0	1	1	20	1638	819
1	0	1	0	0	21	1560	780
1	0	1	0	1	22	1488	744
1	0	1	1	0	23	1424	712
1	0	1	1	1	24	1364	682
1	1	0	0	0	25	1310	655
1	1	0	0	1	26	1260	630
1	1	0	1	0	27	1212	606
1	1	0	1	1	28	1170	585
1	1	1	0	0	29	1128	564
1	1	1	0	1	30	1092	546
1	1	1	1	0	31	1056	528
1	1	1	1	1	32	1024	512

If the preamble is detected correctly the correlator keeps searching for a data pattern. The duration of the preamble plus the pattern should not be longer than 40 bits (see bit rate definition in Table 18). The data pattern can be defined by the user and consists of two bytes which are stored in the registers R5<7:0> and R6<7:0>. The two bytes define the pattern consisting of 16 half bit periods. This means the pattern and the bit period can be selected by the user. The only limitation is that the pattern (in combination with preamble) must obey Manchester coding and timing. It must be noted that according to Manchester coding a down-to-up bit transition represents a symbol "0", while a transition up-to-down represents a symbol "1". If the default code is used (96 [hex]) the binary code is (10 01 01 10 01 10 10 01). MSB has to be transmitted first.

The user can also select (R1<2>) if single or double data pattern is used for wake-up. In case double pattern detection is set, the same pattern has to be repeated 2 times.

Additionally it is possible to set the number of allowed missing zero bits (not symbols) in the received bitstream (R2<6:5>), as shown in the Table 19.

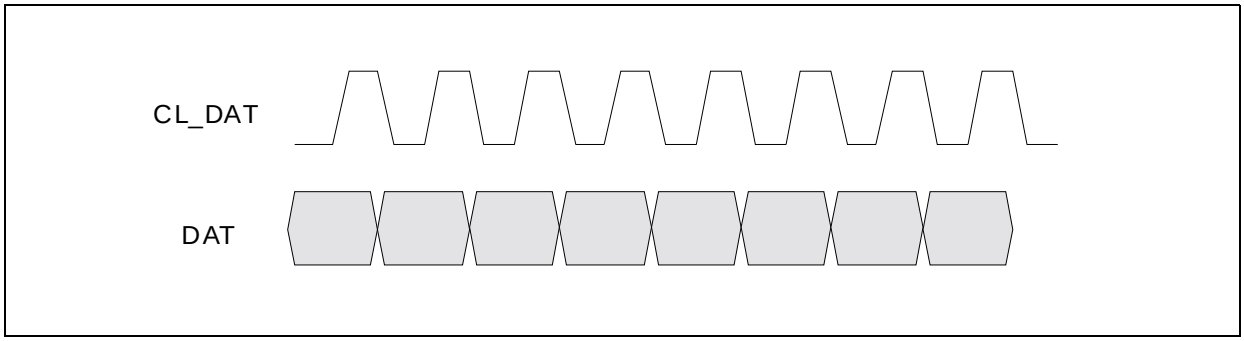
Table 19. Allowed Pattern Detection Errors

R2<6>	R2<5>	Maximum allowed error in the pattern detection
0	0	No error allowed
0	1	1 missed zero
1	0	2 missed zeros
1	1	3 missed zeros

If the pattern is matched the wake-up interrupt is displayed on the WAKE output. In case the Manchester decoder is enabled (R1<3>) the data coming out from the DAT pin are decoded and the clock is recovered on the pin DAT_CL.

The data coming out from the DAT pin are stable (and therefore can be acquired) on the rising edge of the CL_DAT clock, as shown in Figure 16.

Figure 16. Synchronization of Data with Recovered Manchester clock



If the pattern detection fails the internal wake-up (on all active channels) is terminated with no signal sent to MCU and the false wakeup register will be incremented (R13<7:0>).

The wake-up state is terminated with the direct command 'clear_wake' Table 12. This command terminates the MCU activity. The termination can also be automatic in case there is no response from MCU. The time out for automatic termination is set in a register R7<7:5>, as shown in the Table 20.

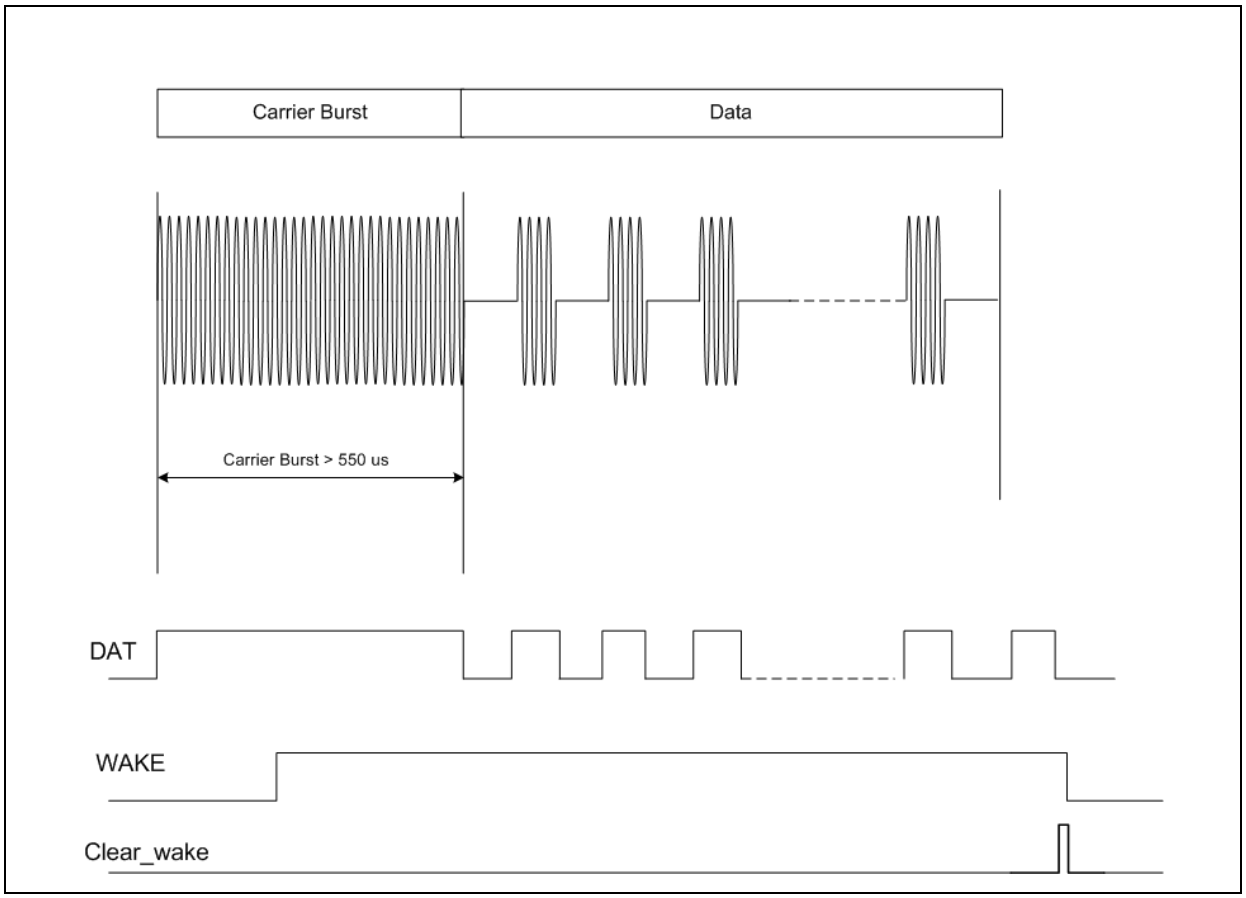
Table 20. Timeout Setup

R7<7>	R7<6>	R7<5>	Time out
0	0	0	0 sec
0	0	1	50 msec
0	1	0	100 msec
0	1	1	150 msec
1	0	0	200 msec
1	0	1	250 msec
1	1	0	300 msec
1	1	1	350 msec

8.7 Wakeup Protocol - Carrier Frequency 125 kHz

8.7.1 Without pattern detection (Manchester decoder disabled)

Figure 17. Wakeup Protocol Overview without Pattern Detection (only carrier frequency detection, Manchester decoder disabled)



In case the data correlation is disabled (R1<1>=0) the AS3930 wakes up upon detection of the carrier frequency only as shown in Figure 17. In order to ensure that AS3930 wakes up the carrier burst has to last longer than 550 µs. To set AS3930 back to listening mode there are two possibilities: either the microcontroller sends the direct command clear_wake via SDI or the time out option is used (R7<7:5>). In case the latter is chosen,AS3930is automatically set to listening mode after the time defined in T_OUT (R7<7:5>), counting starts at the low-to-high WAKE edge on the WAKE pin.

8.7.2 Single Pattern Detection (Manchester decoder disabled)

The Figure 18 shows the wakeup protocol in case the pattern correlation is enabled (R1<1>=1) for a 125 kHz carrier frequency. The initial carrier burst has to be longer than 550 µs and can last maximum 16 bits (see bit rate definition in Table 18). If the ON/OFF mode is used (R1<5>=1), the minimum value of the maximum carrier burst duration is limited to 10 ms. This is summarized in Table 21. In case the carrier burst is too long the internal wakeup will be set back to low and the false wakeup counter (R13<7:0>) will be incremented by one.

The carrier burst must be followed by a preamble (0101... modulated carrier with a bit duration defined in Table 18) and the wakeup pattern stored in the registers R5<7:0> and R6<7:0>. The preamble must have at least 4 bits and the preamble duration together with the pattern should not be longer than 40 bits. If the wakeup pattern is correct the signal on the WAKE pin is set to high and the data transmission can get started. To set the chip back to listening mode the direct command clear_false, as well as the time out option (R7<7:5>) can be used.

Figure 18. Wakeup Protocol Overview with Single Pattern Detection (Manchester decoder disabled)

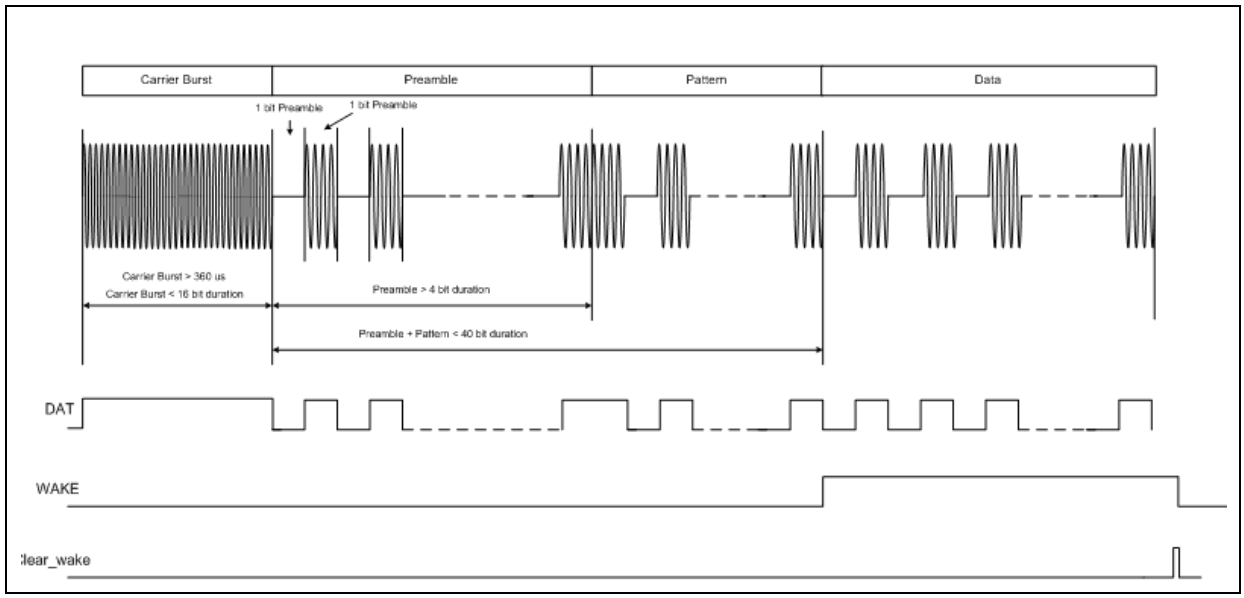


Table 21. Preamble Requirements in Standard Mode, Scanning Mode and ON/OFF Mode

Bit rate (bit/s)	Maximum duration of the carrier burst in Standard Mode and Scanning Mode (ms)	Maximum duration of the carrier burst in ON/OFF Mode (ms)
8192	1.95	10
6552	2.44	10
5460	2.93	10
4680	3.41	10
4096	3.90	10
3640	4.39	10
3276	4.88	10
2978	5.37	10
2730	5.86	10
2520	6.34	10
2340	6.83	10
2184	7.32	10
2048	7.81	10
1926	8.30	10
1820	8.79	10
1724	9.28	10
1638	9.76	10
1560	10.25	10.25
1488	10.75	10.75
1424	11.23	11.23
1364	11.73	11.73
1310	12.21	12.21
1260	12.69	12.69

Table 21. Preamble Requirements in Standard Mode, Scanning Mode and ON/OFF Mode

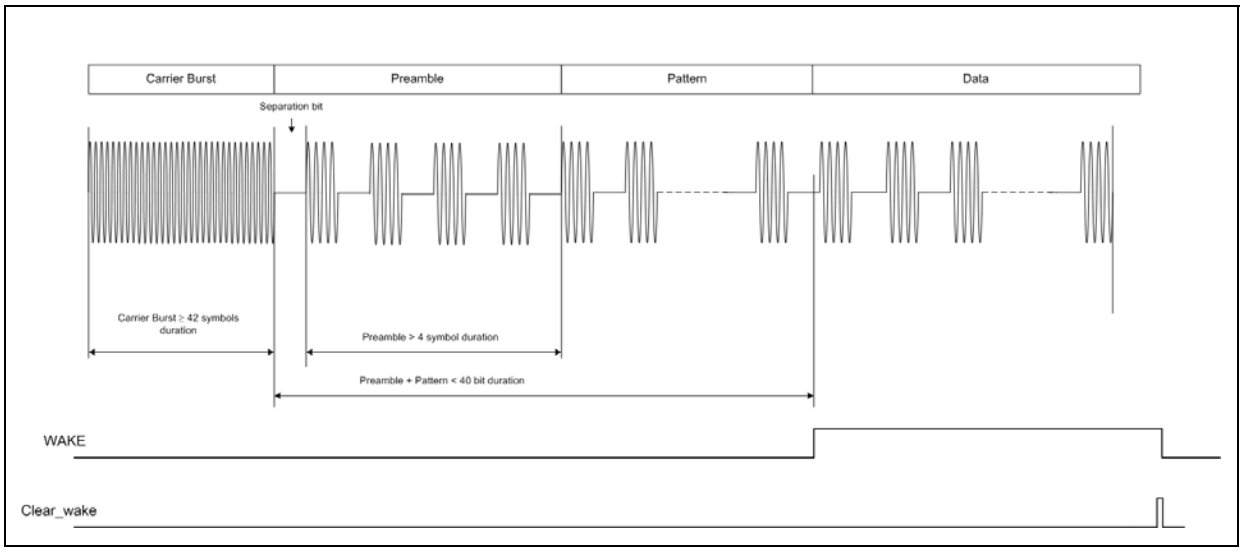
Bit rate (bit/s)	Maximum duration of the carrier burst in Standard Mode and Scanning Mode (ms)	Maximum duration of the carrier burst in ON/OFF Mode (ms)
1212	13.20	13.20
1170	13.67	13.67
1128	14.18	14.18
1092	14.65	14.65
1056	15.15	15.15
1024	15.62	15.62

8.7.3 Single Pattern Detection (Manchester decoder enabled)

The Figure 19 shows the wakeup protocol in case both the pattern correlation and the Manchester decoder are enabled (R1<1>=1 and R1<3>=1) for a 125 kHz carrier frequency. The initial carrier burst has to be at least 42 Manchester symbols long and has to be followed by a separation bit (one bit of no-carrier). The carrier burst must be followed by a minimum 4 Manchester symbol preamble (10101010) and the pattern stored in the R5<7:0> and R6<7:0>. The preamble can only be made up by integer Manchester symbol and the preamble duration together with the pattern should not be longer than 40 bits. If the pattern is correct the signal on the WAKE pin is set to high, the data are internally decoded and the Manchester clock is recovered. To set the AS3930 back to listening mode the direct command clear_false or the time out option (R7<7:5>) can be used.

In case the On/OFF mode is enabled the Manchester decoder can not be used.

Figure 19. Wakeup Protocol Overview with Single Pattern Detection (Manchester decoder enabled)



8.8 False Wakeup Register

The wakeup strategy in the AS3930 is based on 2 steps:

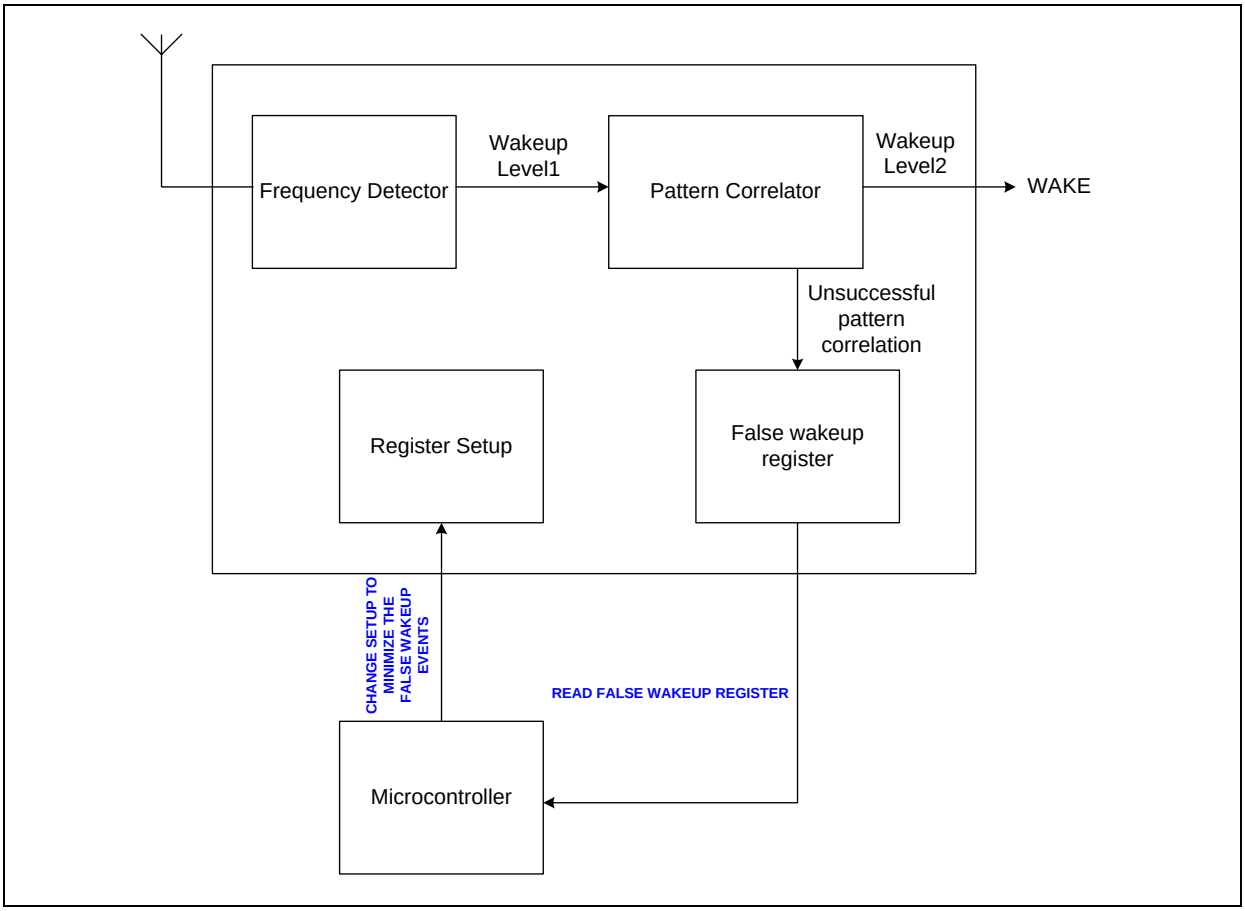
1. Frequency Detection: in this phase the frequency of the received signal is checked.
2. Pattern Correlation: here the pattern is demodulated and checked whether it corresponds to the valid one.

If there is a disturber or noise capable to overcome the first step (frequency detection) without producing a valid pattern, then a false wakeup call happens.Each time this event is recognized a counter is incremented by one and the respective counter value is stored in a memory cell (false wakeup register). Thus, the microcontroller can periodically look at the false wakeup register, to get a feeling how noisy the surrounding environment is and can then react accordingly (e.g. reducing the gain of the LNA during frequency detection, set the AS3930 temporarily to power down etc.), as shown in the Figure 20. The false wakeup counter is a useful tool to quickly adapt the system to any changes in the noise environment and thus avoid false wakeup events.

Most wakeup receivers have to deal with environments that can rapidly change. By periodically monitoring the number of false wakeup events it is possible to adapt the system setup to the actual characteristics of the environment and enables a better use of the full flexibility of AS3930.

Note: If the Manchester decoder is enabled, the false wakeup register is not able to store the false wakeup events.

Figure 20. Concept of False Wakeup Register together with System



8.9 Real Time Clock (RTC)

The RTC can be based on a crystal oscillator (R1<0>=1), the internal RC-oscillator (R1<0>=0) or an external clock source (R1<0>=1). The crystal has higher precision of the frequency but a higher current consumption and needs three external components (crystal plus two capacitors). The RC-oscillator is completely integrated and can be calibrated if a reference signal is available for a very short time to improve the frequency accuracy. The calibration gets started with the trim_osc direct command. Since no non-volatile memory is available on the chip, the calibration must be done every time after battery replacement. Since the RTC defines the time base of the frequency detection, the selected frequency (frequency of the crystal oscillator or the reference frequency used for calibration of the RC oscillator) should be about one forth of the carrier frequency:

$$F_{RTC} \sim F_{CAR} * 0.25 \qquad \text{(EQ 1)}$$

Where: F_{CAR} is the carrier frequency and F_{RTC} is the RTC frequency

Note: The third option for the RTC is the use of an external clock source, which must be applied directly to the XIN pin (XOUT floating).

8.9.1 Crystal Oscillator

Table 22. Characteristics of XTAL

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Crystal accuracy (initial)	Overall accuracy			±120	p.p.m.
	Crystal motional resistance				60	KΩ
	Frequency			32.768		kHz
	Contribution of the oscillator to the frequency error			±5		p.p.m
	Start-up Time	Crystal dependent		1		s
	Duty cycle		45	50	55	%
	Current consumption			1		µA

8.9.2 RC-Oscillator

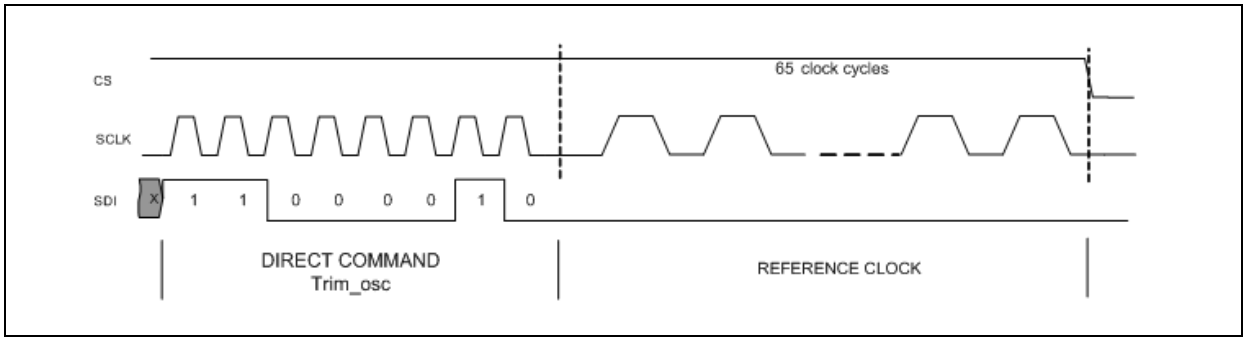
Table 23. Characteristics of RCO

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Frequency	If no calibration is performed	27	32.768	42	kHz
		If calibration is performed	31	32.768	34.5	kHz
	Calibration time	Periods of reference clock			65	cycles
	Current consumption			200		nA

To trim the RC-Oscillator, set the chip select (CS) to high before sending the direct command trim_osc over SDI. Then 65 digital clock cycles of the reference clock (e.g. 32.768 kHz) have to be sent on the clock bus (SCL), as shown in Figure 21. After that the signal on the chip select (CS) has to be pulled down.

The calibration is effective after the 65th reference clock edge and it will be stored in a volatile memory. In case the RC-oscillator is switched off or a power-on-reset happens (e.g. battery change) the calibration has to be repeated.

Figure 21. RC-Oscillator calibration via SDI



8.9.3 External Clock Source

To clock the AS3930 with an external signal the crystal oscillator has to be enabled (R1<1>=1). As shown in the Figure 3 the clock must be applied on the pin XIN while the pin XOUT must stay floating. The RC time constant has to be 100µs with a tolerance of ±10% (e.g. R=680 kΩ and C=22pF). In the Table 24 the clock characteristics are summarized.

Table 24. Characteristics of External Clock

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vl	Low level		0		0.1* V_{DD}	V
Vh	High level		0.9*V_{DD}		V_{DD}	V

Table 24. Characteristics of External Clock

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Tr	Rise-time				3	µs
Tf	Fall-time				3	µs
T=1/2πRC	RC Time constant		90	100	110	µs

Note: In power down mode the external clock has to be set to V_{DD}.

9 Package Drawings and Markings

The product is available in 16 pin TSSOP and QFN 4x4 16 LD packages.

Figure 22. Package Diagram 16 pin TSSOP

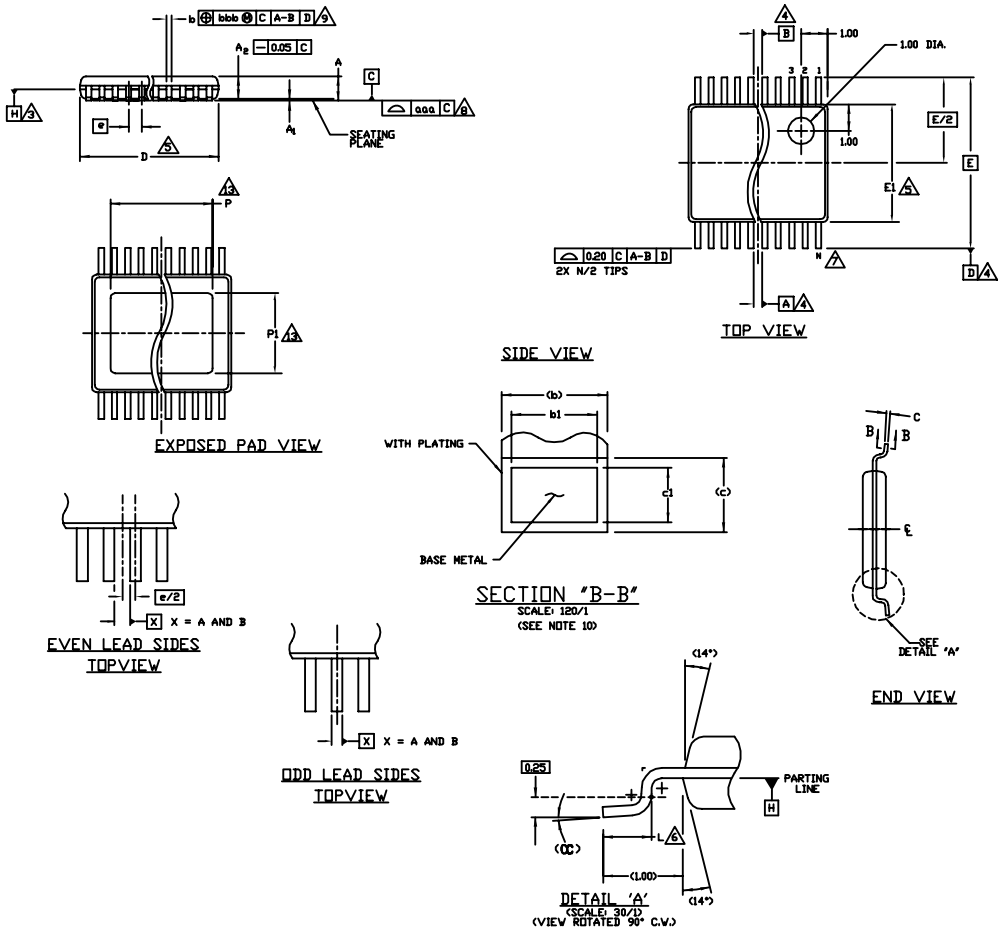


Table 25. Package Dimensions 16 pin TSSOP

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max			
A			1.10	E	6.40 BSC					
A1	0.05		0.15	L	0.50	0.60	0.70			
A2	0.85	0.90	0.95	a	0°	4°	8°			
aaa	0.076			N, P, P1	See Variations					
b	0.19	-	0.30	Variations:						
b1	0.19	0.22	0.25		D			P	P1	N
bbb	0.10			AA/AAT	2.90	3.00	3.10	1.59	3.2	8
C	0.09	-	0.20	AB-1/ABT-1	4.90	5.00	5.10	3.1	3.0	14
C1	0.09	0.127	0.16	AB/ABT	4.90	5.00	5.10	3.0	3.0	16
D	See Variations			AC/ACT	6.40	6.50	6.60	4.2	3.0	20
E1	4.30	4.40	4.50	AD/ADT	7.70	7.80	7.90	5.5	3.2	24
e	0.65 BSC			AE/AET	9.60	9.70	9.80	5.5	3.0	28

Note:

1. Die thickness allowable is 0.279 ± 0.0127.
2. Dimensioning and tolerances conform to *ASME Y14.5M-1994*.
3. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
4. Datum A-B and D to BE determined where center line between leads exits plastic body at datum plane H.
5. D & E1 are reference datum and do not include mold flash or protrusions, and are measured at the bottom parting line. Mold lash or protrusions shall not exceed 0.15mm on D and 0.25mm on E per side.
6. Dimension is the length of terminal for soldering to a substrate.
7. Terminal positions are shown for reference only.
8. Formed leads shall be planar with respect to one another within 0.076mm at seating plane.
9. The lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.07mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusions and an adjacent lead should be 0.07mm for 0.65mm pitch.
10. Section B-B to be determined at 0.10mm to 0.25mm from the lead tip.
11. Dimensions P and P1 are thermally enhanced variations. Values shown are maximum size of exposed pad within lead count and body size. End user should verify available size of exposed pad for specific device application.
12. All dimensions are in millimeters, angle is in degrees.
13. N is the total number of terminals.

Figure 23. Package Diagram QFN 4x4 16 LD

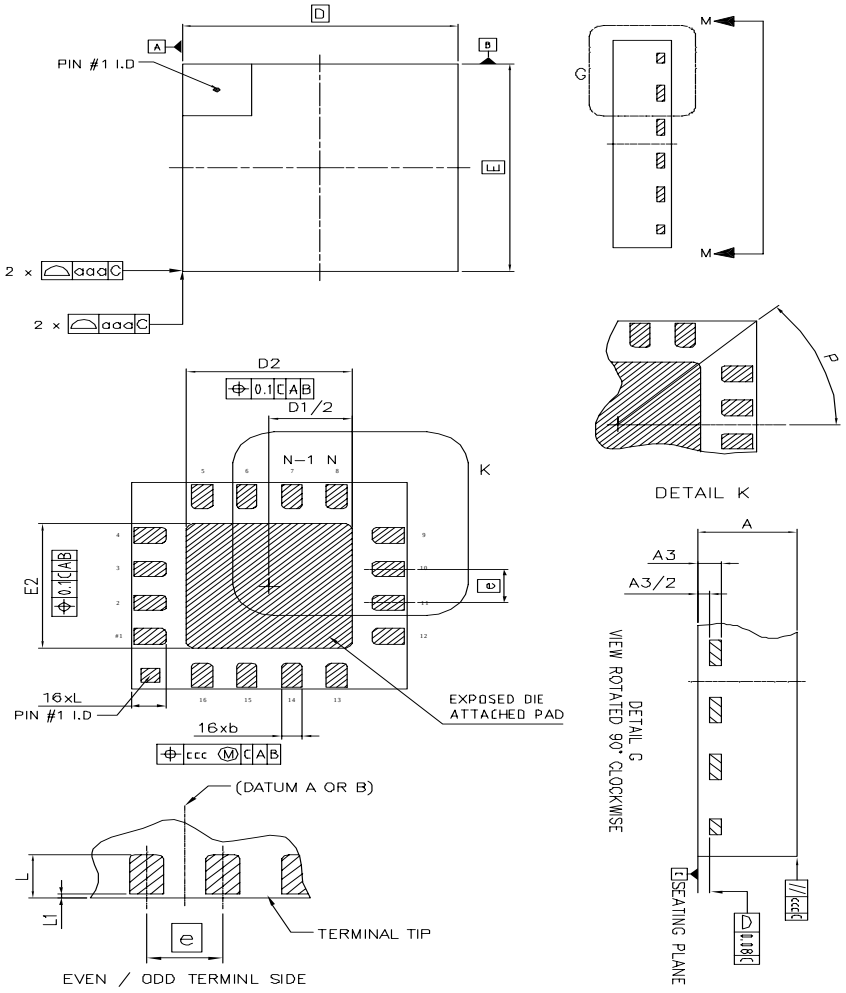


Table 26. Package Dimensions QFN 4x4 16 LD

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.75	0.85	0.95	e		0.65 BSC	
A1		0.203 REF		L	0.40	0.50	0.60
b	0.25	0.30	0.35	L1			0.10
D		4.00 BSC		P		45° BSC	
E		4.00 BSC		aaa		0.15	
D2	2.30	2.40	2.50	ccc		0.10	
E2	2.30	2.40	2.50				

Note:

1. Die thickness allowable is 0.279 ± 0.0127.
2. Dimensioning and tolerances conform to *ASME Y14.5M-1994*.
3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional

Revision History

Table 27. Revision History

Revision	Date	Owner	Description
1.0	07/10/09	rlc	

10 Ordering Information

Table 28. Ordering Information

Ordering Code	Type	Marking	Delivery Form[1]	Delivery Quantity
AS3930-BTST	16 pin TSSOP	AS3930	7 inches Tape&Reel	1000 pcs
AS3930-BQFT	QFN 4x4 16 LD	AS3930	7 inches Tape&Reel	1000 pcs

1. Dry Pack Sensitivity Level =3 according to IPC/JEDEC J-STD-033A for full reels.

Note: All products are RoHS compliant and Pb-free.
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