DS90LV027AQ Automotive LVDS Dual Differential Driver

Check for Samples: DS90LV027AQ

FEATURES

- **AECQ-100 Grade 1**
- **>600 Mbps (300MHz) Switching Rates**
- **0.3 ns Typical Differential Skew**
- **0.7 ns Maximum Differential Skew**
- **3.3V Power Supply Design**
- **Low Power Dissipation (46 mW @ 3.3V Static)**
- **Flow-Through Design Simplifies PCB Layout**
- **Power Off Protection (Outputs in High Impedance)**
- **Conforms to TIA/EIA-644 Standard**
- **8-Lead SOIC Package Saves Space**

DESCRIPTION

The DS90LV027AQ is a dual LVDS driver device optimized for high data rate and low power applications. The device is designed to support data rates in excess of 600Mbps (300MHz) utilizing Low Voltage Differential Signaling (LVDS) technology. The DS90LV027AQ is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized.

The device is in a 8-lead SOIC package. The DS90LV027AQ has a flow-through design for easy PCB layout. The differential driver outputs provides low EMI with its typical low output swing of 360 mV. It is perfect for high speed transfer of clock and data. The DS90LV027AQ can be paired with its companion dual line receiver, the DS90LV028AQ, or with any of TI's LVDS receivers, to provide a high-speed point-to-point LVDS interface.

Connection Diagram

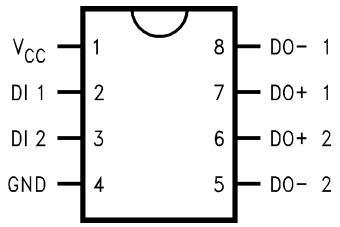
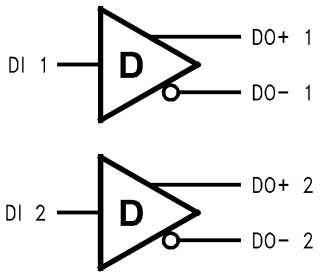


Figure 1. Dual-In-Line
See Package Number D0008A

Functional Diagram



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage (V_{CC})	−0.3V to +4V
Input Voltage (DI)	−0.3V to (V_{CC} + 0.3V)
Output Voltage (DO±)	−0.3V to +3.9V
Maximum Package Power Dissipation @ +25°C	
D Package	1068 mW
Derate D Package	9.71 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
θ_{JA}	103.0°C/W
θ_{JC}	50.0°C/W
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering	
(4 sec.)	+260°C
Maximum Junction Temperature	+135°C
ESD Ratings	
HBM (3)	≥ 8kV
MM (4)	≥ 250V
CDM (5)	≥ 1250V

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114C
(4) Machine Model, applicable std. JESD22-A115-A
(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Temperature (T_A)	−40	25	+125	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)(2)(3)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS							
V_{OD}	Output Differential Voltage	R_L = 100Ω (Figure 2)	DO+, DO−	250	360	450	mV
ΔV_{OD}	V_{OD} Magnitude Change				1	35	mV
V_{OH}	Output High Voltage				1.4	1.6	V
V_{OL}	Output Low Voltage			0.9	1.1		V
V_{OS}	Offset Voltage			1.125	1.2	1.375	V
ΔV_{OS}	Offset Magnitude Change			0	3	25	mV
I_{OXD}	Power-off Leakage	V_{OUT} = V_{CC} or GND, V_{CC} = 0V			±1	±10	µA
I_{OSD}	Output Short Circuit Current				−5.7	−8	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}.
(2) All typicals are given for: V_{CC} = +3.3V and T_A = +25°C.
(3) The DS90LV027AQ is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.

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Electrical Characteristics (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)(2)(3)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS								
V_{IH}	Input High Voltage			DI	2.0		V_{CC}	V
V_{IL}	Input Low Voltage				GND		0.8	V
I_{IH}	Input High Current	V_{IN} = 3.3V or 2.4V				±2	±10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.5V				±1	±10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.6		V
I_{CC}	Power Supply Current	No Load	V_{IN} = V_{CC} or GND	V_{CC}		8	14	mA
		R_L = 100Ω				14	20	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified.(1)(2)(3)(4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS						
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 15 pF	0.3	0.8	2.0	ns
t_{PLHD}	Differential Propagation Delay Low to High	(Figure 3 and Figure 4)	0.3	1.1	2.0	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$ (5)		0	0.3	0.7	ns
t_{SKD2}	Channel to Channel Skew (6)		0	0.4	0.8	ns
t_{SKD3}	Differential Part to Part Skew (7)		0		1.0	ns
t_{SKD4}	Differential Part to Part Skew (8)		0		1.7	ns
t_{TLH}	Transition Low to High Time		0.2	0.5	1.0	ns
t_{THL}	Transition High to Low Time		0.2	0.5	1.0	ns
f_{MAX}	Maximum Operating Frequency (9)			350		MHz

(1) All typicals are given for: V_{CC} = +3.3V and T_A = +25°C.
(2) These parameters are ensured by design. The limits are based on statistical analysis of the device over PVT (process, voltage, temperature) ranges.
(3) C_L includes probe and fixture capacitance.
(4) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r ≤ 1 ns, t_f ≤ 1 ns (10%-90%).
(5) t_{SKD1}, $|t_{PHLD} - t_{PLHD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(6) t_{SKD2} is the Differential Channel to Channel Skew of any event on the same device.
(7) t_{SKD3}, Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(8) t_{SKD4}, part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
(9) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, 0V to 3V. Output criteria: duty cycle = 45%/55%, V_{OD} > 250mV, all channels switching.

Parameter Measurement Information

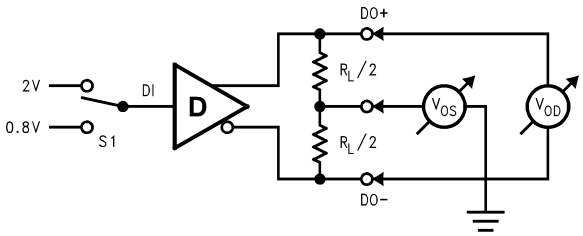

Figure 2. Differential Driver DC Test Circuit

Parameter Measurement Information (continued)

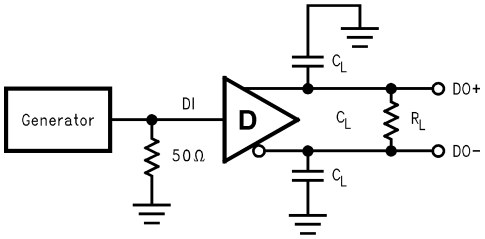

Figure 3. Differential Driver Propagation Delay and Transition Time Test Circuit

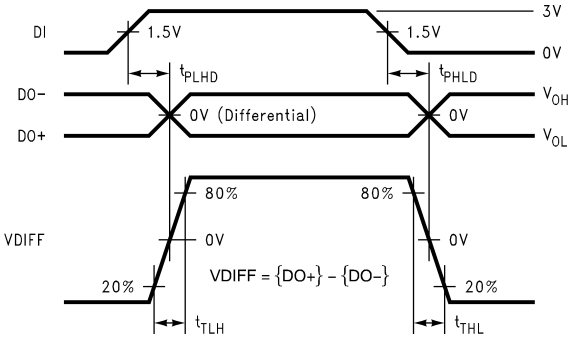

Figure 4. Differential Driver Propagation Delay and Transition Time Waveforms

APPLICATION INFORMATION

DEVICE PIN DESCRIPTIONS

Pin #	Name	Description
2, 3	DI	TTL/CMOS driver input pins
6, 7	DO+	Non-inverting driver output pin
5, 8	DO−	Inverting driver output pin
4	GND	Ground pin
1	V_{CC}	Positive power supply pin, +3.3V ± 0.3V

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Typical Performance Curves

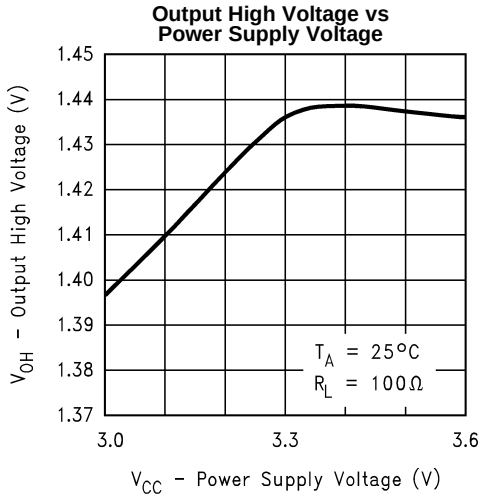

Figure 5.

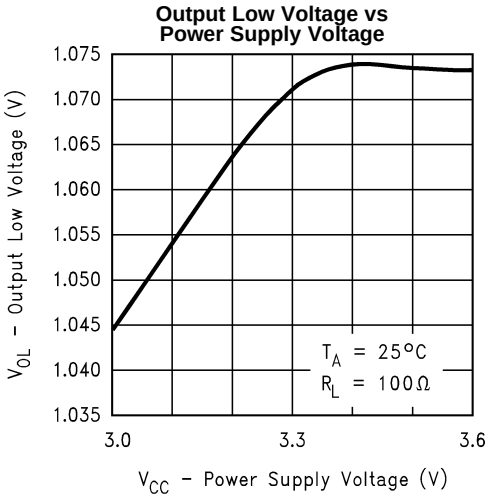

Figure 6.

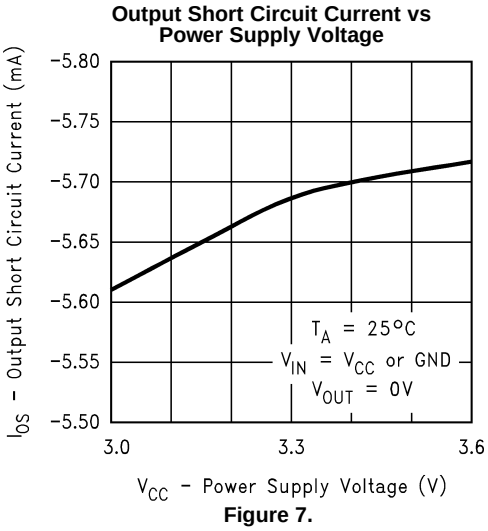

Figure 7.

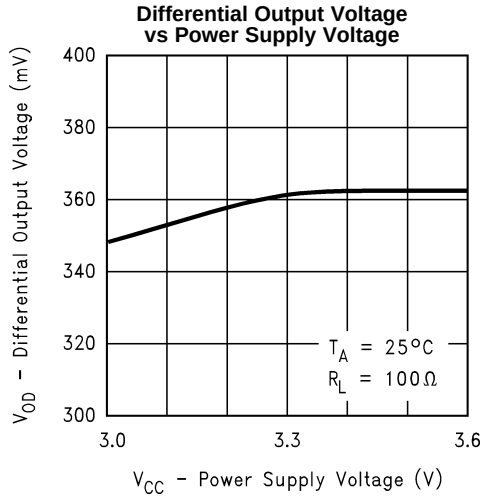

Figure 8.

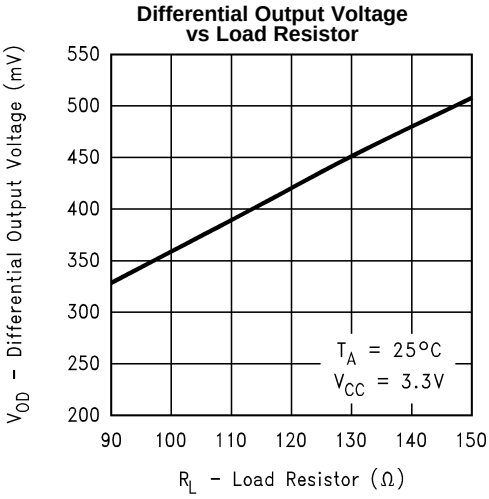

Figure 9.

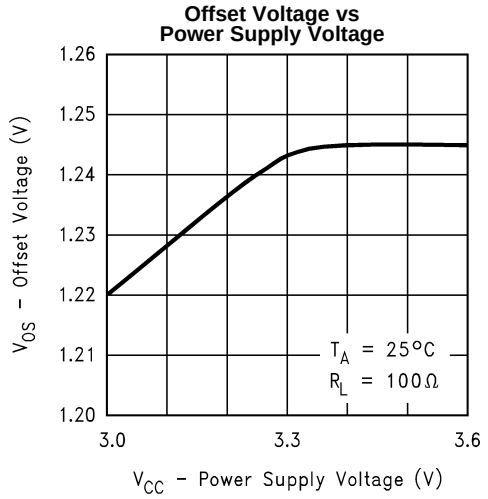

Figure 10.

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Typical Performance Curves (continued)

Power Supply Current vs Frequency

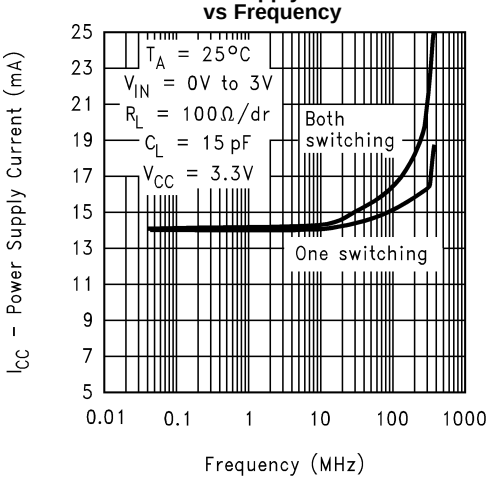

Figure 11.

Power Supply Current vs Power Supply Voltage

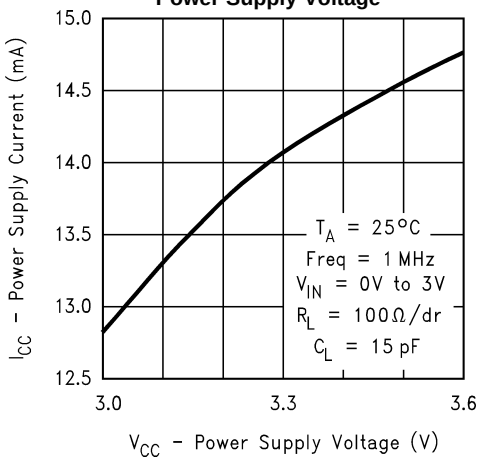

Figure 12.

Power Supply Current vs Ambient Temperature

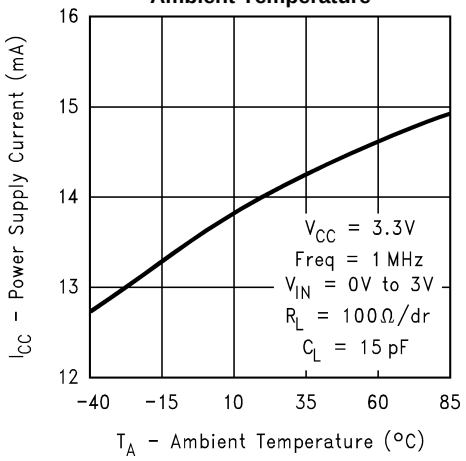

Figure 13.

Differential Propagation Delay vs Power Supply Voltage

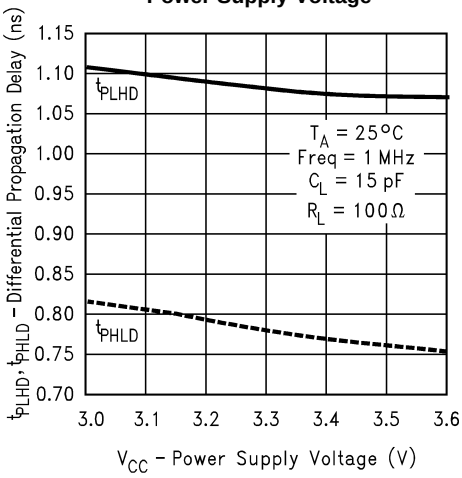

Figure 14.

Differential Propagation Delay vs Ambient Temperature

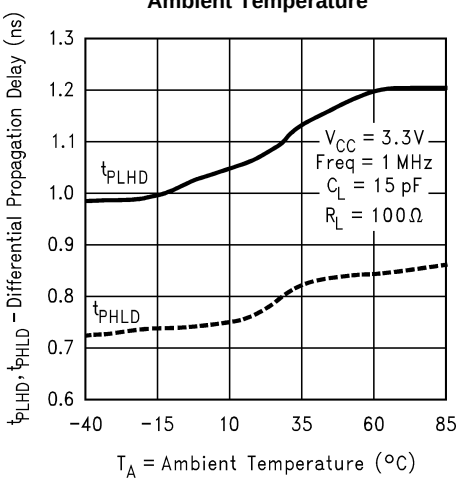

Figure 15.

Differential Skew vs Power Supply Voltage

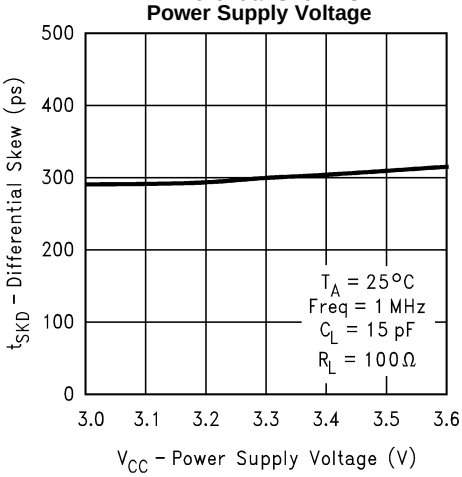

Figure 16.

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Typical Performance Curves (continued)

Differential Skew vs Ambient Temperature

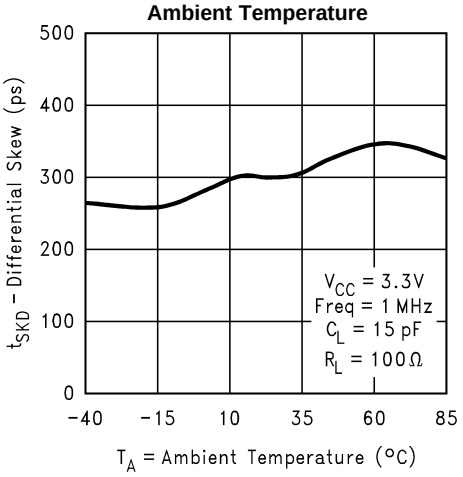

Figure 17.

Transition Time vs Power Supply Voltage

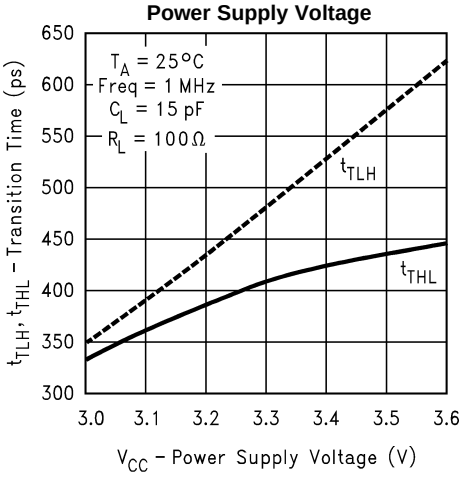

Figure 18.

Transition Time vs Ambient Temperature

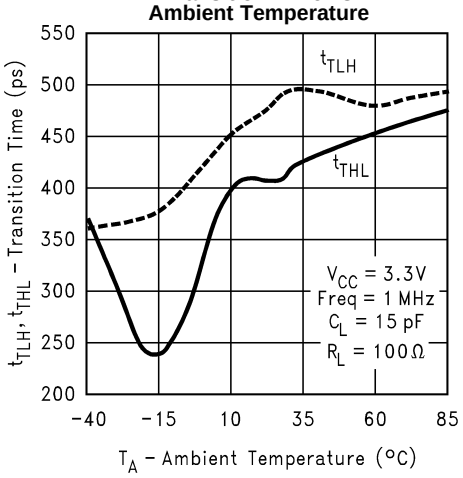

Figure 19.

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	7

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90LV027AQMA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	90LV0 27AQM
DS90LV027AQMA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	90LV0 27AQM
DS90LV027AQMA/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	-	Call TI	Call TI	-40 to 125	
DS90LV027AQMAX/NO.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	90LV0 27AQM
DS90LV027AQMAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	90LV0 27AQM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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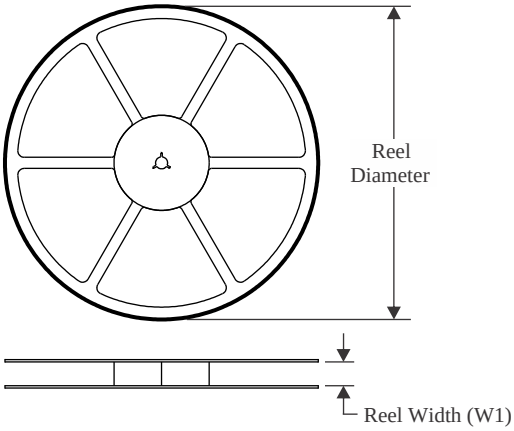
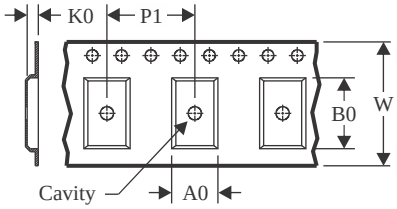
TAPE AND REEL INFORMATION

REEL DIMENSIONS

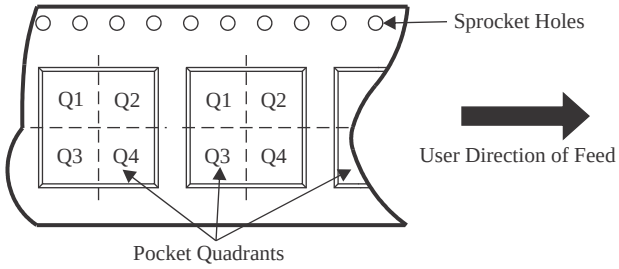


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

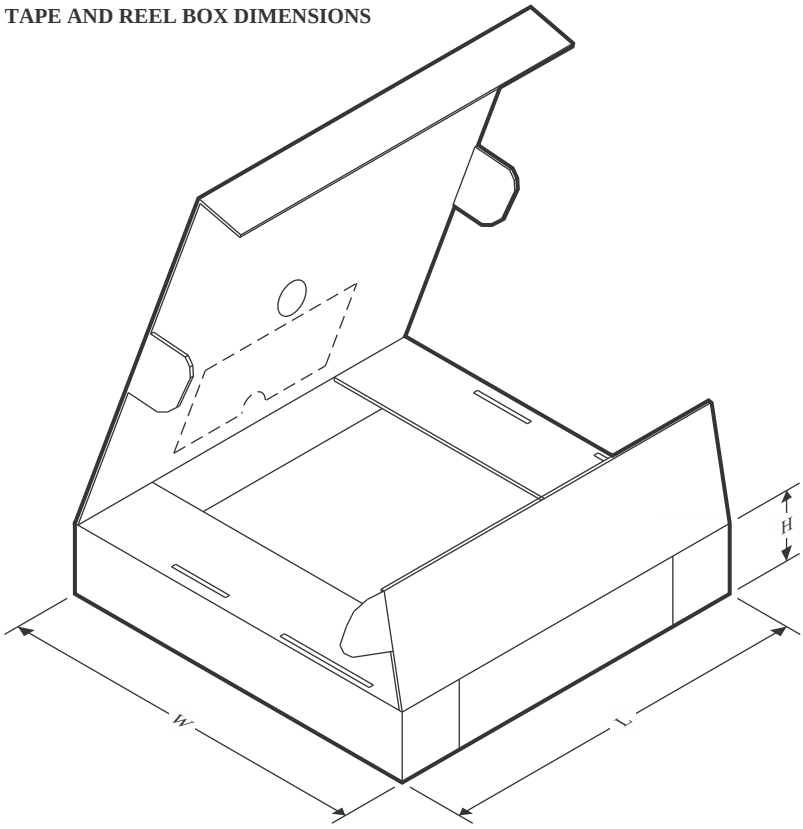
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV027AQMAX/ NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

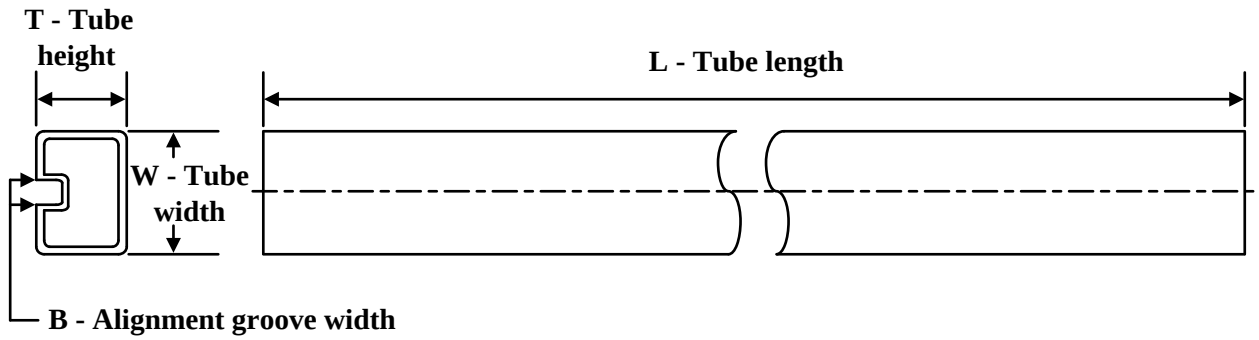
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

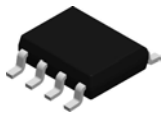
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV027AQMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS90LV027AQMA/NOPB	D	SOIC	8	95	495	8	4064	3.05
DS90LV027AQMA/ NOPB.A	D	SOIC	8	95	495	8	4064	3.05

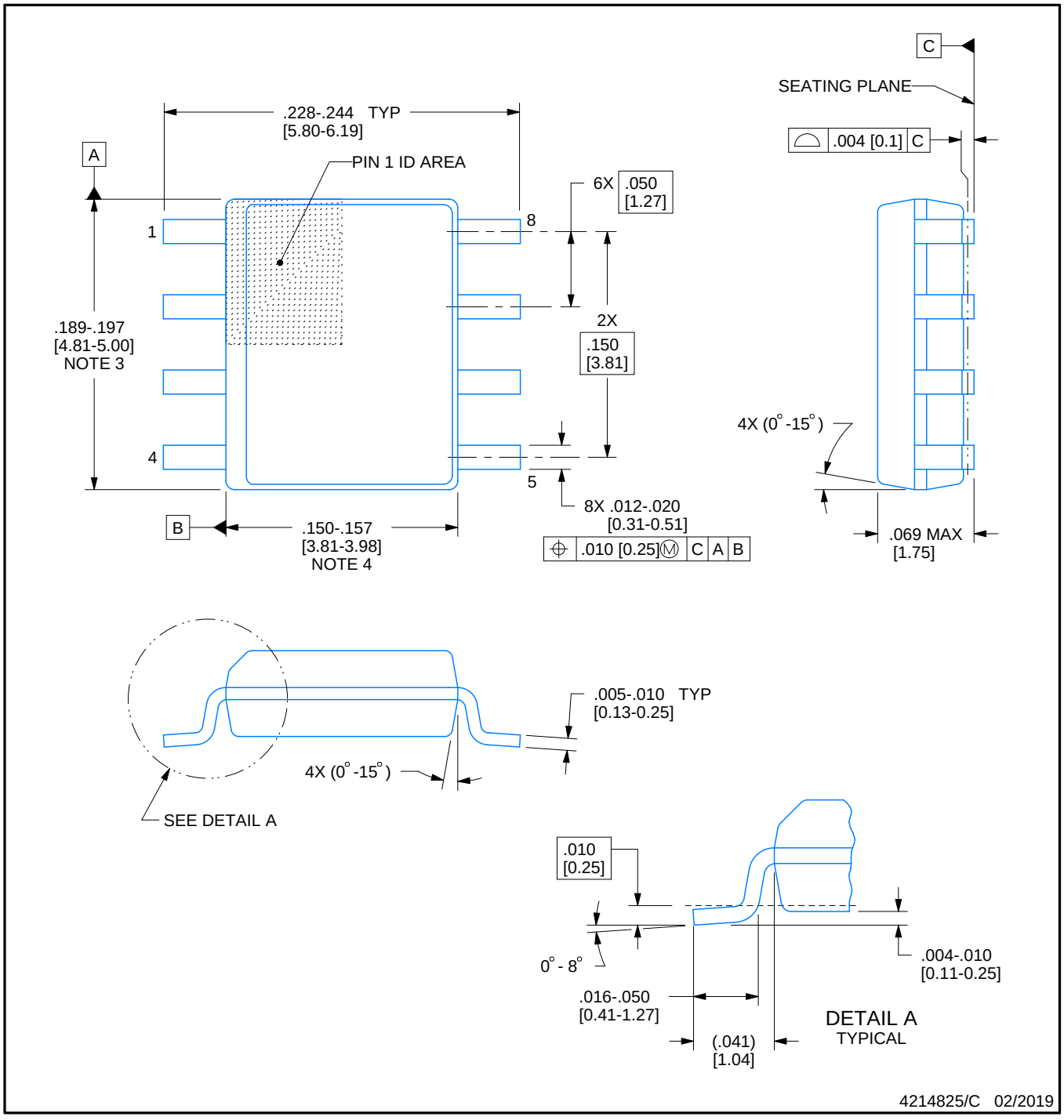


PACKAGE OUTLINE

D0008A

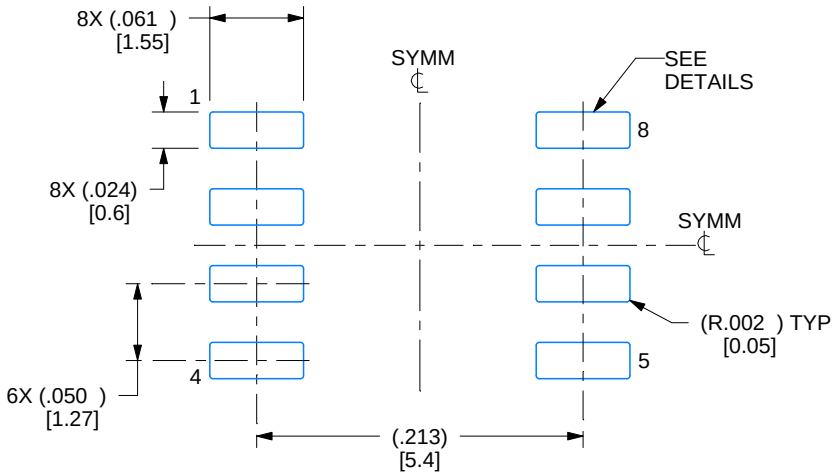
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

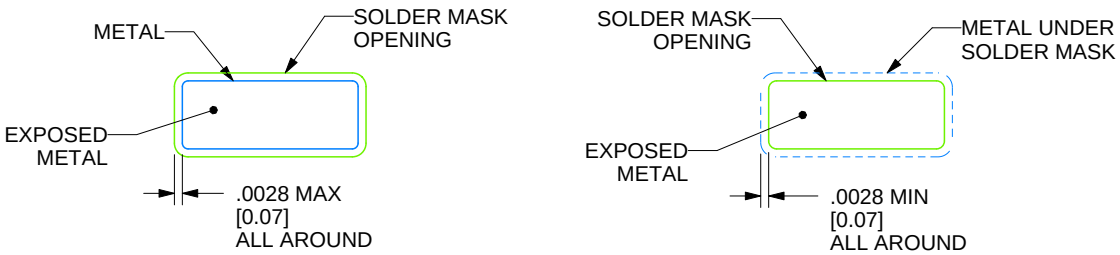


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

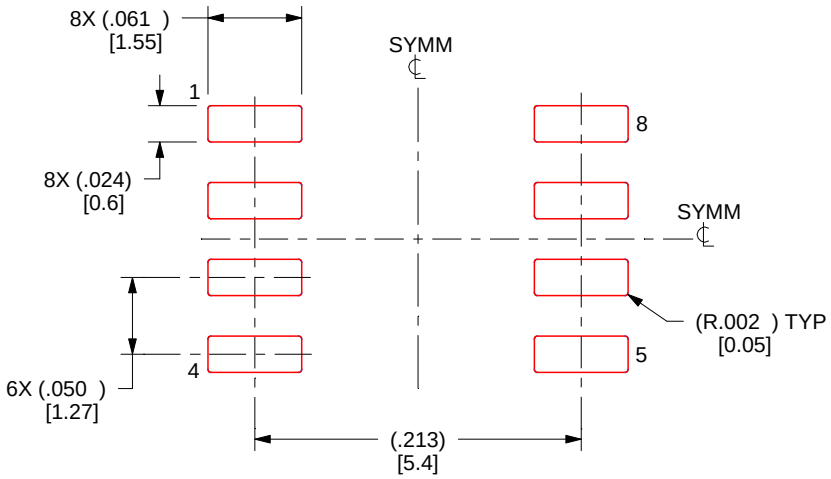
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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