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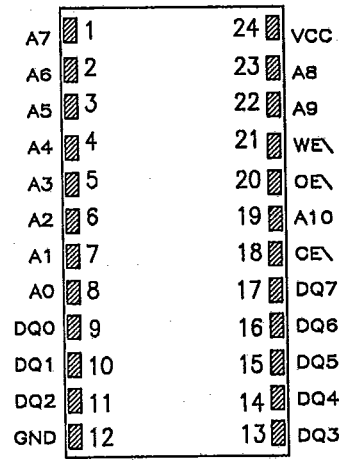
DALLAS SEMICONDUCTOR

DS1220AB/AD
16K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 2K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 100ns, 120ns, 150ns, or 200ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN DESCRIPTION



24-PIN ENCAPSULATED PACKAGE
(720 Mil Extended)

PIN NAMES (\ Denotes Condition Low)

A_0-A_{10}	- Address Inputs
CE\	- Chip Enable
GND	- Ground
DQ_0-DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
WE\	- Write Enable
OE\	- Output Enable

DESCRIPTION

The DS1220AB and DS1220AD are 16,384-bit, fully static, nonvolatile RAMs organized as 2048 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The DS1220AB/AD can be used in place of existing 2K x 8 SRAMs directly conforming to the popular bytewide 24-pin DIP standard. The DS1220AB also matches the pinout of the 2716 EPROM or the 2816 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1220AB and DS1220AD execute a read cycle whenever WE\ (Write Enable) is inactive (high) and CE\ (Chip Enable) is active (low). The unique address specified by the 11 address inputs (A_0-A_{10}) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that the CE\ and OE\ (Output Enable) access times are also satisfied. If OE\ and CE\ access times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access.

WRITE MODE

The DS1220AB and DS1220AD are in the write mode whenever the WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The OE\ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1220AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5V. The DS1220AD provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25V. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for the DS1220AD and 4.75 volts for the DS1220AB.

SHIPPING AND START-UP

The DS1220AB/AD is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS
DS1220AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V
DS1220AD Power Supply Voltage	V_{CC}	4.50	5.0	5.50	V
Input Logic 1	V_{IH}	2.2		V_{CC}	V
Input Logic 0	V_{IL}	0.0		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10% for DS1220AD)
(0°C to 70°C; V_{CC} = 5V ± 5% for DS1220AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	-1.0		+1.0	uA
I/O Leakage Current CE\ ≥ V_{IH} ≤ V_{CC}	I_{IO}	-1.0		+1.0	uA
Output Current @ 2.4V	I_{OH}	-1.0			mA
Output Current @ 0.4V	I_{OL}	2.0			mA
Standby Current CE\=2.2V	I_{CCS1}		5.0	10.0	mA
Standby Current CE\= V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA
Operating Current t_{CYC}=200ns (Commercial)	I_{CCO1}			75	mA
Operating Current t_{CYC}=200ns (Industrial)	I_{CCO1}			85	mA
Write Protection Voltage (DS1220AB)	V_{TP}	4.5	4.62	4.75	V
Write Protection Voltage (DS1220AD)	V_{TP}	4.25	4.37	4.5	V

DC TEST CONDITIONS

Outputs open.

All voltages are referenced to ground.

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	TYP	MAX	UNITS
Input Capacitance	C_{IN}	5	10	pF
Input/Output Capacitance	$C_{I/O}$	5	10	pF

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V ± 10% for DS1220AD)
(0°C to 70°C, V_{CC} = 5.0V ± 5% for DS1220AB)

		DS1220AD-100 DS1220AB-100		DS1220AD-120 DS1220AB-120		DS1220AD-150 DS1220AB-150		DS1220AD-200 DS1220AB-200			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	100		120		150		200		ns	
Access Time	t_{ACC}		100		120		150		200	ns	
OE\ to Output Valid	t_{OE}		50		60		70		100	ns	
CE\ to Output Valid	t_{CO}		100		120		150		200	ns	
OE\ or CE\ to Output Active	t_{COE}	5		5		5		5		ns	5
Output High Z from Deselection	t_{OD}		35		40		70		100	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		5		ns	
Write Cycle Time	t_{WC}	100		120		150		200		ns	
Write Pulse Width	t_{WP}	75		90		100		150		ns	3
Address Setup Time	t_{AW}	0		0		0		0		ns	
Write Recovery Time	t_{WR}	20		20		20		20		ns	
Output High Z from WE\	t_{ODW}		35		40		70		80	ns	5
Output Active from WE\	t_{OEW}	5		5		5		5		ns	5
Data Setup Time	t_{DS}	40		50		60		80		ns	4
Data Hold Time	t_{DH}	20		20		20		20		ns	4

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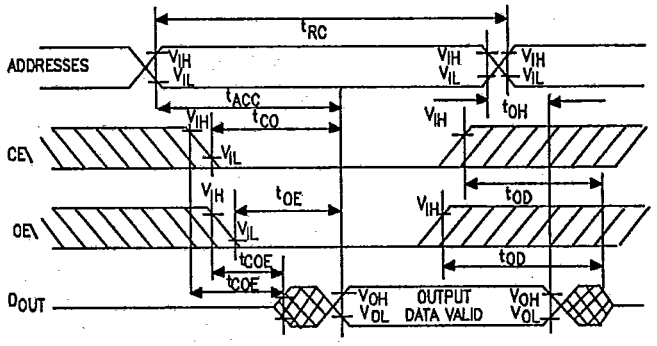
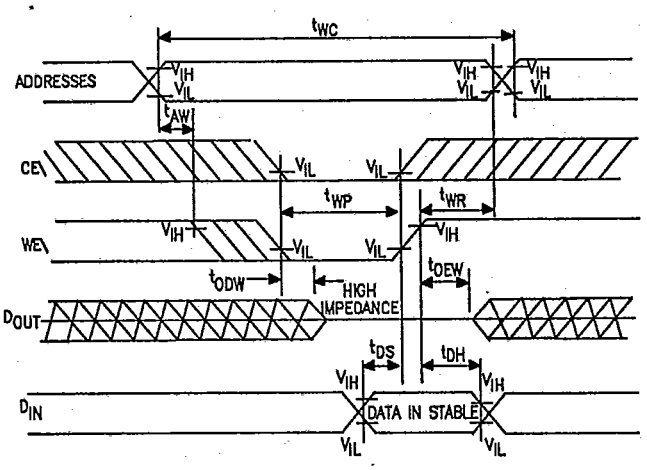
AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0V - 3.0V
Timing Measurement Reference Levels:
Input: 1.5V Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

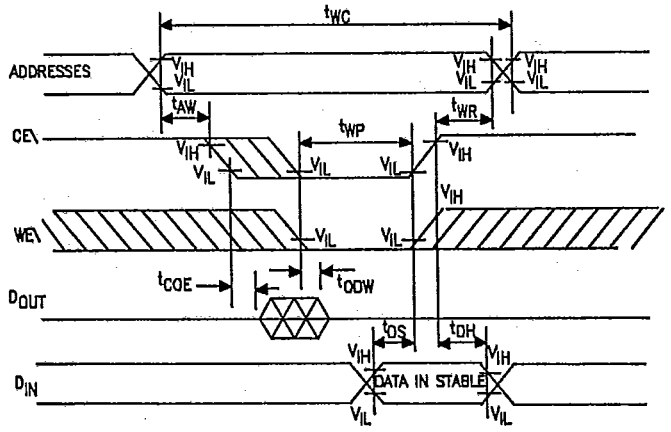
READ CYCLE (1)



WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



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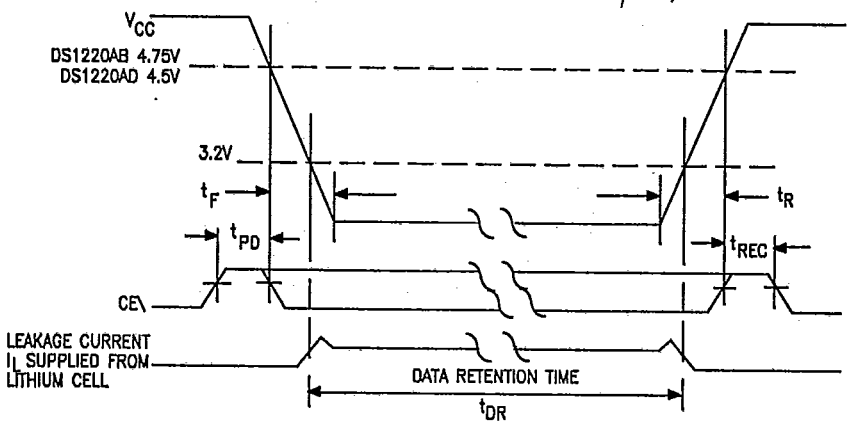
POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		us	10
t_F	V_{CC} Slew from 4.75V to 0V (CE\ at V_{IH})	300		us	DS1220AB
t_F	V_{CC} slew from 4.5V to 0V (CE\ at V_{IH})	300		us	DS1220AD
t_R	V_{CC} Slew from 0V to 4.75V (CE\ at V_{IH})	0		us	DS1220AB
t_R	V_{CC} slew from 0V to 4.5V (CE\ at V_{IH})	0		us	DS1220AD
t_{REC}	CE\ at V_{IH} after Power-Up	2	125	ms	

(t_A=25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in the battery backup mode.

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NOTES:

1. WE\ is high for a Read Cycle.

2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impedance state.

3. t_{WP} is specified as the logical AND of CE\ and WE\. t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.

4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.

5. These parameters are sampled with a 5 pF load and are not 100% tested.

6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.

9. Each DS1220 AB/AD has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.

10. See the DS1210 Nonvolatile Controller Chip data sheet for battery backup operation.