

**PRELIMINARY****CY62148**

512K x 8 Static RAM

Features

- 4.5V–5.5V operation
- CMOS for optimum speed/power
- Low active power
— 660 mW (max.)
- Low standby power (Commercial L version)
— 2.75 mW (max.)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options

Functional Description

The CY62148 is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has

an automatic power-down feature that reduces power consumption by more than 99% when deselected.

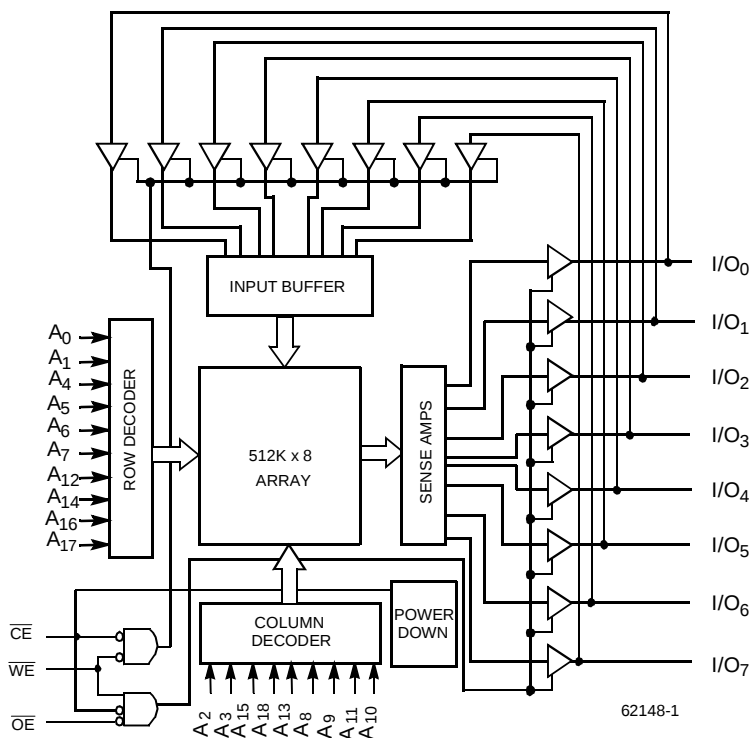
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH for read. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

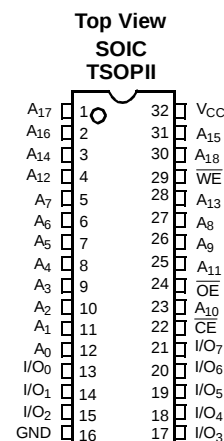
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY62148 is available in a standard 32 pin 450-mil-wide body width SOIC and 32 pin TSOP II packages.

Logic Block Diagram



Pin Configuration



62148-2

Selection Guide

			CY62148-55	CY62148-70	CY62148-100
Maximum Access Time (ns)			55	70	100
Maximum Operating Current (mA)			120	120	120
		L	90	90	90
		LL	90	90	90
Maximum CMOS Standby Current			2 mA	2 mA	2 mA
		L	100 μ A	100 μ A	100 μ A
	Com'l	LL	20 μ A	20 μ A	20 μ A
	Ind'l	LL	40 μ A	40 μ A	40 μ A

Shaded areas contain advance information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to +70°C	4.5V - 5.5V
Industrial	-40°C to +85°C	

Electrical Characteristics Over the Operating Range

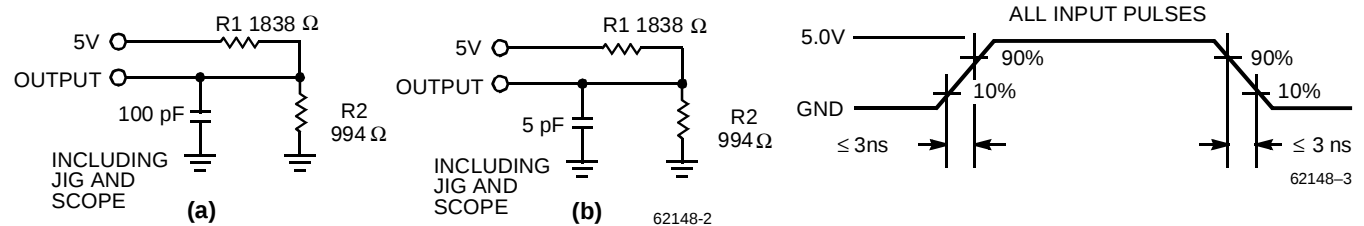
Parameter	Description	Test Conditions	Min.	Typ ^[3]	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -1 \text{ mA}$	2.4			V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 2.1 \text{ mA}$			0.4	V
V_{IH}	Input HIGH Voltage		2.2		$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		-0.3		0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1		+1	μ A
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-1		+1	μ A
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$			120	mA
		L			90	mA
		LL			90	mA
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$			15	mA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V, f = 0$		1.6 μ A	2	mA
		L		1.6	100	μ A
		Com'l LL		1.6	20	μ A
		Ind'l LL		1.6	40	μ A

Notes:

- $V_{IL}(\text{min.}) = -2.0V$ for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- Typical values are measured at $V_{CC} = 5V, T_A = 25^\circ C$, and are included for reference only and are not tested or guaranteed.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$	6	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT
 OUTPUT $\text{---} 645\ \Omega \text{---} 1.75\text{V}$

Switching Characteristics^[6] Over the Operating Range

Parameter	Description	62148-55		62148-70		62148-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	55		70		100		ns
t _{AA}	Address to Data Valid		55		70		100	ns
t _{OHA}	Data Hold from Address Change	10		10		10		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		55		70		100	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		20		35		50	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[8]	5		5		5		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[7, 8]		20		25		30	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[8]	10		10		10		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[7, 8]		20		25		30	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		55		70		100	ns
WRITE CYCLE ^[9]								
t _{WC}	Write Cycle Time	55		70		100		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	45		60		80		ns
t _{AW}	Address Set-Up to Write End	45		60		80		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	45		55		60		ns
t _{SD}	Data Set-Up to Write End	25		25		25		ns

Notes

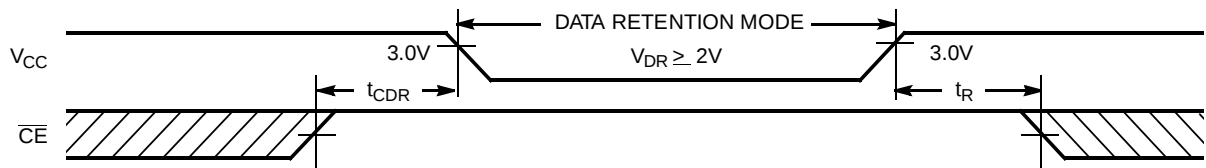
- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 5ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured $\pm 500\text{ mV}$ from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Characteristics^[6] Over the Operating Range (continued)

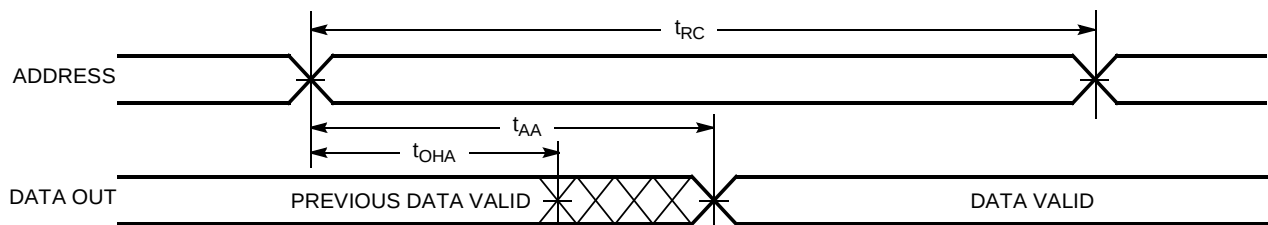
Parameter	Description	62148-55		62148-70		62148-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z ^[8]	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z ^[7,8]		20		25		30	ns

Data Retention Characteristics Over the Operating Range

Parameter	Description		Conditions	Min.	Typ ^[3]	Max	Unit
V_{DR}	V_{CC} for Data Retention			2.0			V
I_{CCDR}	Data Retention Current	Com'l	No input may exceed $V_{CC} + 0.3V$ $V_{CC} = V_{DR} = 3.0V$, $CE \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		1.6 μA	1.7	mA
						80	μA
						20	μA
		Ind'l				40	μA
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time			0			ns
t_R	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform


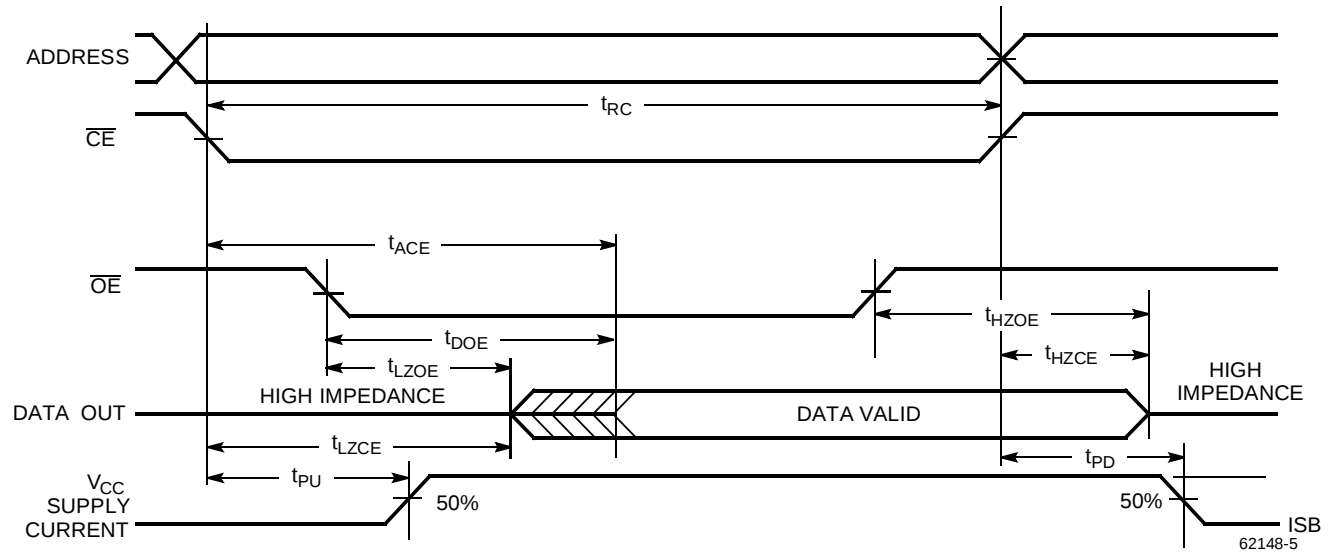
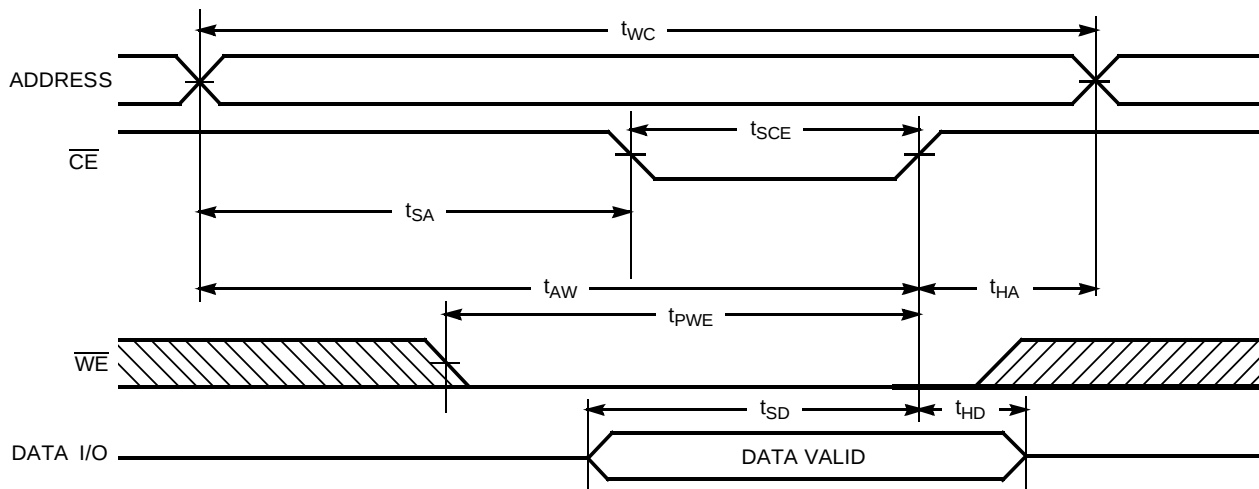
62148-5

Switching Waveforms
Read Cycle No.1^[10,11]


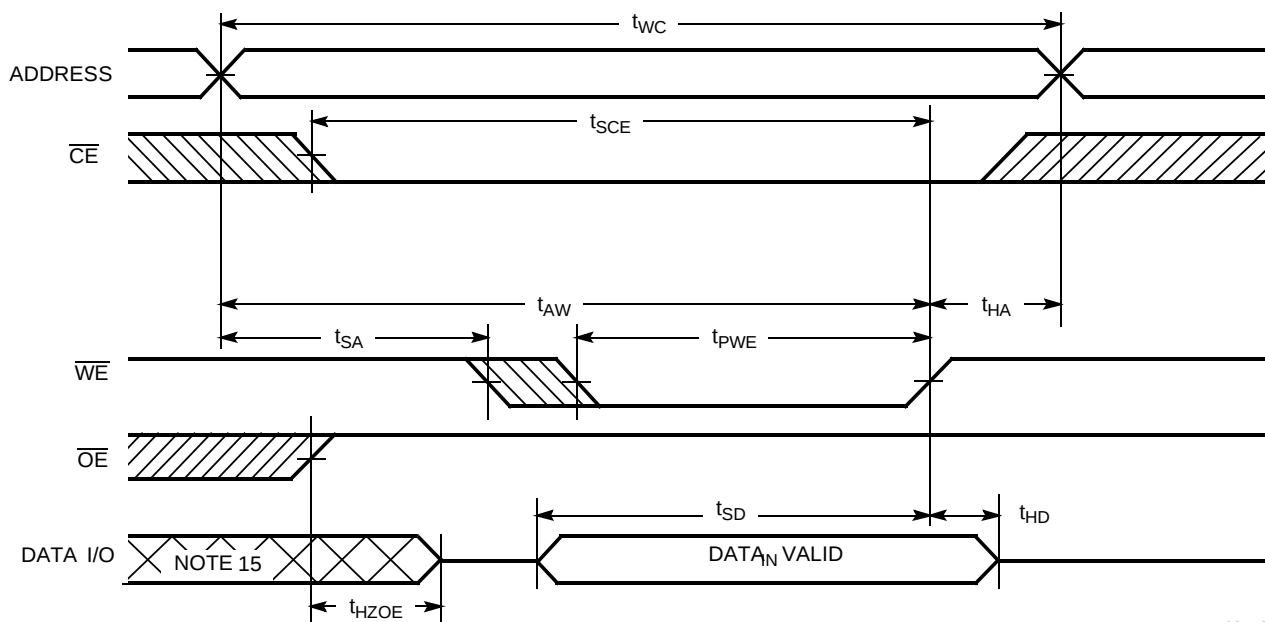
62148-4

Notes:

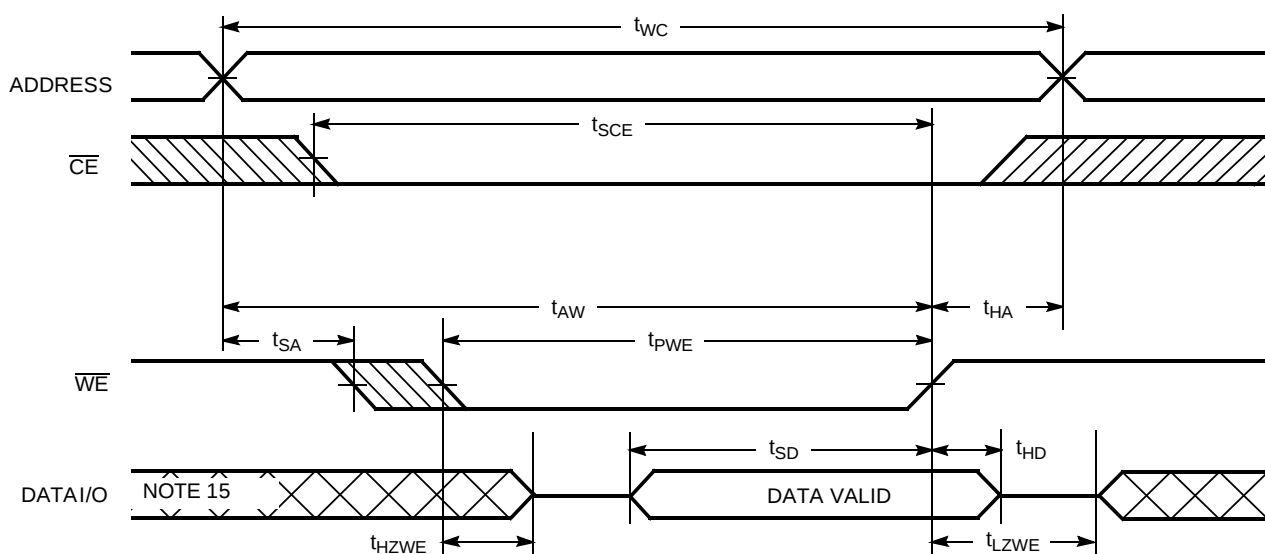
10. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
11. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 ($\overline{OE}$ Controlled)^[11,12]

Write Cycle No. 1 ($\overline{CE}$ Controlled)^[13,14]

Notes:

12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O is high impedance if $OE = V_{IH}$.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)^[13,14]


62148-7

Write Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)^[13,14]


62148-8

Notes:

15. During this period the I/Os are in the output state and input signals should not be applied

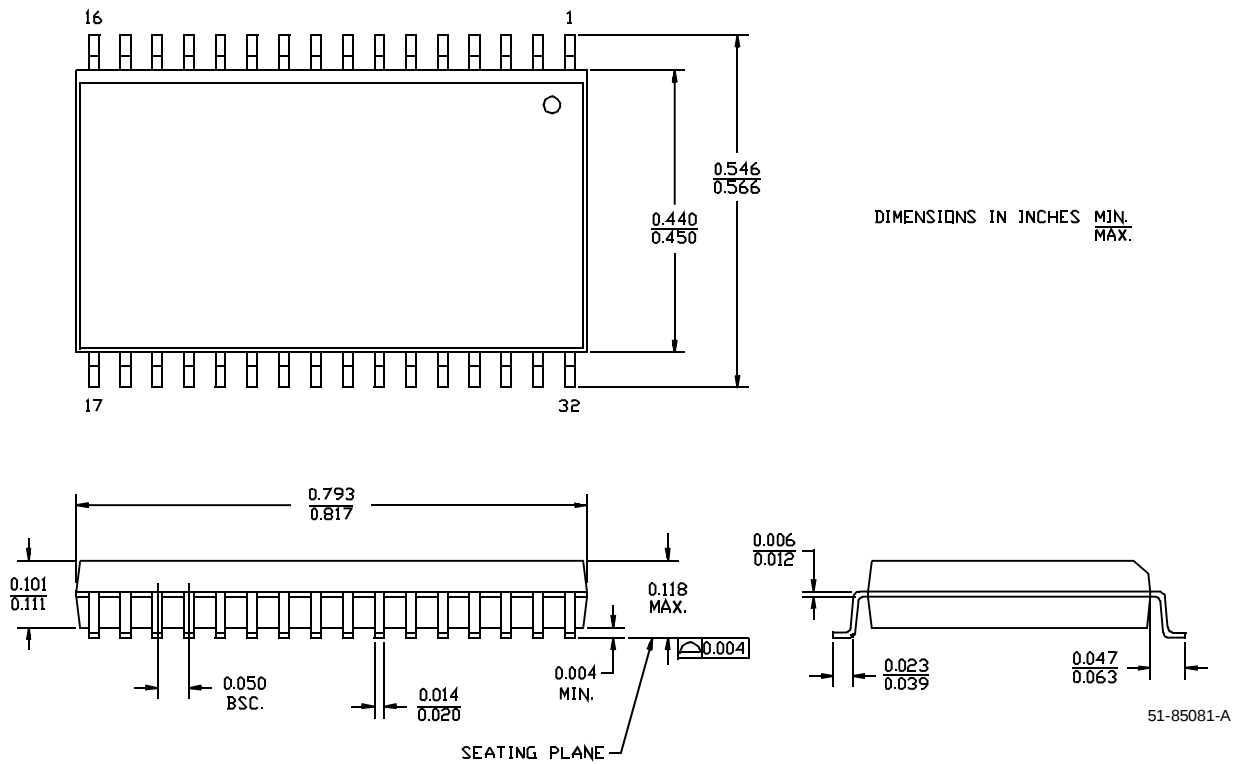
Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O ₀ – I/O ₇	Mode	Power
H	X	X	High Z	Power-Down	Standby (I _{SB})
L	L	H	Data Out	Read	Active (I _{CC})
L	X	L	Data In	Write	Active (I _{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I _{CC})

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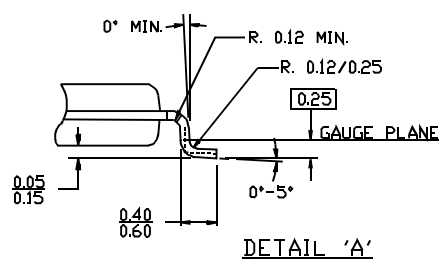
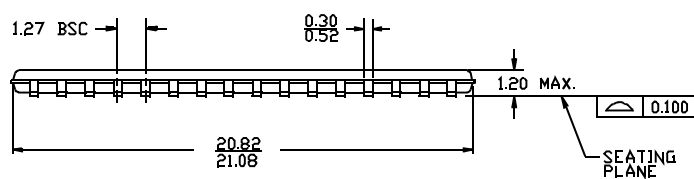
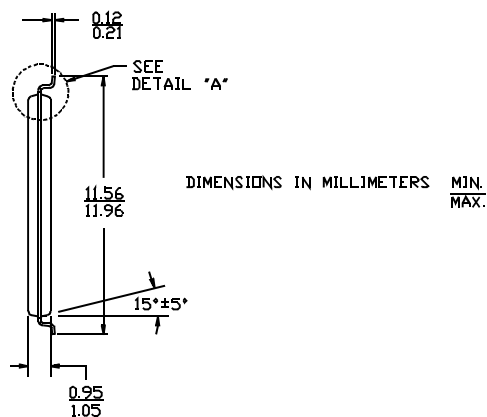
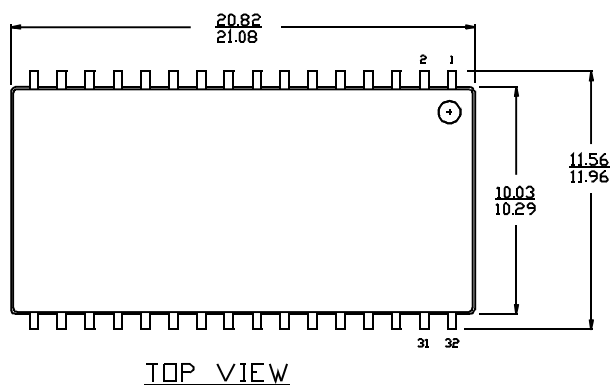
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62148-70SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
	CY62148-70ZSC	ZS32	32-Lead TSOP II	
	CY62148L-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148L-70ZSC	ZS32	32-Lead TSOP II	
	CY62128LL-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148LL-70ZSC	ZS32	32-Lead TSOP II	
	CY62148-70SI	S34	32-Lead (450-Mil) Molded SOIC	Industrial
	CY62148-70ZSI	ZS32	32-Lead TSOP II	
	CY62148L-70SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148L-70ZSI	ZS32	32-Lead TSOP II	
	CY62128LL-70SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148LL-70ZSI	ZS32	32-Lead TSOP II	
100	CY62148-100SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
	CY62148-100ZSC	ZS32	32-Lead TSOP II	
	CY62148L-100SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148L-100ZSC	ZS32	32-Lead TSOP II	
	CY62128LL-100SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148LL-100ZSC	ZS32	32-Lead TSOP II	
	CY62148-100SI	S34	32-Lead (450-Mil) Molded SOIC	Industrial
	CY62148-100ZSI	ZS32	32-Lead TSOP II	
	CY62148L-100SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148L-100ZSI	ZS32	32-Lead TSOP II	
	CY62128LL-100SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148LL-100ZSI	ZS32	32-Lead TSOP II	

Package Diagrams
32-Lead (450-Mil) Molded SOIC S34


Package Diagrams (continued)

32-Lead TSOP II ZS32



51-85095