RHF1201

Rad-hard 12-bit 50 Msps A/D converter

Datasheet - production data

Ceramic SO48 package

The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package.

Features

- Qml-V qualified, smd 5962-05217
- Rad-hard: 300 kRad(Si) TID
- Failure immune (SEFI) and latchup immune (SEL) up to 120 MeV-cm^2/mg at 2.7 V and 125 °C
- Hermetic package
- Wide sampling range
- Tested at 50 Msps
- Optimwatt^{TM} adaptive power: 44 mW at 0.5 Msps and 100 mW at 50 Msps
- Optimized for 2 V_{pp} differential input
- SFDR up to 75 dB at F_S = 50 Msps, F_{in} = 15 MHz
- 2.5 V/3.3 V compatible digital I/O
- Built-in reference voltage with external bias capability

Applications

- Digital communication satellites
- Space data acquisition systems
- Aerospace instrumentation
- Nuclear and high-energy physics

Description

The RHF1201 is a 12-bit, 50 Msps sampling frequency analog-to-digital converter that uses pure CMOS 0.25 µm technology combining high performance and very low power consumption. The device is based on a pipeline structure and digital error correction to provide excellent static linearity. Specifically designed to optimize the speed power consumption ratio, the RHF1201 integrates a proprietary track-and-hold structure making it ideal for IF-sampling applications up to 150 MHz. A voltage reference network is integrated in the circuit to simplify the design and minimize external components. A tri-state capability is available on the outputs to allow common bus sharing. Output data can be coded in two different formats. A data ready signal, raised when the data is valid on the output, can be used for synchronization purposes.

Table 1. Device summary

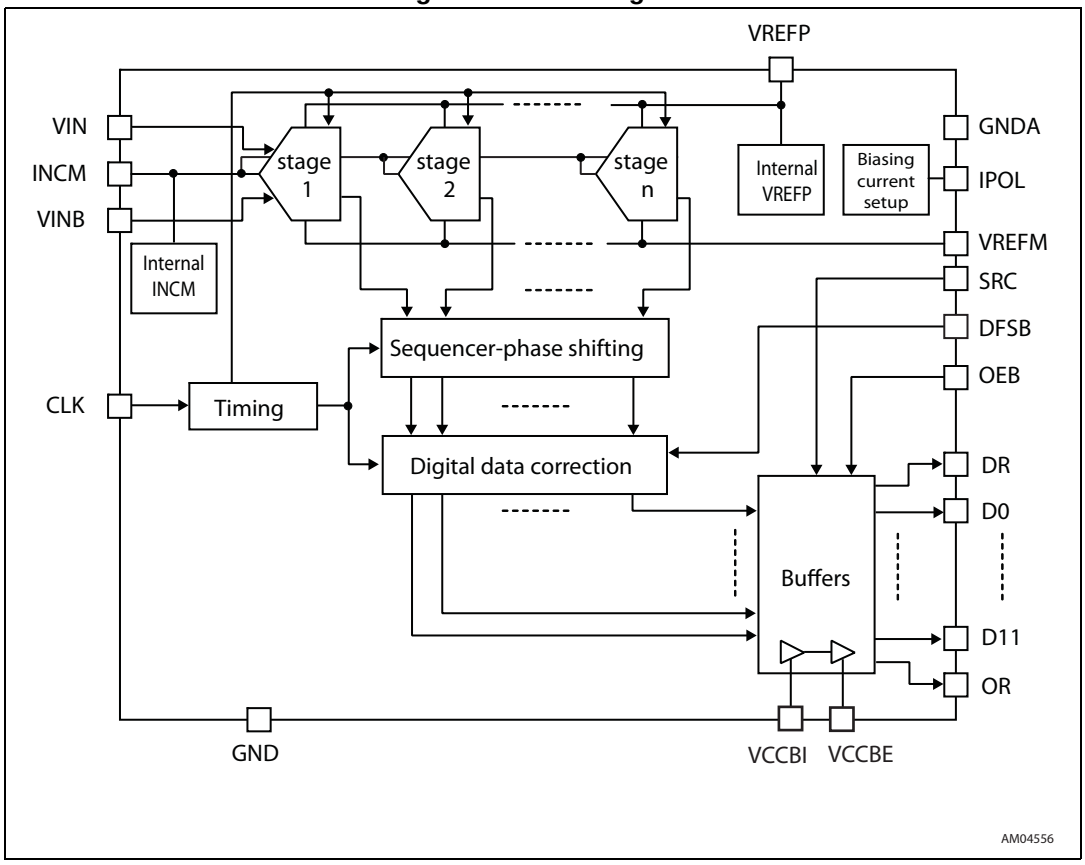
Order code	SMD pin	Quality level	Package	Lead finish	Packing	Marking
RHF1201KSO1	—	Engineering model	SO48	Gold	Strip pack	RHF1201KSO1
RHF1201KSO-01V	5962F0521701VXC	QMLV-flight				5962F0521701VXC

Contents

1 Description

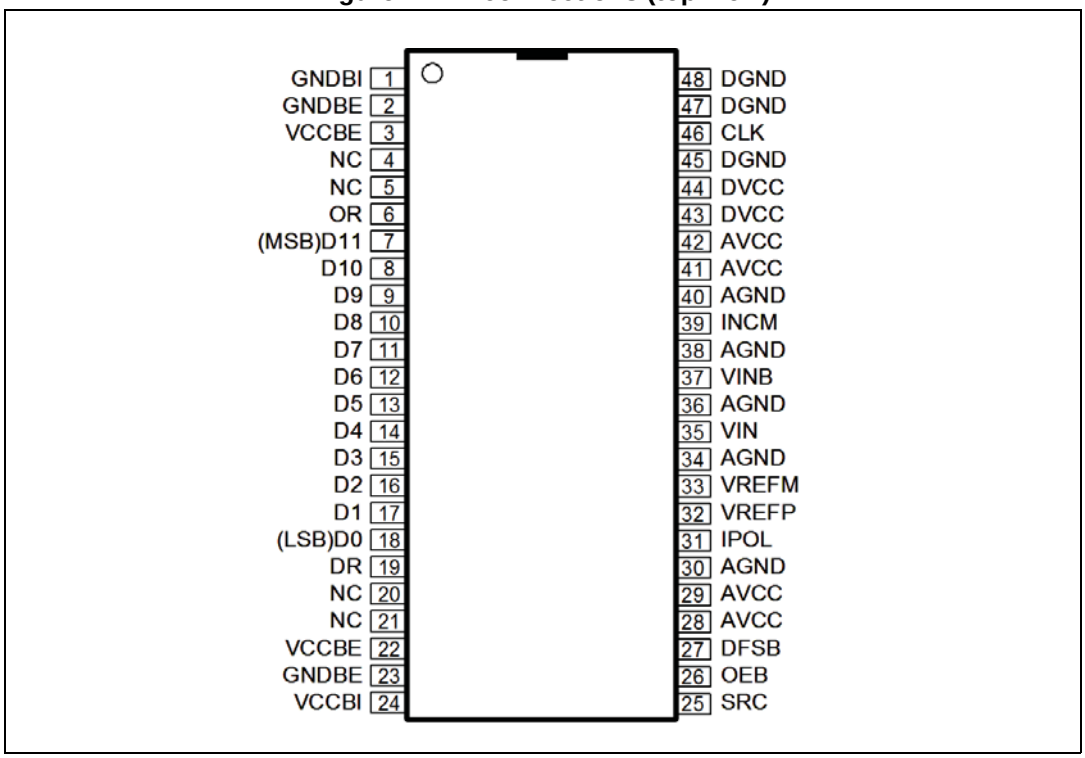
1.1 Block diagram

Figure 1. Block diagram



1.2 Pin connections

Figure 2. Pin connections (top view)



1.3 Pin descriptions

Table 2. Pin descriptions

Pin	Name	Description	Note	Pin	Name	Description	Note
1	GNDBI	Digital buffer ground	0 V	25	SRC	Slew rate control input	2.5 V/3.3 V CMOS input
2	GNDBE	Digital buffer ground	0 V	26	OEB	Output Enable input	2.5 V/3.3 V CMOS input
3	VCCBE	Digital buffer power supply	2.5 V/3.3 V	27	DFSB	Data Format Select input	2.5 V/3.3 V CMOS input
4		NC	Not connected to the dice	28	AVCC	Analog power supply	2.5 V
5		NC	Not connected to the dice	29	AVCC	Analog power supply	2.5 V
6	OR	Out-of-range output	CMOS output (2.5 V/3.3 V)	30	AGND	Analog ground	0 V
7	D11(MSB)	Most significant bit output	CMOS output (2.5 V/3.3 V)	31	IPOL	Analog bias current input	
8	D10	Digital output	CMOS output (2.5 V/3.3 V)	32	VREFP	Top voltage reference	Can be internal or external
9	D9	Digital output	CMOS output (2.5 V/3.3 V)	33	VREFM	Bottom voltage reference	External
10	D8	Digital output	CMOS output (2.5 V/3.3 V)	34	AGND	Analog ground	0 V
11	D7	Digital output	CMOS output (2.5 V/3.3 V)	35	VIN	Analog input	Optimized for $1V_{pp}$
12	D6	Digital output	CMOS output (2.5 V/3.3 V)	36	AGND	Analog ground	0 V
13	D5	Digital output	CMOS output (2.5 V/3.3 V)	37	VINB	Inverted analog input	Optimized for $1V_{pp}$
14	D4	Digital output	CMOS output (2.5 V/3.3 V)	38	AGND	Analog ground	0 V
15	D3	Digital output	CMOS output (2.5 V/3.3 V)	39	INCM	Input common mode	Can be internal or external
16	D2	Digital output	CMOS output (2.5 V/3.3 V)	40	AGND	Analog ground	0 V
17	D1	Digital output	CMOS output (2.5 V/3.3 V)	41	AVCC	Analog power supply	2.5 V
18	D0(LSB)	Least significant bit output	CMOS output (2.5 V/3.3 V)	42	AVCC	Analog power supply	2.5 V
19	DR	Data ready output	CMOS output (2.5 V/3.3 V)	43	DVCC	Digital power supply	2.5 V
20		NC	Not connected to the dice	44	DVCC	Digital power supply	2.5 V
21		NC	Not connected to the dice	45	DGND	Digital ground	0 V
22	VCCBE	Digital buffer power supply	2.5 V/3.3 V	46	CLK	Clock input	2.5 V compatible CMOS input
23	GNDBE	Digital buffer ground	0 V	47	DGND	Digital ground	0 V
24	VCCBI	Digital buffer power supply	2.5 V	48	DGND	Digital ground	0 V

1.4 Equivalent circuits

Figure 3. Analog inputs

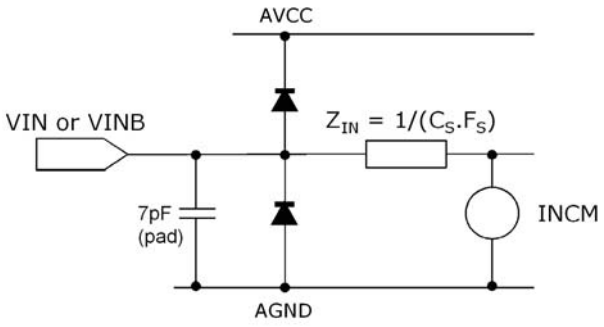


Figure 4. Output buffers

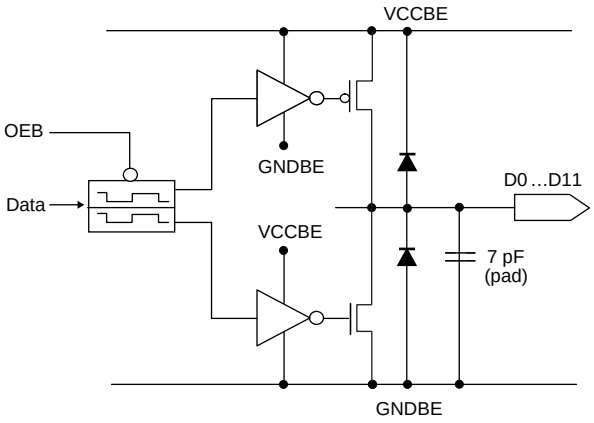


Figure 5. Clock input

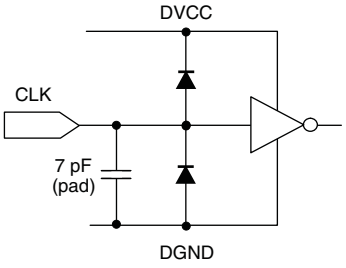


Figure 6. Data format input

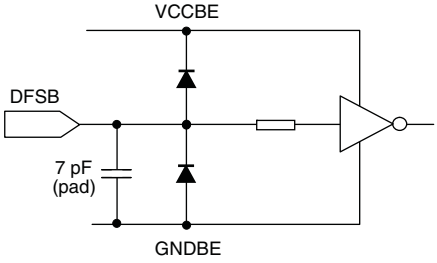


Figure 7. Slew rate control input

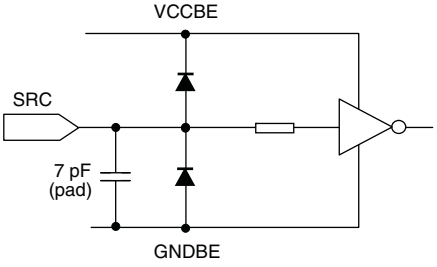


Figure 8. Output enable input

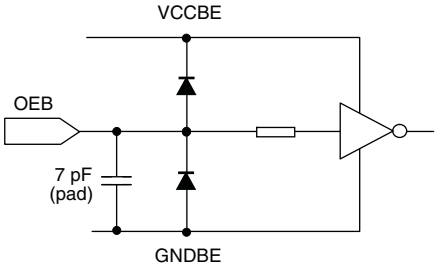


Figure 9. VREFP and INCM input

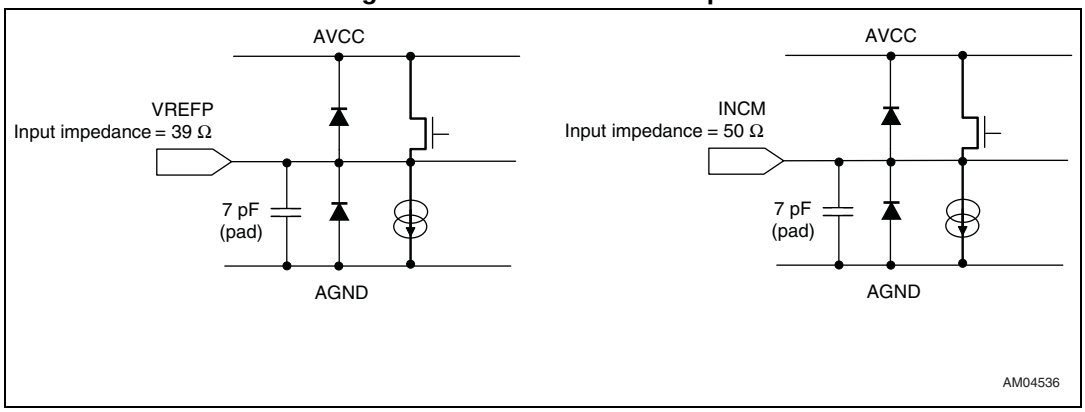
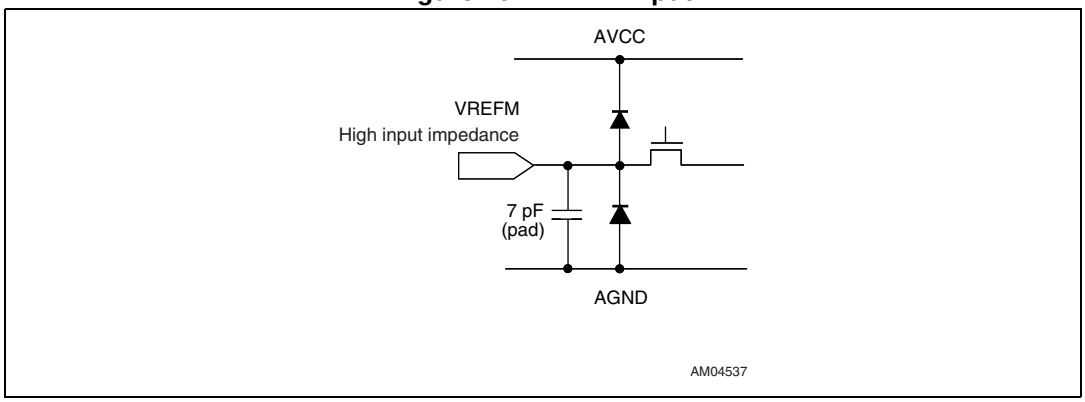


Figure 10. VREFM input



2 Absolute maximum ratings and operating conditions

Table 3. Absolute maximum ratings

Symbol	Parameter	Values	Unit
AV_{CC}	Analog supply voltage	3.3	V
DV_{CC}	Digital supply voltage		
V_{CCBI}	Digital buffer supply voltage		
V_{CCBE}	Digital buffer supply voltage	3.6	
V_{IN} V_{INB}	Analog inputs: bottom limit -> top limit	-0.6 V -> AV_{CC}+0.6 V	
V_{REFP} V_{INCM}	External references: bottom limit -> top limit	-0.6 V -> AV_{CC}+0.6 V	
I_{Dout}	Digital output current	-100 to 100	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thjc}	Thermal resistance junction to case	22	°C/W
R_{thja}	Thermal resistance junction to ambient	125	
ESD	HBM (human body model) (1)	2	kV

1. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 ΩW resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

Table 4. Operating conditions (1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
AV_{CC}	Analog supply voltage	2.3	2.5	2.7	V
DV_{CC}	Digital supply voltage	2.3	2.5	2.7	V
V_{CCBI}	Digital internal buffer supply	2.3	2.5	2.7	V
V_{CCBE}	Digital output buffer supply	2.3	2.5	3.4	V
V_{REFP}	Top external reference voltage	0.5		1.4	V
V_{REFM}	Bottom external reference voltage	0		0.5	V
V_{INCM}	Forced common mode voltage	0.2		1.1	V
V_{IN} & V_{INB}	Maximum input voltage versus GND		1	1.6	V
	Minimum input voltage versus GND	-0.2	0		V
V_{REFP} - V_{REFM}	Difference between reference voltage	0.3			V
DFSB	Digital inputs (2)	GND		V_{CCBE}	V
SRC		GND		V_{CCBE}	V
OEB		GND		V_{CCBE}	V

1. Please note that driving externally Vrefp and INCM inputs induces some constraints. Refer to *Chapter 5.5.2: External voltage reference* for more information.
2. See *Table 9* for thresholds.

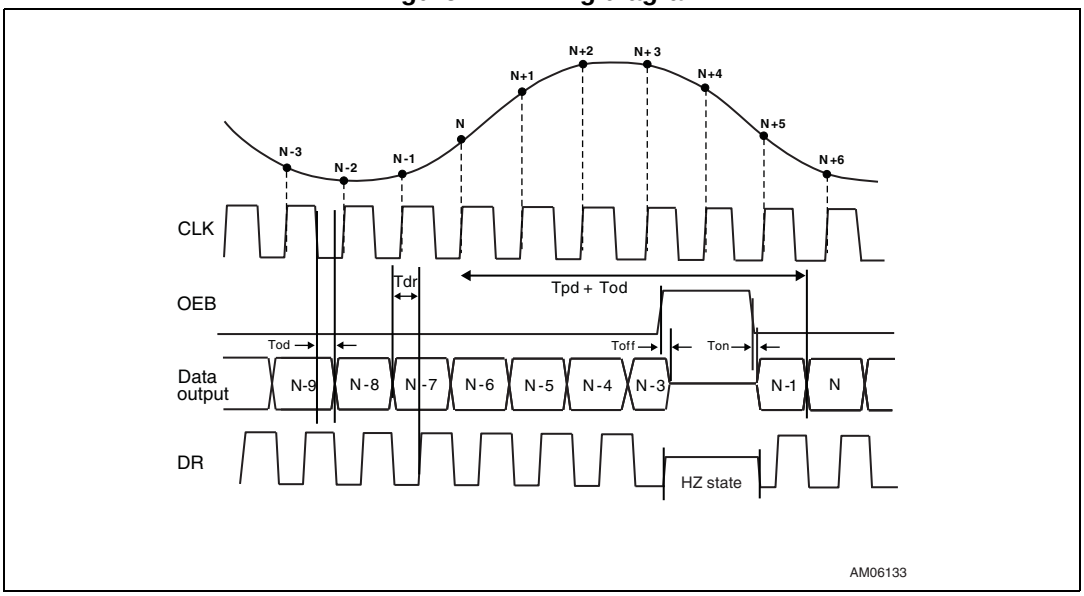
3 Timing characteristics

Table 5. Timing table

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC	Clock duty cycle	F_S = 45 Msps	45	50	65	%
T_{od}	Data output delay (1) (fall of clock to data valid)	10 pF load	4	5	6	ns
T_{pd}	Data pipeline delay (1)			5.5		cycles
T_{dr}	Data ready rising edge delay after data change (2)	Duty cycle = 50%		0.5		
T_{on}	Falling edge of OEB to digital output valid data			1	3	ns
T_{off}	Rising edge of OEB to digital output tri-state			1	3	
T_{rD}	Data rising time	5 pF load, SRC = 0		2.8		
		5 pF load, SRC = 1		5.7		
T_{fD}	Data falling time	5 pF load, SRC = 0		2		
		5 pF load, SRC = 1		4.3		

1. Guaranteed by design.
2. T_{dr} is linked to the duty cycle, conditioned by the duration of the low level of DR signal.

Figure 11. Timing diagram



The input signal is sampled on the rising edge of the clock while the digital outputs are synchronized on the falling edge of the clock. The duty cycles on DR and CLK are the same. The rising and falling edges of the OR pin are synchronized with the falling edge of the DR pin.

4 Electrical characteristics (unchanged after 300 kRad)

Unless otherwise specified, the test conditions in the following tables are:
AV_{CC} = DV_{CC} = V_{CCBI} = V_{CCBE} = 2.5 V, F_S = 50 Msps, differential input configuration, F_{in} = 15 MHz, V_{REFP} = internal, V_{REFM} = 0 V, T_{amb} = 25 °C.

Table 6. Analog inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}-V_{INB}	Full-scale input differential voltage (1) (FS) (2)			2		V_{p-p}
C_{in}	Input capacitance		—	7.0	—	pF
Z_{in}	Input impedance vs. INCM (3)	Fs = 13Msps		64		kΩ
ERB	Effective resolution bandwidth (1)			95		MHz

1. See *Section 6: Definitions of specified parameters* for more information.
2. Optimized differential input: 2 Vp-p.
3. Zin = 1/(Fs x C) with C=1.2 pF.

Table 7. Internal reference voltage (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{REFP}	Top internal reference voltage (2)	AV_{CC} =2.5 V	0.79	0.95	1.16	V
V_{INCM}	Input common mode voltage (2)		0.40	0.52	0.67	
R_{out}	Output resistance of internal reference	V_{REFP}		39		Ω
		V_{INCM}		50		Ω
TempCo	Temperature coefficient of V_{REFP} (2)	T_{min} < T_{amb} < T_{max}		0.12		mV/°C
	Temperature coefficient of INCM (2)					

1. Refer to *Section 5.2: Driving the analog input: how to correctly bias the RHF1201* for correct biasing of RHF1201
2. Not fully tested over the temperature range. Guaranteed by sampling.

Table 8. Static accuracy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OE	Offset error	Fs = 5 Msps		+/-50		LSB
GE	Gain error	Fs = 5 Msps		+/-0.3		%
DNL	Differential non-linearity (1)	F_{in} = 2 MHz, V_{IN} = 1Vp-p F_s = 50 Msps		+/-0.5		LSB
INL	Integral non-linearity (1)	F_{in} = 2 MHz, V_{IN} = 1Vp-p F_s = 50 Msps		+/-1.7		
	Monotonicity and no missing codes		Guaranteed			

1. See *Section 6* for more information.

Table 9. Digital inputs and outputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Clock input						
CT	Clock threshold	DV_{CC} = 2.5 V		1.25		V
CA	Clock amplitude (DC component = 1.25 V)	Square clock DV_{CC} = 2.5 V	0.8		2.5	Vp-p
Digital inputs						
V_{IL}	Logic "0" voltage			0	0.25 x V_{CCBE}	V
V_{IH}	Logic "1" voltage		0.75 x V_{CCBE}	V_{CCBE}		
Digital outputs						
V_{OL}	Logic "0" voltage	I_{OL} = -10 µA		0	0.2	V
V_{OH}	Logic "1" voltage	I_{OH} = +10 µA	V_{CCBE} - 0.2 V			
I_{OZ}	High impedance leakage current	OEB set to V_{IH}	-15		15	µA

Table 10. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SFDR	Spurious free dynamic range	F_{in} = 15 MHz		-75	-63	dBc
		F_{in} = 95 MHz		-70		
		F_{in} = 145 MHz		-57		
SNR	Signal to noise ratio	F_{in} = 15 MHz	59	63		dB
		F_{in} = 95 MHz		60		
		F_{in} = 145 MHz		59		
THD	Total harmonics distortion	F_{in} = 15 MHz		-76	-64	
		F_{in} = 95 MHz		-72		
		F_{in} = 145 MHz		-58		
SINAD	Signal to noise and distortion ratio	F_{in} = 15 MHz	58	63		
		F_{in} = 95 MHz		60		
		F_{in} = 145 MHz		56.5		
ENOB	Effective number of bits	F_{in} = 15 MHz	9.7	10.3		bits
		F_{in} = 95 MHz		9.5		
		F_{in} = 145 MHz		9.1		
PSRR	Power supply rejection ratio	F = 260 kHz Fs = 2 MHz R_{pol} = 200 k Ω each power supply at 2.5 V decoupled by 10 µF//470 nF		93		dB

5 User manual

5.1 Power consumption optimization

The polarization current in the input stage is set by an external resistor (R_{pol}). When selecting the resistor value, it is possible to optimize the power consumption according to the sampling frequency of the application. For this purpose, an external R_{pol} resistor is placed between the IPOL pin and the analog ground.

The values in *Figure 12* are achieved with VREFP = 1 V, VREFM = 0 V, INCM = 0.5 V and the input signal is 2 Vpp with a differential DC connection. If the conditions are changed, the R_{pol} resistor varies slightly but remains in the domain described in *Figure 12*.

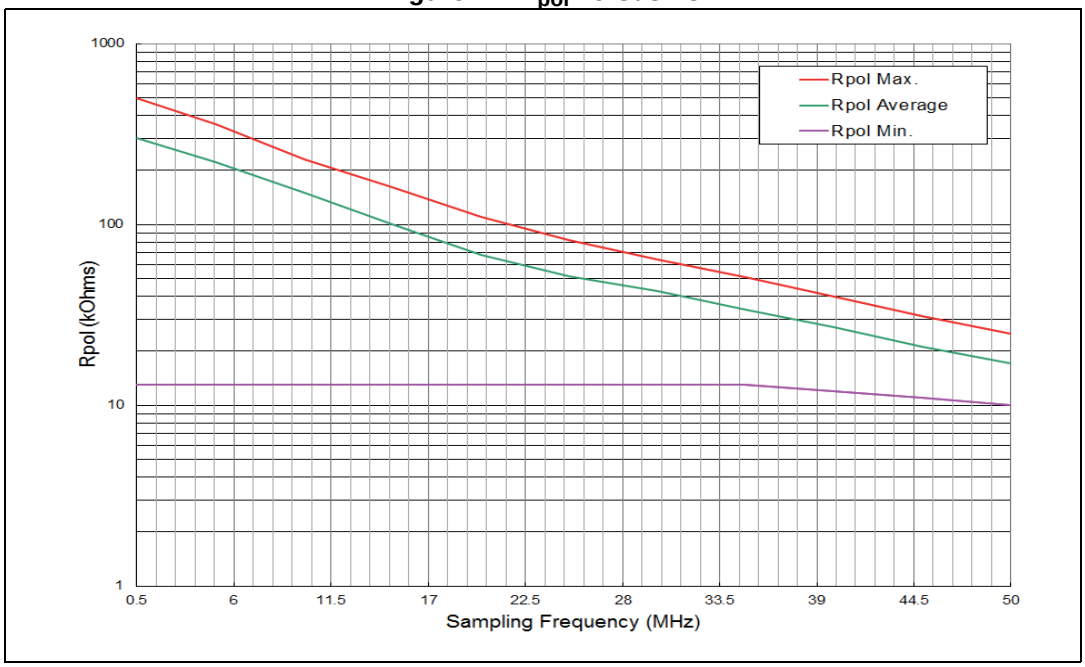
Figure 12 shows the optimum R_{pol} resistor value to obtain the best ENOB value. It also shows the minimum and maximum values to get good results. ENOB decreases by approximately 0.2 dB when you change R_{pol} from optimum to maximum or minimum.

If R_{pol} is higher than the maximum value, there is not enough polarization current in the analog stage to obtain good results. If R_{pol} is below the minimum, THD increases significantly.

Therefore, the total dissipation can be adjusted across the entire sampling range to fulfill the requirements of applications where power saving is critical.

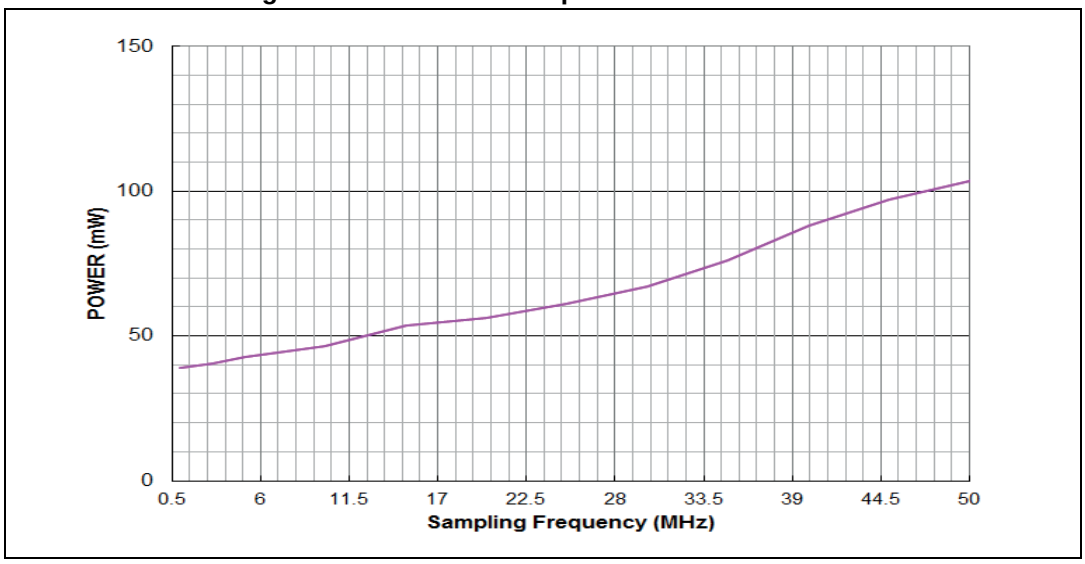
For sampling frequencies below 2 MHz, the optimum resistor value is approximately 200 kOhms.

Figure 12. R_{pol} versus Fs



The power consumption depends on the R_{pol} value and the sampling frequency. R_{pol} is defined in *Figure 13* as the optimum.

Figure 13. Power consumption values versus Fs



5.2 Driving the analog input: how to correctly bias the RHF1201

It is mandatory to follow some simple biasing rules to reach optimal performance when driving the RHF1201.

DC biasing and the AC swing must be considered in order to keep the analog input in the correct range. Let's define some parameters:

Definition 1: The common mode of the input signal is:

$$CMinput = \frac{(Vin + Vinb)}{2}$$

Definition 2 : the common mode of the reference voltage is:

$$CMref = \frac{(Vrefp + Vrefm)}{2}$$

To have correct biasing of RHF1201, **this condition must be respected at all times**:

$$CMinput \leq CMref + 0.2V$$

Please note that the INCM value is not a parameter from previous equations. INCM is an input/output that's used to bias internal OTA amplifiers. So INCM can be any value from *Table 4*.

However, if the INCM value is used to bias analog inputs (Vin and Vinb), Cminput becomes dependent on INCM. In this case, the setting of INCM must be chosen to respect the equation:

$$CMinput \leq CMref + 0.2V$$

Now let's see what happens when the RHF1201 is driven in differential mode and single-ended mode. We will use a sinusoidal input signal for ease of computation, but the results presented after can be easily extrapolated to another kind of signal shape.

5.2.1 Differential mode biasing

In differential mode we have

- Vin = Vbias + A sin(ωt) and Vinb = Vbias – A sin(ωt) with A = peak of input signal.
- Vbias can be provided by the source signal or by INCM which is the DC biasing of the sinusoidal input signal.

As by definition, AC components are in opposite phase for Vin and Vinb, at any time on the signal we have CMinput = Vbias.
In differential mode, to keep a safe operation of the RHF1201 analog inputs, we have to respect :

$$Vbias \leq CMref + 0.2V$$

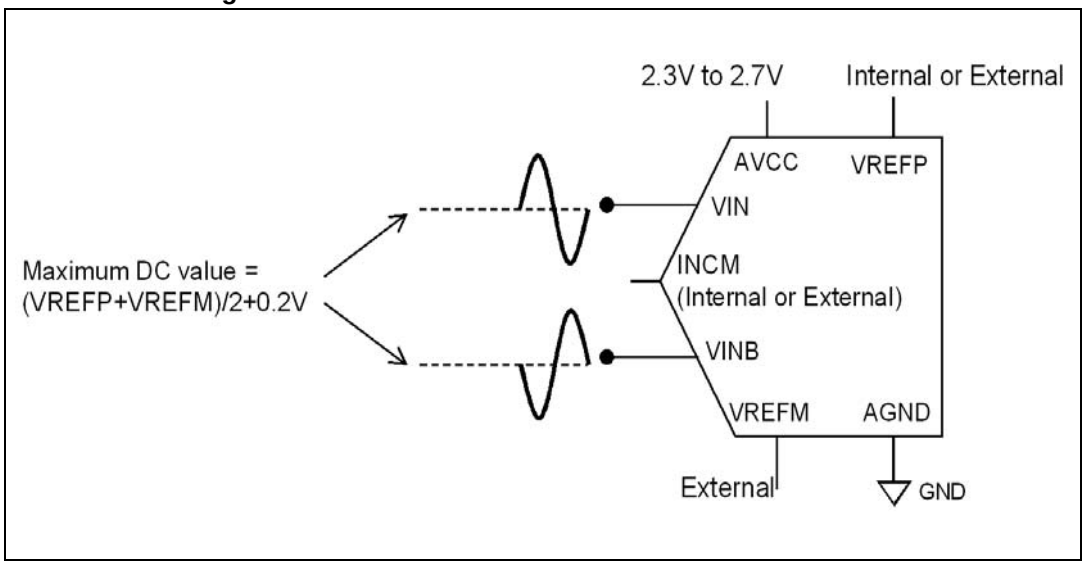
and referring to *Table 4* for the maximum input signal allowed we have:

$$A + Vbias \leq 1.6V$$

and

$$Vbias - A \geq -0.2V$$

Figure 14. RHF1201 in recommended differential mode



5.2.2 Single-ended mode biasing

In single-ended mode, the biasing consideration is different because, as we will see, CMinput is no longer constant but dependent on the amplitude of the input signal. This dependency limits considerably the possibilities of single-ended use.

Please note also that in the demonstration below, Vin is variable and Vinb is fixed, but the opposite is possible simply by exchanging Vin and Vinb in the equations.

Let us take a typical situation with:

- Vin = Vbias + A sin(ω t) and Vinb = Vbias with A = peak of input signal
- Vbias can be provided by the source signal or by INCM which is the DC biasing of sinusoidal input signal

In this case,

$$CMinput = \frac{(A \times \sin\omega t)}{2} + Vbias$$

and CMinput is totally dependent on the amplitude of the input signal.

In addition, as the following relationship is still true:

$$CMinput \leq CMref + 0.2V$$

we now have:

$$\frac{(A \times \sin\omega t)}{2} + Vbias \leq CMref + 0.2V$$

and of course, referring to *Table 4* for maximum input signal allowed we have:

$$A + Vbias \leq 1.6V$$

and

$$Vbias - A \geq -0.2V$$

So, depending on the settings of Vrefp, Vrefm, the following condition

$$\frac{(A \times \sin\omega t)}{2} + Vbias \leq CMref + 0.2V$$

can occur very soon before reaching the full-scale input of RHF1201.

Example: you have an input sig nal in single-ended that maximizes the full swing authorized for RHF1201 input -0.2 V to 1.6V which gives 1.8 Vpp in single-ended. The biasing settings are as follows:

As the full scale of ADC is defined by (Vrefp – Vrefm)x2, if Vrefm = 0 V we have 2xVrefp =1.8 V, then Vrefp = 0.9 V.

Vbias = 1.6 V – 1.8V/2 = 0.7 V, then Vin = 0.7 V + (1.8V/2)xsin(ω t) = 0.7 V + 0.9Vxsin(ω t), then A = 0.9V

Vinb = Vbias Vin= 0.7 V

With these settings, we can calculate CMref + 0.2 V = 0.65 V and CMinput = 0.7 V + (0.9Vxsin(ω t))/2. Then, CMinput is maximum when sin(ωt)=1 that gives CMinputmax.= 1.15 V which is far beyond the limit of 0.65 Vpreviously calculated. The range of Vin allowed is -0.2 V to 0.65 V that is even below the half scale requested initially.

A solution to this problem would be to increase the CMref value which is done by increasing Vrefm and Vrefp.

Let us take Vrefm = 0.5 V and calculate Vrefp to have CMref + 0.2 V = 1.15 V.

The solution is Vrefp = 1.4 V that is the maximum allowed in *Table 4*.

Of course, this solution is suitable but, if you want to have some margin tolerance to detect a clipping input, you have to change some parameters.

So, the only way is to reduce the input swing in accordance with the maximum Vrefp and Vrefm allowed in *Table 4*.

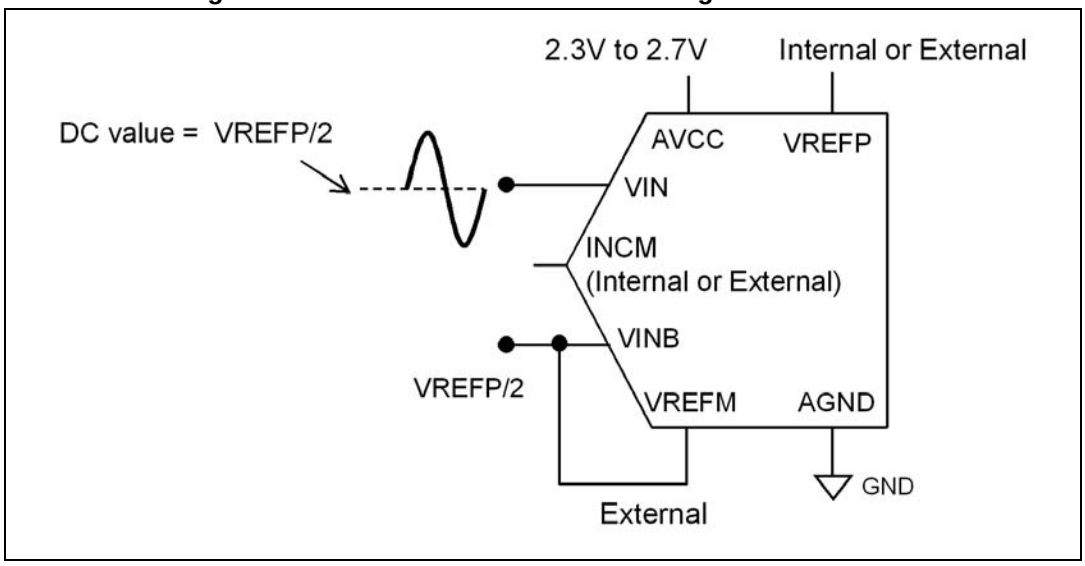
With Vrefp = 1.3 V, Vrefm = 0.5 V, CMref + 0.2 V = 1.1V . CMinput maximum = 1.1V that gives Vbias = 1.1 V - A/2. With A = 0.8 V, Vbias = 0.7 V => Vinpp = 1.6 V, A + Vbias = 1.5 V, Vbias - A = -0.1 V. By reducing the input amplitude by 200 mVpp, we are able to find a solution that fits the limits given in*Table 4* plus a possible clipping detection.

With this example, we can see that the main limitation in single-ended mode on the condition to maximize the full digital swing (0 to 2^{12}), will come from the CMinput maximum vs. Vrefp and Vrefm allowed.

We can see also with the previous example, to fit the large full swing requested, you need three different biasing values (Vrefp, Vrefm, Vbias = INCM) or four if the Vbias value is not compatible with the INCM range allowed.

More generally, if the number of different biasing values is a problem, it's possible to work in single-ended with two different biasing values. By setting INCM = Vrefm = Vbias = Vinb = Vrefp/2, you can have a "simple" single-ended as represented in *Figure 15*.

Figure 15. RHF1201 in recommended single-ended mode



However, we can calculate that the main limitation will come from Vrefm maximum value = 0.5 V

Let us take Vrefm = INCM = Vbias = Vinb =0.5 V and Vrefp = 1 V => the input swing allowed on Vin is 1Vpp centered at 0.5 V => A = 0.5 V

Here, CMref = 0.75 V and CMinput maximum = 0.75 V. So for an input voltage Vin from 0 V to 1 V, the output code will vary from 0 to 2^{12}.

Now, let's see how much the maximum input amplitude Vin can be in order to go in saturation mode (bit OR set to 1).

As CMref + 0.2 V = 0.95 V, the theoretical input voltage Vin allowed can be: Vin = 0.5 V + 0.9V sin(ω t).

Here, CMinput maximum = 0.95 V but A + Vbias = 1.4 V and Vbias - A = -0.4 V. The -0.4 V is a problem because only -0.2 V is allowed. Finally, the practical input voltage Vin is: Vin = 0.5 V + 0.7 V sin(ωt) => CMinput maximum = 0.85 V, A + Vbias = 1.2 V and Vbias - A = -0.2V.

Particular case where Vrefm = 0 V and cannot be changed

In some applications, a dual mode can be requested: differential mode and single-ended mode with a preference for differential mode first.

Let us take a typical example for differential mode:

Vrefp = 1 V, Vrefm = 0 V, Vbias = INCM = 0.5 V. This safe configuration gives a full scale at 2 Vpp (1 Vpp on each input with Vbias = 0.5 V and A = 0.5 V). Here you can use all digital output codes from 0 to 2^{12}.

Now let's go to single-ended mode by keeping: Vrefp = 1 V, Vrefm = 0 V, Vbias = INCM = Vinb = 0.5 V. What would be the maximum swing allowed on Vin and what would be the resulting code? So:

Full scale = 2 x (Vrefp - Vrefm) = 2 V

CMref = 0.5 V and CMref + 0.2V = 0.7 V

By definition, the limitation on the lower side is -0.2 V.

The limitation of Vin on the upper side is given by this equation:

$$\frac{(Vinmax + Vbias)}{2} \leq 0.7V$$

So Vinmax = 0.9 V.

Finally

$$-0.2V \leq Vin \leq 0.9V$$

that gives:

$$1433 \leq \text{Output Code (decimal)} \leq 2867$$

Here the full scale is not usable but is a limited range only.

5.2.3 INCM biasing

As previously discussed, INCM is an input/output that's used to bias the internal OTA amplifiers of RHF1201. So INCM can be any value from *Table 4*.

However, depending on the INCM value, the performance can change slightly. For RHF1201 and for INCM from 0.4 V to 1V, no impact on performance can be observed.

For INCM from 0.2V to 0.4V and 1V to 1.1V, it's possible to have, under boundary conditions, a typical loss of one bit of ENOB. So, if you have the choice, keep the value of INCM value in the range 0.4 V to 1 V.

Please note also that driving externally INCM input induces some constraints. Please refer to *Section 5.2.2: Single-ended mode biasing* for more information.

5.3 Output code vs. analog input and mode usage

Whatever the configuration chosen (differential or single-ended), the two following equations are always true for RHF1201:

- The full scale of analog input is defined by: Full scale = 2 x (Vrefp - Vrefm)
- The output code is defined also as: Output code = f(Vin - Vinb) vs. full scale

Finally we got for DFSB = 1:

$$\text{Output code (12 bits)} = \frac{FFF \times (Vin - VinB)}{2 \times (Vrefp - Vrefm)} + 7FF$$

and for DFSB = 0:

$$\text{Output code (12 bits)} = \frac{FFF \times (Vin - VinB)}{2 \times (Vrefp - Vrefm)} + 7FF + 800$$

5.3.1 Differential mode output code

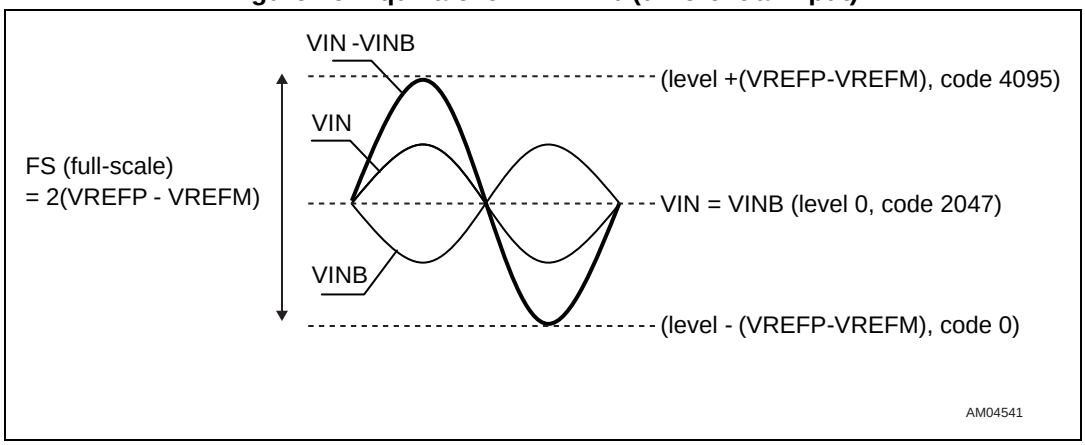
In this mode, the DC component of Vin and Vinb is naturally subtracted. We get the following table:

Table 11. Differential mode output codes

Vin - Vinb =	DFSB = 1	DFSB = 0
+ (VREFP-VREFM)	FFF	7FF
0	7FF	FFF
- (VREFP-VREFM)	000	800

Figure 16 shows the code behavior for DFSB = 1.

Figure 16. Equivalent Vin - Vinb (differential input)



5.3.2 Single-ended mode output code

In single ended mode, Vin or Vinb is constant and equal to Vbias.

If Vin = Vbias + A sin(ωt) and Vinb = Vbias with A = peak of input signal, then (Vin - Vinb) = A sin(ωt) and A = (Vrefp - Vrefm) for maximum swing on input.

Table 12. Single-ended mode output codes with Vinb = Vbias and A = (Vrefp - Vrefm)

Vin =	DFSB = 1	DFSB = 0
Vbias + (VREFP-VREFM)	FFF	7FF
Vbias	7FF	FFF
Vbias - (VREFP-VREFM)	000	800

5.4 Design examples

The RHF1201 is designed to obtain optimum performance when driven on differential inputs with a differential amplitude of two volts peak-to-peak (2 V_{pp}). This is the result of 1 V_{pp} on the Vin and Vinb inputs in phase opposition (*Figure 17*).

For all input frequencies, it is mandatory to add a capacitor on the PCB (between Vin and Vinb) to cut the HF noise. The lower the frequency, the higher the capacitor.

The RHF1201 is specifically designed to meet sampling requirements for intermediate frequency (IF) input signals. In particular, the track-and-hold in the first stage of the pipeline is designed to minimize the linearity limitations as the analog frequency increases.

Differential mode

Figure 17 shows an example of how to drive RHF1201 in differential and DC coupled.

Figure 17. Example 2 V_{pp} differential input

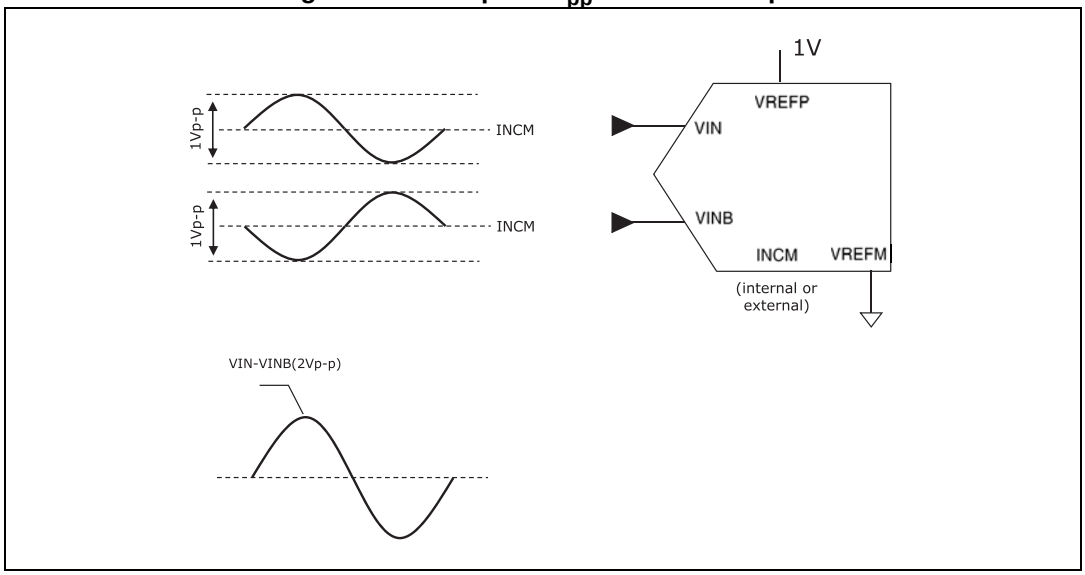
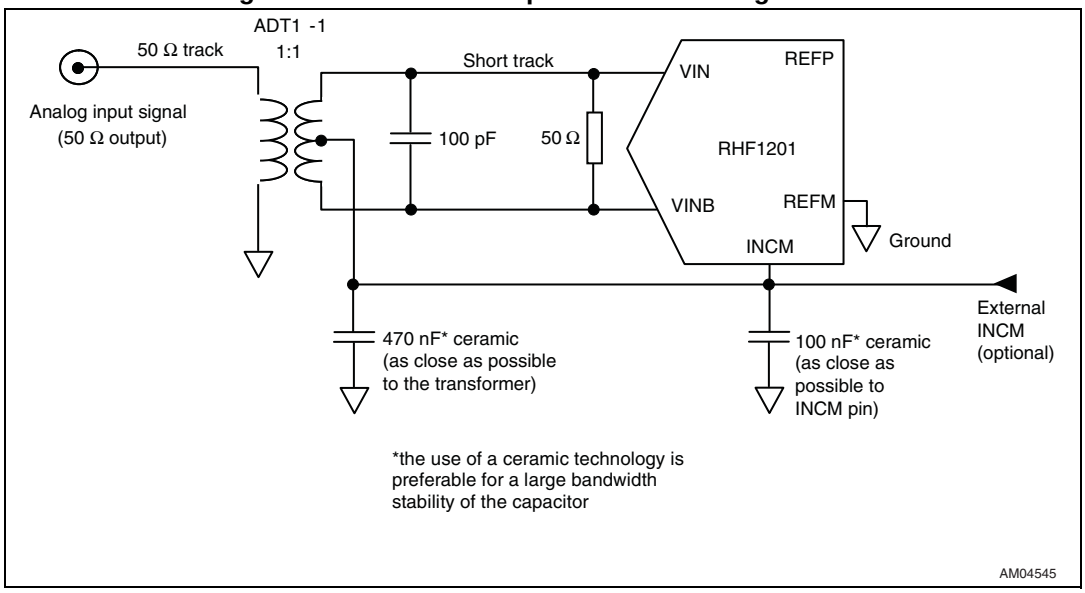


Figure 18 shows an isolated differential input solution. The input signal is fed to the transformer's primary, while the secondary drives both ADC inputs. The transformer must be matched with generator output impedance: 50 Ω in this case for proper matching with a 50 Ω generator. The tracks between the secondary and Vin and Vinb pins must be as short as possible.

Figure 18. Differential implementation using a balun

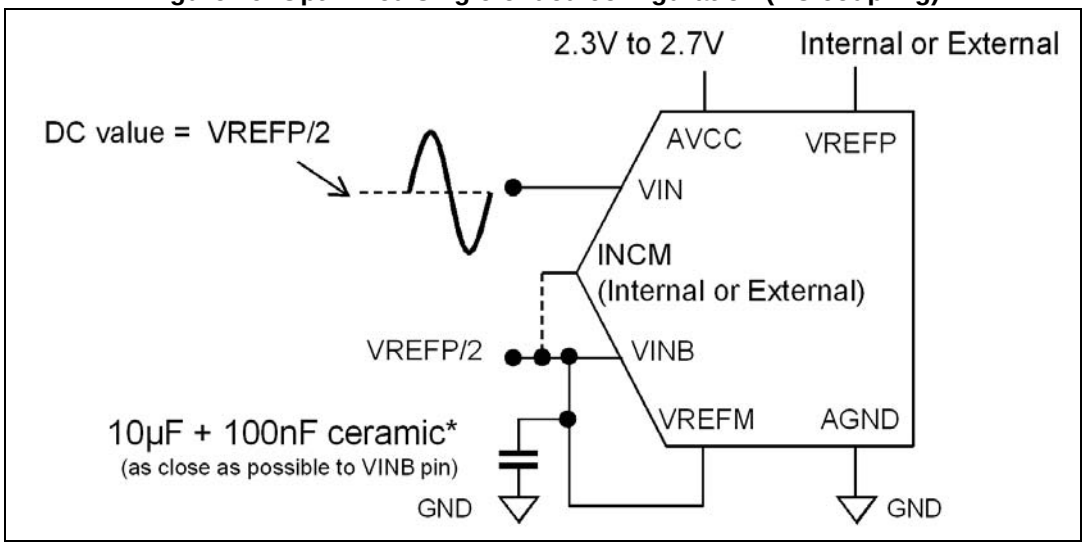


The input common-mode voltage of the ADC (INCM) is connected to the center tap of the transformer's secondary in order to bias the input signal around the common voltage (see *Table 7*).The INCM is decoupled to maintain a low noise level on this node. Ceramic technology for decoupling provides good capacitor stability across a wide bandwidth.

Single-ended mode

Figure 19 shows an example of how to drive RHF1201 in single-ended and DC coupled. This is the optimized configuration recommended. For more explanations, see *Section 5.2: Driving the analog input: how to correctly bias the RHF1201.*

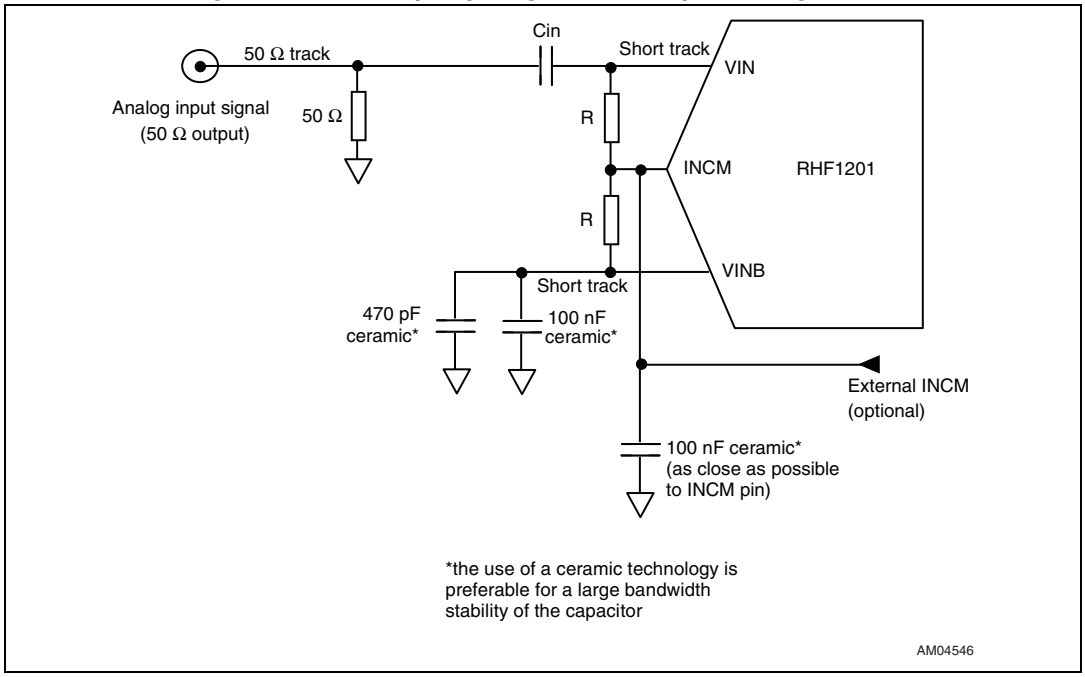
Figure 19. Optimized single-ended configuration (DC coupling)



*Note: *The use of ceramic technology is preferable to ensure large bandwidth stability of the capacitor.*

As some applications may require a single-ended input, it can be easily done with the configuration shown in *Figure 19* for DC coupling and *Figure 20* for AC coupling. However, with this type of configuration, a degradation in the rated performance of the RHF1201 may occur compared with a differential configuration. **You should expect a degradation of ENOB of about 2 bits compared to differential mode.** A sufficiently decoupled DC reference should be used to bias the RHF1201 inputs. An AC-coupled analog input can also be used and the DC analog level set with a high value resistor R (10 ΩW) connected to a proper DC source. Cin and R behave like a high-pass filter and are calculated to set the lowest possible cutoff frequency.

Figure 20. AC-coupling single-ended input configuration



5.5 Reference connections

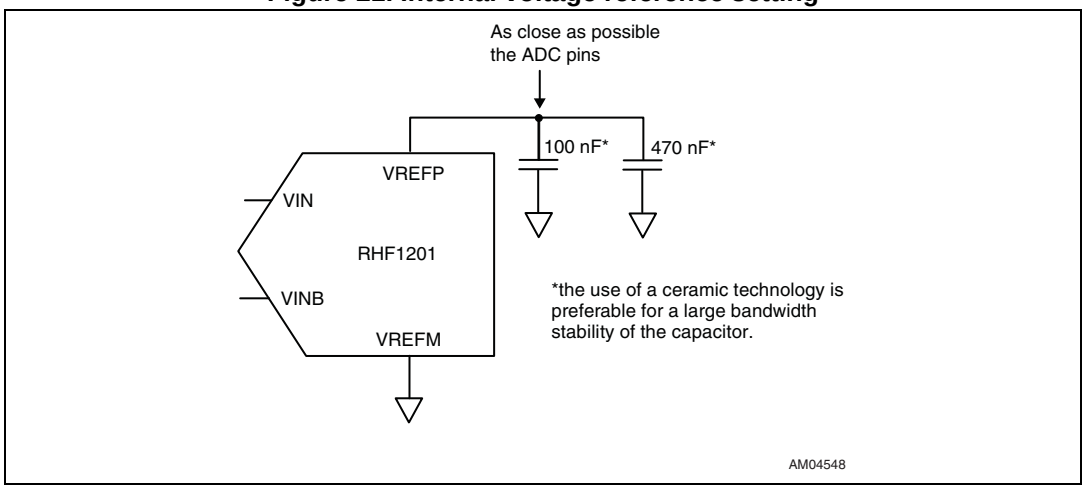
5.5.1 Internal voltage reference

In standard configuration, the ADC is biased with two internal voltage references: VREFP and INCM. They must be decoupled to minimize low and high frequency noise.

Both internal voltage references are able to drive external components.

The VREFM pin has no internal reference and must be connected to a voltage reference. It is usually connected to the analog ground for differential mode and to Vrefp/2 for single-ended mode.

Figure 21. Internal voltage reference setting



5.5.2 External voltage reference

External voltage references can be used for specific applications requiring better linearity, enhanced temperature behavior, or different voltage values (see *Table 4: Operating conditions*). Internal voltage references cannot be disabled but can be forced externally. As this voltage is forced on an internal resistance that is relatively low, the driver will have to be able to sink or source a certain amount of current.

Figure 22 shows the equivalent internal schematic of Vrefp and INCM inputs.

Internal value of Vrefp, INCM and Rout can be found in *Table 7: Internal reference voltage*.

When you force externally a voltage on Vrfep/INCM pin, a sink or a source current must be provide by the driver and this current is expressed with the following equation:

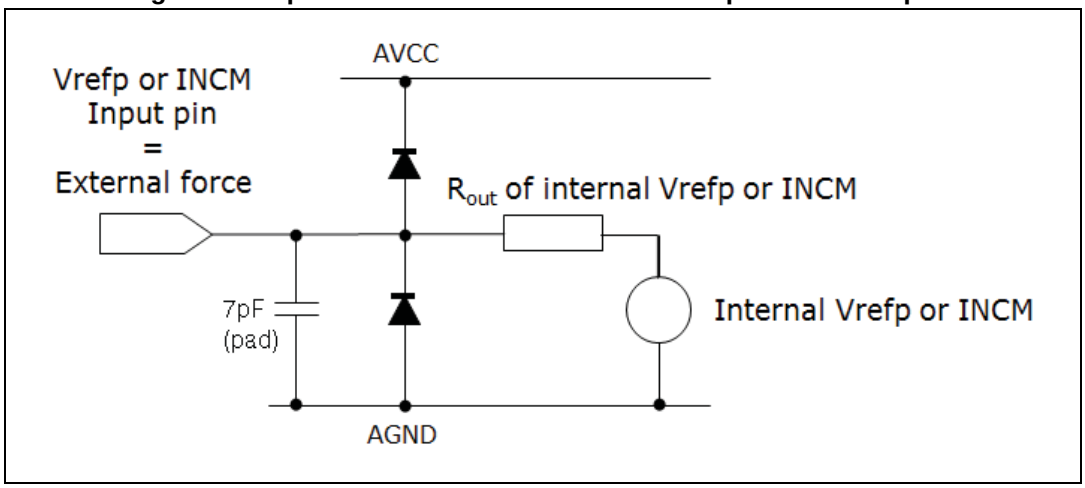
$$\text{Isink or source} = \frac{(\text{External Vrefp/INCM force} - \text{Internal Vrefp/INCM})}{\text{Vrefp/INCM Rout}}$$

Depending on the difference between the external and internal value, the current can be positive or negative (source/sink).

Example 1: You wanted to force Vrefp at 1.2 V and on the RHF1201, internal Vrefp = 0.85 V. As Rout for Vrefp = 39 Ω, the current provided by the driver will be positive and equal to (1.2 - 0.85)/39 = 9 mA

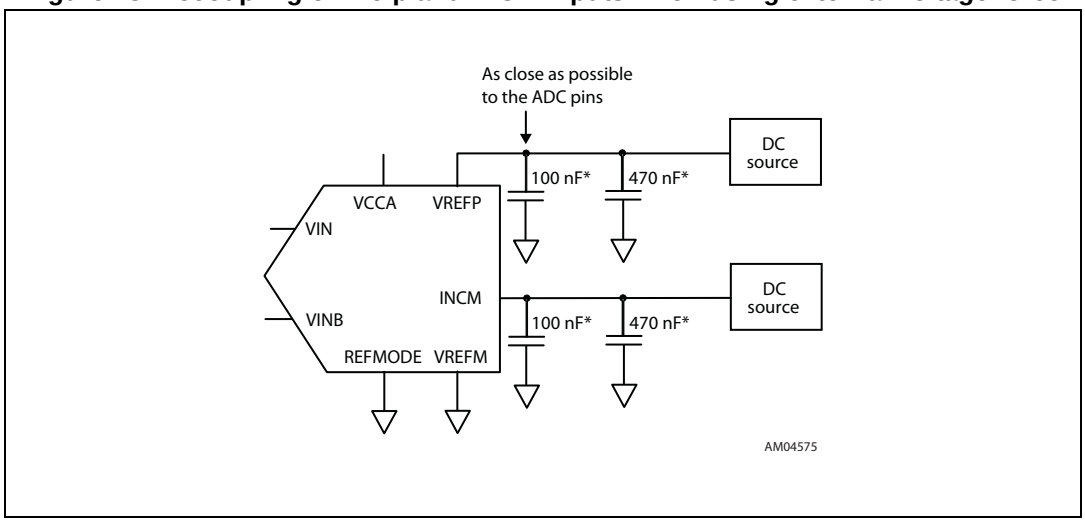
Example 2: You wanted to force INCM at 0.4 V and on the RHF1201 internal INCM = 0.5 V. As Rout for INCM= 50 Ω, the current provided by the driver will be negative and equal to (0.4 - 0.5)/50 = 2 mA.

Figure 22. Equivalent internal schematic of Vrefp and INCM inputs



Of course, the external voltage references with the configuration shown in *Figure 23*, must be decoupled by using ceramic capacitors to achieve optimum linearity versus frequency.

Figure 23. Decoupling of Vrefp and INCM inputs when using external voltage force



*Note: *The use of ceramic technology is preferable to ensure large bandwidth stability of the capacitor.*

5.6 Clock input

The quality of the converter very much depends on the accuracy of the clock input in terms of jitter. The use of a low-jitter, crystal-controlled oscillator is recommended.

The following points should also be considered.

- The clock's power supplies must be independent of the ADC's output supplies to avoid digital noise modulation at the output.
- When powered on, the circuit needs several clock periods to reach its normal operating conditions.
- The square clock must respect the values in *Table 5* and *Table 9.*

The signal applied to the CLK pin is critical to obtain full performance from the RHF1201. It is recommended to use a square signal with fast transition times and to place proper termination resistors as close as possible to the device.

5.7 Reset of RHF1201

To reset the RHF1201, it is **mandatory** to apply several clock periods.

At power-up, without any clock signal applied to RHF1201, the device is not reset.

In this case, parameters like Vrefp, INCM and Rout are in line with values in*Table 7*.

5.8 RHF1201 operating modes

Extra functionalities are provided to simplify the application board as much as possible. The operating modes offered by the RHF1201 are described in *Table 13*.

Table 13. RHF1201 operating modes

Inputs				Outputs		
Analog input differential amplitude	**DFSB**	**OEB**	**SRC**	**OR**	**DR**	**Most significant bit (MSB)**
(V_{IN}-V_{INB}) above maximum range	H	L	X	H	CLK	D11
	L	L	X	H	CLK	D11 complemented
(V_{IN}-V_{INB}) below minimum range	H	L	X	H	CLK	D11
	L	L	X	H	CLK	D11 complemented
(V_{IN}-V_{INB}) within range	H	L	X	L	CLK	D11
	L	L	X	L	CLK	D11 complemented
X	X	H	X	High impedance		
	X	L	H	X	CLK low slew rate	Low slew rate
	X	L	L	X	CLK high slew rate	High slew rate

5.8.1 Digital inputs

Data format select (DFSB): when set to low level (V_{IL}), the digital input DFSB provides a two's complement digital output MSB. This can be of interest when performing some further signal processing. When set to high level (V_{IH}), DFSB provides a standard binary output coding.

Output enable (OEB): when set to low level (V_{IL}), all digital outputs remain active. When set to high level (V_{IH}), all digital output buffers are in high impedance state while the converter goes on sampling. When OEB is set to a low level again, the data arrives on the output with a very short T_{on} delay. This feature enables the chip select of the device. *Figure 11: Timing diagram* summarizes this functionality.

Slew rate control (SRC): when set to high level (V_{IH}), all digital output currents are limited to a clamp value so that any digital noise power is reduced to the minimum. When set to low level (V_{IL}), the output edges are twice as fast.

5.8.2 Digital outputs

Out-of-range (OR): this function is implemented at the output stage to automatically detect any digital data that is over the full-scale range. For data within the range, OR remains in a low-level state (V_{OL}), but switches to a high-level state (V_{OH}) as soon as out-of-range data is detected.

Data ready (DR): the data ready output is an image of the clock being synchronized on the output data (D0 to D11). This is a very helpful signal that simplifies the synchronization of the measurement equipment or of the controlling DSP.

As all other digital outputs, DR and OR go into a high impedance state when OEB is set to high level, as shown in *Figure 11: Timing diagram*.

5.9 Digital output load considerations

The features of the internal output buffers limit the maximum load on the digital data output. In particular, the shape and amplitude of the Data Ready signal, toggling at the clock frequency, can be weakened by a higher equivalent load.

In applications that impose higher load conditions, it is recommended to use the falling edge of the master clock instead of the Data Ready signal. This is possible because the output transitions are internally synchronized with the falling edge of the clock.

Figure 24. Output buffer fall time

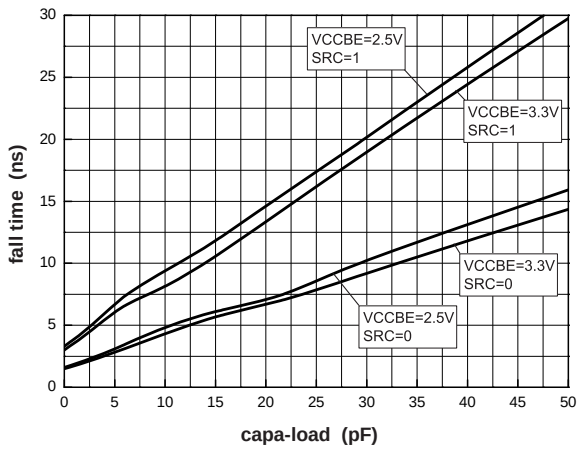
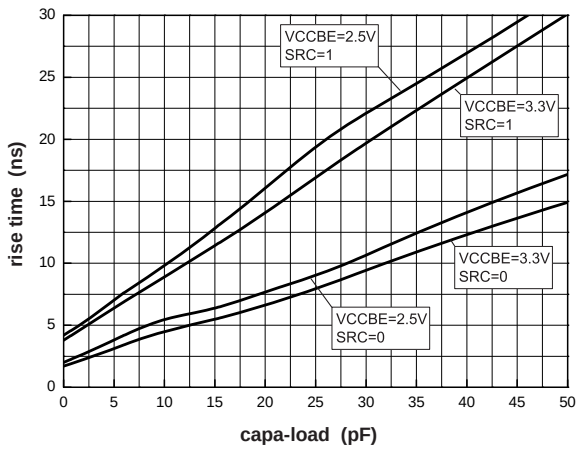


Figure 25. Output buffer rise time



5.10 PCB layout precautions

- A ground plane on each layer of the PCB with multiple vias dedicated for inter connexion is recommended for high-speed circuit applications to provide low parasitic inductance and resistance. The goal is to have a “common ground plane” where AGND and DGND are connected with the lowest DC resistance and lowest AC impedance.
- The separation of the analog signal from the digital output is mandatory to prevent noise from coupling onto the input signal.
- Power supply bypass capacitors must be placed as close as possible to the IC pins to improve high-frequency bypassing and reduce harmonic distortion.
- All leads must be as short as possible, especially for the analog input, so as to decrease parasitic capacitance and inductance.
- To minimize the transition current when the output changes, the capacitive load at the digital outputs must be reduced as much as possible by using the shortest possible routing tracks. One way to reduce capacitive load is to remove the ground plane under the output digital pins and layers at high sampling frequencies.
- Choose the smallest possible component sizes (SMD)

6 Definitions of specified parameters

6.1 Static parameters

Differential non-linearity (DNL)

The average deviation of any output code width from the ideal code width of 1 LSB.

Integral non-linearity (INL)

An ideal converter exhibits a transfer function which is a straight line from the starting code to the ending code. The INL is the deviation from this ideal line for each transition.

6.2 Dynamic parameters

Spurious free dynamic range (SFDR)

The ratio between the power of the worst spurious signal (not always a harmonic) and the amplitude of the fundamental tone (signal power) over the full Nyquist band. Expressed in dBc.

Total harmonic distortion (THD)

The ratio of the rms sum of the first five harmonic distortion components to the rms value of the fundamental line. Expressed in dB.

Signal-to-noise ratio (SNR)

The ratio of the rms value of the fundamental component to the rms sum of all other spectral components in the Nyquist band ($f_S/2$) excluding DC, fundamental, and the first five harmonics. SNR is reported in dB.

Signal-to-noise and distortion ratio (SINAD)

Similar ratio as for SNR but including the harmonic distortion components in the noise figure (not DC signal). Expressed in dB.

The effective number of bits (ENOB) is easily deduced from the SINAD, using the formula:

$$SINAD = 6.02 \times ENOB + 1.76 \text{ dB}$$

When the applied signal is not full scale (FS) but has an amplitude A_0, the SINAD expression becomes:

$$SINAD = 6.02 \times ENOB + 1.76 \text{ dB} + 20 \log (A_0/FS)$$

ENOB is expressed in bits.

Effective resolution bandwidth

For a given sampling rate and clock jitter, this is the analog input frequency at which the SINAD is reduced by 3 dB, and the ENOB is reduced by 0.5 bits.

Pipeline delay

Delay between the initial sample of the analog input and the availability of the corresponding digital data output on the output bus. Also called data latency, it is expressed as a number of clock cycles.

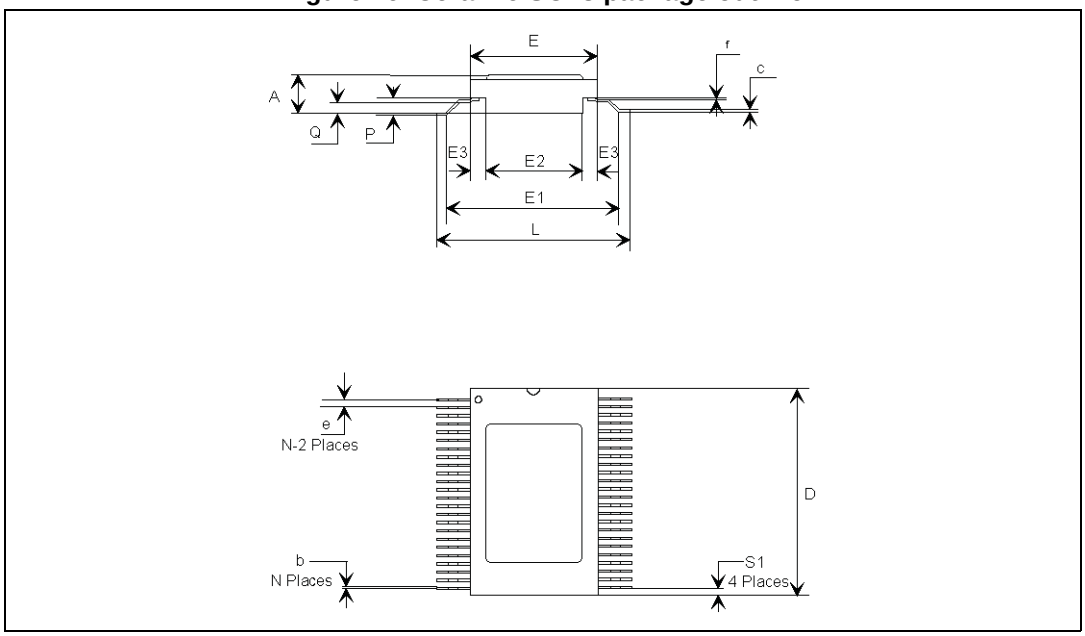
When powering *off* to *on*, there is a delay of several clock cycles before the ADC can achieve a reliable and stable signal conversion. During this delay, some conversion artifacts may appear.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 SO48 package information

Figure 26. Ceramic SO48 package outline



1. The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting unused pins or metal lid to ground or to the power supply will not affect the electrical characteristics.

Table 14. Ceramic SO48 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18	2.47	2.72	0.086	0.097	0.107
b	0.20	0.254	0.30	0.008	0.010	0.012
c	0.12	0.15	0.18	0.005	0.006	0.007
D	15.57	15.75	15.92	0.613	0.620	0.627
E	9.52	9.65	9.78	0.375	0.380	0.385
E1		10.90			0.429	
E2	6.22	6.35	6.48	0.245	0.250	0.255
E3	1.52	1.65	1.78	0.060	0.065	0.070
e		0.635			0.025	
f		0.20			0.008	
L	12.28	12.58	12.88	0.483	0.495	0.507
P	1.30	1.45	1.60	0.051	0.057	0.063
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.25	0.43	0.61	0.010	0.017	0.024

8 Ordering information

Table 15. Order code

Order code	Description	Temp. range	Package	Marking (1)	Packing
RHF1201KSO1	Engineering model	-55 °C to 125 °C	SO48	RHF1201KSO1	Strip pack
RHF1201KSO-01V	QML-V flight			5962F0521701VXC	

1. Specific marking only. Complete marking includes the following:
   - SMD pin (for QML flight only)
   - ST logo
   - Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)
   - QML logo (Q or V)
   - Country of origin (FR = France)

Note: Contact your ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.

9 Other information

9.1 Date code

The date code is structured as shown below:

- Engineering model: EM xyywwz
- QML flight model: FM yywwz

Where:

x (EM only): 3, assembly location Rennes (France)

yy: last two digit year

ww: week digits

z: lot index in the week

9.2 Documentation

Table 16. Documentation provided for QMLV flight

Quality level	Documentation
Engineering model	
QML-V flight	– Certificate of conformance with Group C (reliability test) and group D (package qualification) reference – Precap report – PIND(1) test summary (test method conformance certificate) – SEM(2) report – X-ray report – Screening summary – Failed component list (list of components that have failed during screening) – Group A summary (QCI(3) electrical test) – Group B summary (QCI(3) mechanical test) – Group E (QCI(3) wafer lot radiation test)

1. PIND = particle impact noise detection
2. SEM = scanning electron microscope
3. QCI = quality conformance inspection

10 Revision history

Table 17. Document revision history

Date	Revision	Changes
01-Sep-2006	1	Initial release in new format.
29-Jun-2007	2	Updated failure immune and latchup immune value to 120 MeV-cm^2/mg. Updated package mechanical data. Removed reference to non rad-hard components from Section 5.4.2: External voltage reference on page 24.
10-Oct-2008	3	Changed cover page graphic. Changed Figure 2. Added Chapter 1.4: Equivalent circuits. Added Note 1 under Table 3. Expanded Table 4 with additional parameters. Modified “Test conditions” and Vrefp/Vincm in Table 7. Improved readability in Table 13. Added Figure 16 to Figure 18. Modified Figure 18 and Figure 20. Added Figure 21. Removed IF sampling section. Modified Figure 22 and Figure 16. Added Figure 12. Added ECOPACK information and updated presentation in Chapter 7.
09-Apr-2010	4	Modified description on cover page. Added Table 1: Device summary on page 1. Removed RHF1201KSO2 order code from Table 1. Removed Fs and Tck values from Table 5. Added Figure 7 and Figure 8. Added DFS, OEB and SRC values in Table 4. Changed VINCM values in Table 4. Removed Fin values from Table 4. Removed output capacitive load values from Table 9. Changed clock threshold values in Table 9. Added PSRR values in Table 10. Added Figure 13 on page 14 to Figure 44. Modified Figure 16, Figure 19 and Figure 18.
29-Jul-2011	5	Added 1. on page 33 and in the “Pin connections” diagram on the cover page.

Table 17. Document revision history (continued)

Date	Revision	Changes
24-July-2014	6	Updated Figure 1: Block diagram Updated Figure 3: Analog inputs, Figure 4: Output buffers Updated Table 4, Table 5 and Figure 11; added new text. Updated Table 6, Table 8. Rewording and new Section 5.1: Power consumption optimization, Section 5.2: Driving the analog input: how to correctly bias the RHF1201, Section 5.3: Output code vs. analog input and mode usage, Section 5.4: Design examples, Section 5.5: Reference connections, Section 5.6: Clock input, Section 5.7: Reset of RHF1201, Section 5.8: RHF1201 operating modes, Section 5.9: Digital output load considerations, Section 5.10: PCB layout precautions Added Section 8: Ordering information, Section 9: Other information
08-July-2015	7	Corrected Table 5: Timing table Corrected Figure 11: Timing diagram
21-Sep-2017	8	Updated V_{OL} and V_{OH} test conditions in *Table 9: Digital inputs and outputs*.
06-Dec-2017	9	Updated the features, description and device summary table in cover page.