

# MC74HCT244A

## Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver with LSTTL-Compatible Inputs

### High-Performance Silicon-Gate CMOS

The MC74HCT244A is identical in pinout to the LS244. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT244A is an octal noninverting buffer line driver line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has non-inverted outputs and two active-low output enables.

The HCT244A is the non-inverting version of the HCT240. See also HCT241.

#### Features

- Output Drive Capability: 15 LSTTL Loads
- TTL NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 112 FETs or 28 Equivalent Gates
- Pb-Free Packages are Available

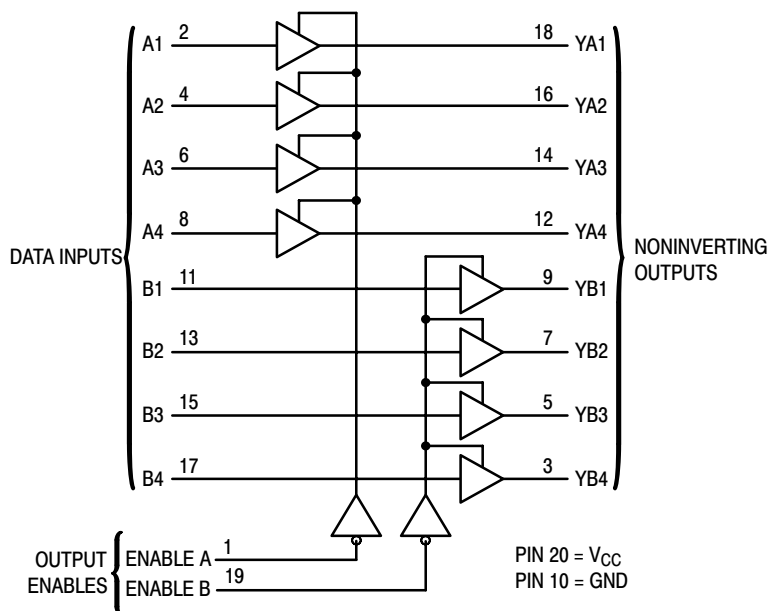
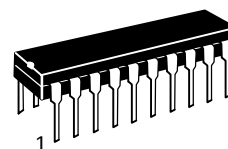


Figure 1. Logic Diagram

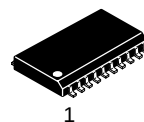


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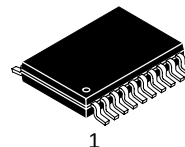
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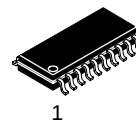
PDIP-20  
N SUFFIX  
CASE 738



SOIC-20W  
DW SUFFIX  
CASE 751D



TSSOP-20  
DT SUFFIX  
CASE 948E



SOEIAJ-20  
M SUFFIX  
CASE 967

#### PIN ASSIGNMENT

|          |    |    |                 |
|----------|----|----|-----------------|
| ENABLE A | 1  | 20 | V <sub>CC</sub> |
| A1       | 2  | 19 | ENABLE B        |
| YB4      | 3  | 18 | YA1             |
| A2       | 4  | 17 | B4              |
| YB3      | 5  | 16 | YA2             |
| A3       | 6  | 15 | B3              |
| YB2      | 7  | 14 | YA3             |
| A4       | 8  | 13 | B2              |
| YB1      | 9  | 12 | YA4             |
| GND      | 10 | 11 | B1              |

#### FUNCTION TABLE

| Inputs                |      | Outputs |
|-----------------------|------|---------|
| Enable A,<br>Enable B | A, B | YA, YB  |
| L                     | L    | L       |
| L                     | H    | H       |
| H                     | X    | Z       |

Z = high impedance, X = don't care

#### ORDERING AND MARKING INFORMATION

See detailed ordering, shipping, and marking information in the package dimensions section on page 5 of this data sheet.

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## MAXIMUM RATINGS

| Symbol    | Parameter                                                                                     | Value                   | Unit |
|-----------|-----------------------------------------------------------------------------------------------|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)                                                         | - 0.5 to + 7            | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)                                                          | - 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)                                                         | - 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin                                                                     | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin                                                                    | $\pm 35$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                                                      | $\pm 75$                | mA   |
| $P_D$     | Power Dissipation in Still Air,<br>Plastic DIP†<br>SOIC Package†<br>TSSOP Package†            | 750<br>500<br>450       | mW   |
| $T_{stg}$ | Storage Temperature                                                                           | - 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP, SOIC, SSOP or TSSOP Package) | 260                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

†Derating  
 - Plastic DIP: - 10 mW/°C from 65° to 125°C  
 - SOIC Package: - 7 mW/°C from 65° to 125°C  
 - TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter                                            | Min  | Max      | Unit |
|-------------------|------------------------------------------------------|------|----------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 4.5  | 5.5      | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0    | $V_{CC}$ | V    |
| $T_A$             | Operating Temperature, All Package Types             | - 55 | + 125    | °C   |
| $t_r, t_f$        | Input Rise and Fall Time (Figure 1)                  | 0    | 500      | ns   |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol           | Parameter                                      | Test Conditions                                                                                                                    | V <sub>CC</sub><br>V | Guaranteed Limit |                 |            | Unit |
|------------------|------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------|-----------------|------------|------|
|                  |                                                |                                                                                                                                    |                      | – 55 to 25° C    | ≤ 85° C         | ≤ 125° C   |      |
| V <sub>IH</sub>  | Minimum High–Level Input Voltage               | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> – 0.1 V<br> I <sub>out</sub>   ≤ 20 μA                                                 | 4.5<br>5.5           | 2<br>2           | 2<br>2          | 2<br>2     | V    |
| V <sub>IL</sub>  | Maximum Low–Level Input Voltage                | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> – 0.1 V<br> I <sub>out</sub>   ≤ 20 μA                                                 | 4.5<br>5.5           | 0.8<br>0.8       | 0.8<br>0.8      | 0.8<br>0.8 | V    |
| V <sub>OH</sub>  | Minimum High–Level Output Voltage              | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                                | 4.5<br>5.5           | 4.4<br>5.4       | 4.4<br>5.4      | 4.4<br>5.4 | V    |
|                  |                                                | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 6 mA                                                 | 4.5                  | 3.98             | 3.84            | 3.7        |      |
| V <sub>OL</sub>  | Maximum Low–Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                                | 4.5<br>5.5           | 0.1<br>0.1       | 0.1<br>0.1      | 0.1<br>0.1 | V    |
|                  |                                                | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 6 mA                                                 | 4.5                  | 0.26             | 0.33            | 0.4        |      |
| I <sub>in</sub>  | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND                                                                                           | 5.5                  | ± 0.1            | ± 1.0           | ± 1.0      | μA   |
| I <sub>OZ</sub>  | Maximum Three–State Leakage Current            | Output in High–Impedance State<br>V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; V <sub>out</sub> = V <sub>CC</sub> or GND | 5.5                  | ± 0.5            | ± 5.0           | ± 10       | μA   |
| I <sub>CC</sub>  | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA                                                                   | 5.5                  | 4                | 40              | 160        | μA   |
| ΔI <sub>CC</sub> | Additional Quiescent Supply Current            | V <sub>in</sub> = 2.4 V, Any One Input<br>V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs<br>I <sub>out</sub> = 0 μA        | 5.5                  | ≥ –55° C         | 25° C to 125° C |            | mA   |
|                  |                                                |                                                                                                                                    |                      | 2.9              | 2.4             |            |      |

- Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
- Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

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## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ , $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

| Symbol                   | Parameter                                                                  | Guaranteed Limit |        |         | Unit |
|--------------------------|----------------------------------------------------------------------------|------------------|--------|---------|------|
|                          |                                                                            | - 55 to 25°C     | ≤ 85°C | ≤ 125°C |      |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Maximum Propagation Delay, A to YA or B to YB<br>(Figures 1 and 3)         | 20               | 25     | 30      | ns   |
| $t_{PLZ}$ ,<br>$t_{PHZ}$ | Maximum Propagation Delay, Output Enable to YA or YB<br>(Figures 2 and 4)  | 26               | 33     | 39      | ns   |
| $t_{PZL}$ ,<br>$t_{PZH}$ | Maximum Propagation Delay, Output Enable to YA or YB<br>(Figures 2 and 4)  | 22               | 28     | 33      | ns   |
| $t_{TLH}$ ,<br>$t_{THL}$ | Maximum Output Transition Time, Any Output<br>(Figures 1 and 3)            | 12               | 15     | 18      | ns   |
| $C_{in}$                 | Maximum Input Capacitance                                                  | 10               | 10     | 10      | pF   |
| $C_{out}$                | Maximum Three-State Output Capacitance<br>(Output in High-Impedance State) | 15               | 15     | 15      | pF   |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| $C_{PD}$ | Power Dissipation Capacitance (Per Enabled Output)* | Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$ | pF |
|----------|-----------------------------------------------------|------------------------------------------|----|
|          |                                                     | 55                                       |    |

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## SWITCHING WAVEFORMS

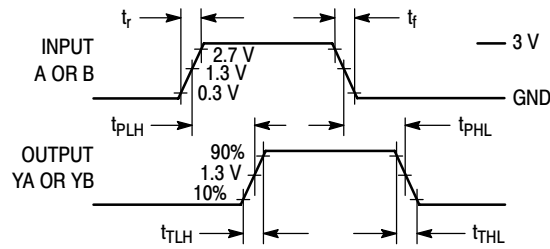


Figure 2.

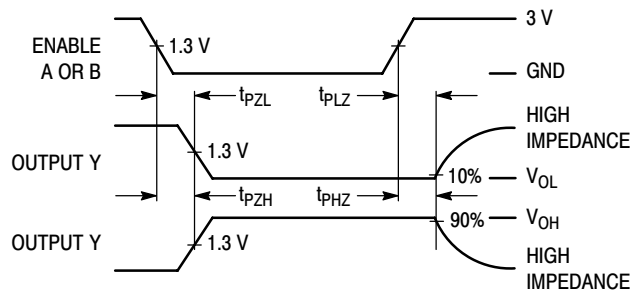
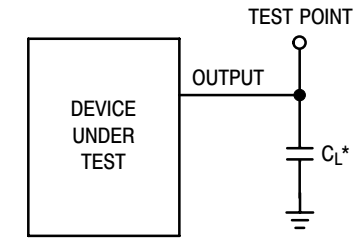


Figure 3.

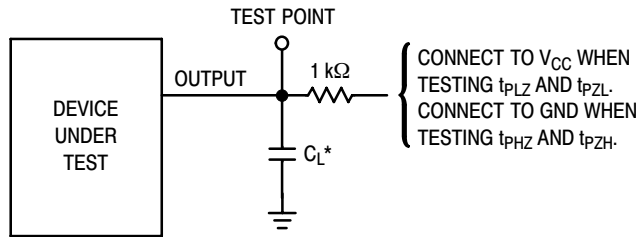
# MC74HCT244A

## TEST CIRCUITS



\*Includes all probe and jig capacitance

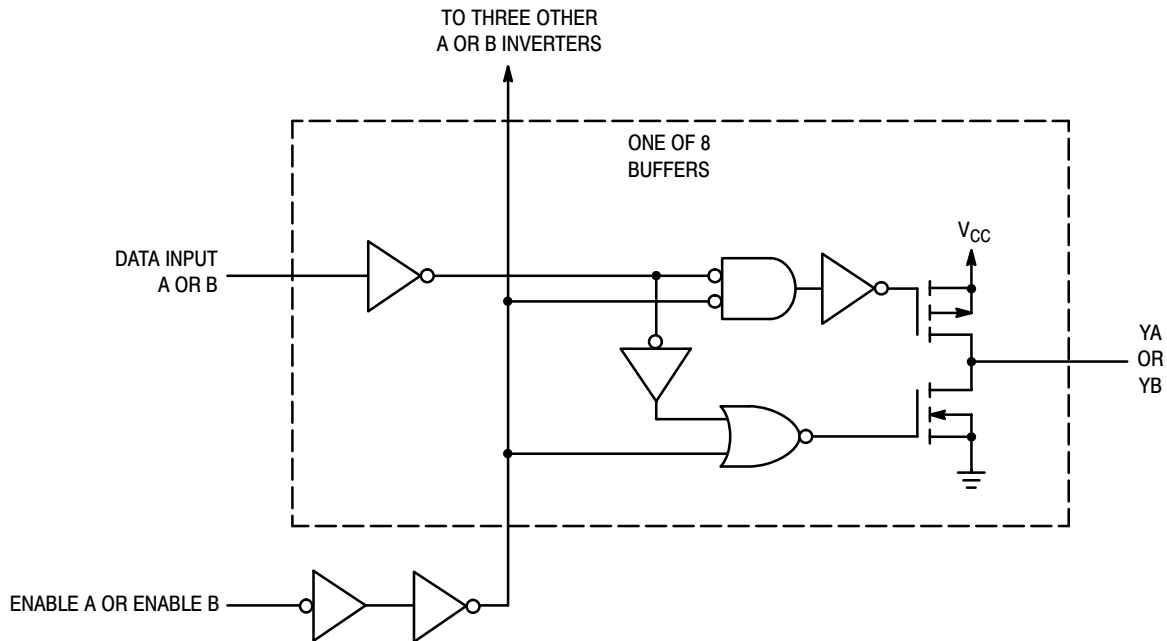
Figure 4.



\*Includes all probe and jig capacitance

Figure 5.

## LOGIC DETAIL



# MC74HCT244A

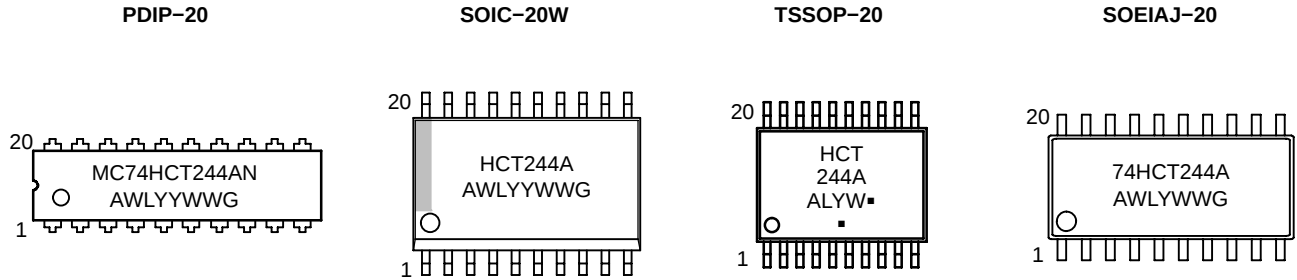
## ORDERING INFORMATION

| Device           | Package                | Shipping <sup>†</sup> |
|------------------|------------------------|-----------------------|
| MC74HCT244AN     | PDIP-20                | 18 Units / Rail       |
| MC74HCT244ANG    | PDIP-20<br>(Pb-Free)   |                       |
| MC74HCT244ADW    | SOIC-20                | 38 Units / Rail       |
| MC74HCT244ADWG   | SOIC-20<br>(Pb-Free)   |                       |
| MC74HCT244ADWR2  | SOIC-20                | 1000 / Tape & Reel    |
| MC74HCT244ADWR2G | SOIC-20<br>(Pb-Free)   |                       |
| MC74HCT244ADTR2  | TSSOP-20*              | 2500 / Tape & Reel    |
| MC74HCT244ADTR2G | TSSOP-20*              |                       |
| MC74HCT244AF     | SOEIAJ-20              | 40 Units / Rail       |
| MC74HCT244AFG    | SOEIAJ-20<br>(Pb-Free) |                       |
| MC74HCT244AFEL   | SOEIAJ-20              | 2000 / Tape & Reel    |
| MC74HCT244AFELG  | SOEIAJ-20<br>(Pb-Free) |                       |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*These packages are inherently Pb-Free.

## MARKING DIAGRAMS



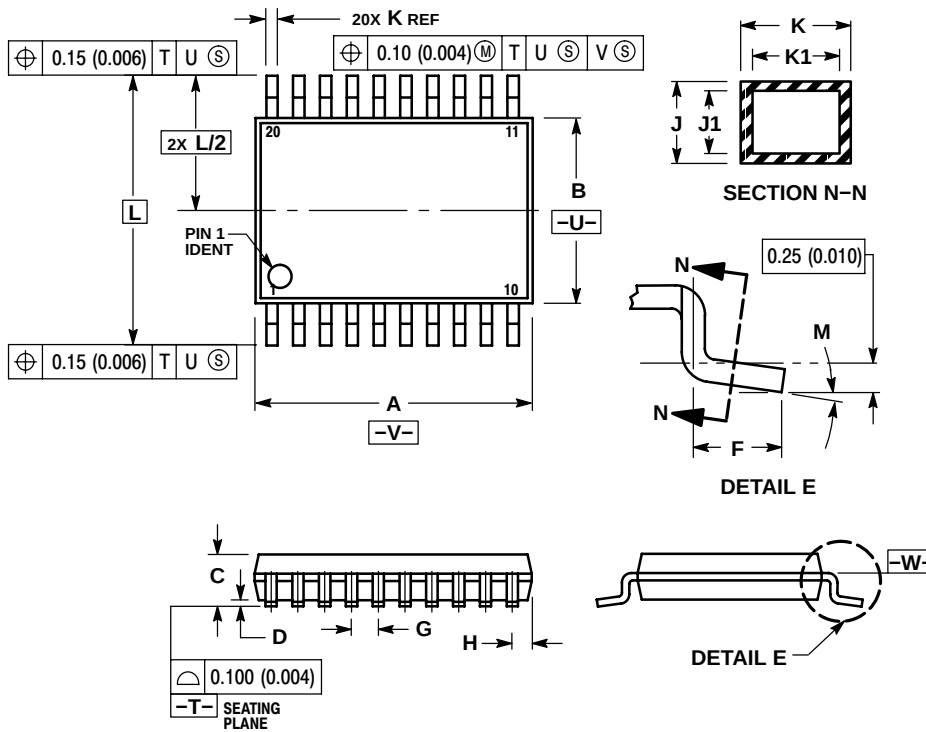
A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G or ■ = Pb-Free Package  
 (Note: Microdot may be in either location)



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## PACKAGE DIMENSIONS

TSSOP-20  
DT SUFFIX  
CASE 948E-02  
ISSUE C

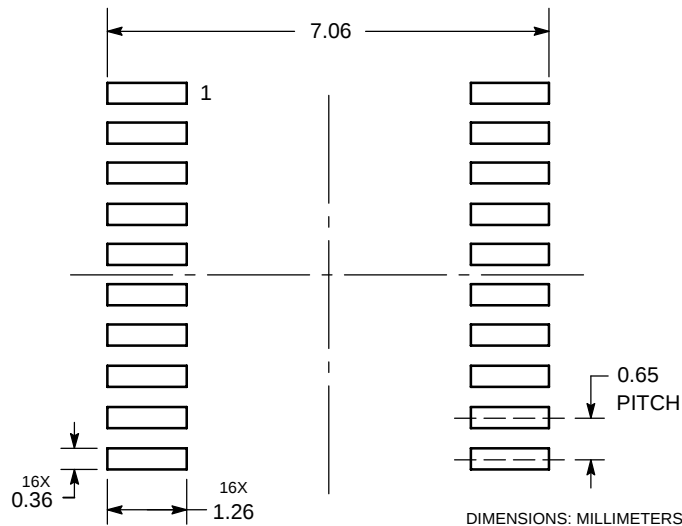


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 6.40        | 6.60 | 0.252     | 0.260 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.27        | 0.37 | 0.011     | 0.015 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

### SOLDERING FOOTPRINT\*

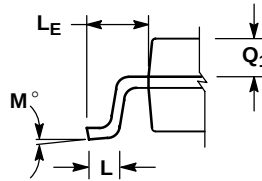
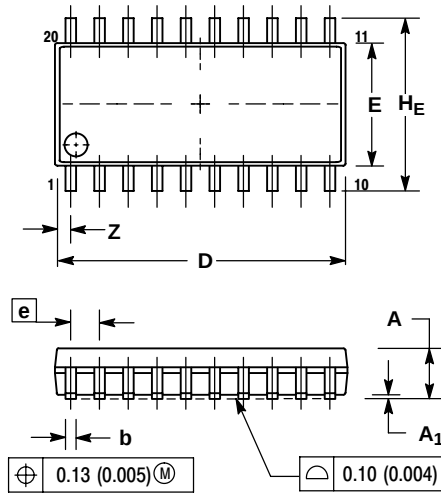


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

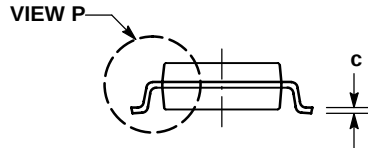
# MC74HCT244A

## PACKAGE DIMENSIONS

SOEIAJ-20  
F SUFFIX  
CASE 967-01  
ISSUE A



DETAIL P



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.15        | 0.25  | 0.006     | 0.010 |
| D              | 12.35       | 12.80 | 0.486     | 0.504 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| H <sub>E</sub> | 7.40        | 8.20  | 0.291     | 0.323 |
| L              | 0.50        | 0.85  | 0.020     | 0.033 |
| L <sub>E</sub> | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 0.81  | ---       | 0.032 |

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