

AZ10ELT20

AZ100ELT20

CMOS/TTL to Differential PECL Translator

FEATURES

- 0.5ns Typical Propagation Delay
- Differential PECL Outputs
- Flow Through Pinouts
- Operating Range of 3.0V to 5.5V
- Direct Replacement for ON Semiconductor MC10ELT20 & MC100ELT20
- Available in a 3x3mm MLP Package

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING
SOIC 8	AZ10ELT20D	AZM10ELT20
SOIC 8 T&R	AZ10ELT20DR1	AZM10ELT20
SOIC 8 T&R	AZ10ELT20DR2	AZM10ELT20
SOIC 8	AZ100ELT20D	AZM100ELT20
SOIC 8 T&R	AZ100ELT20DR1	AZM100ELT20
SOIC 8 T&R	AZ100ELT20DR2	AZM100ELT20
MLP 16	AZ10/100ELT20L	AZMT20
MLP 16 T&R	AZ10/100ELT20LR1	AZMT20
MLP 16 T&R	AZ10/100ELT20LR2	AZMT20
TSSOP 8	AZ10ELT20T	AZTLT20
TSSOP 8 T&R	AZ10ELT20TR1	AZTLT20
TSSOP 8 T&R	AZ10ELT20TR2	AZTLT20
TSSOP 8	AZ100ELT20T	AZHLT20
TSSOP 8 T&R	AZ100ELT20TR1	AZHLT20
TSSOP 8 T&R	AZ100ELT20TR2	AZHLT20
DIE	AZ10/100ELT20X	N/A

DESCRIPTION

The AZ10/100ELT20 is a CMOS/TTL to differential PECL translator. Because PECL (Positive ECL) levels are used, only V_{CC} and ground are required. The small outline packaging and the single gate of the ELT20 makes it ideal for those applications where space, performance and low power are at a premium.

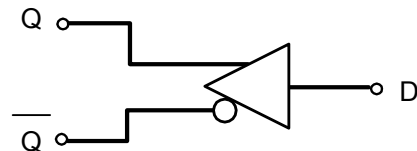
The ELT20 is available in both PECL standards: the 10ELT is compatible with PECL 10K logic levels while the 100ELT is compatible with PECL 100K logic levels.

NOTE: Specifications in PECL tables are valid when thermal equilibrium is established.

PIN DESCRIPTION

PIN	FUNCTION
Q, $\bar{Q}$	Differential PECL Outputs
D	TTL/CMOS Input
GND	Ground
V_{CC} , V_{CCO}	Positive Supply
NC	No Connect
10K, 100K	10K, 100K Mode Select

BLOCK DIAGRAM



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Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	0 to +8.0	V
V _{IN}	Input Voltage	0 to +6.0	V
I _{OUT}	Current Applied to Output in Low Output State --- Continuous --- Surge	50 100	mA
T _A	Operating Temperature Range (In Free-Air)	-40 to +85	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C

TTL/CMOS INPUT DC CHARACTERISTICS (GND = 0.0V, V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I _{IH}	Input HIGH Current			15	μA	V _{IN} = 2.7V
I _{IHH}	Input HIGH Current			20	μA	V _{IN} = V _{CC}
I _{IL}	Input LOW Current			-0.1	mA	V _{IN} = 0.5V
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18mA
V _{IH}	Input HIGH Voltage	2.0			V	
V _{IL}	Input LOW Voltage			0.8	V	

10K LVPECL DC Characteristics (GND = 0.0V, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	2170		2410	2245		2460	2295	2400	2490	2390		2580	mV
V _{OL}	Output LOW Voltage ^{1,2}	1350		1685	1350		1670	1350	1550	1670	1350		1705	mV
I _{CC}	Power Supply Current ³			24			24			24			25	mA

- Output parameters vary 1:1 with V_{CC}.
- Each output is terminated through a 50Ω resistor to V_{CC} - 2V.
- I_{CC} measurements must be done with outputs open.

10K PECL DC Characteristics (GND = 0.0V, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	3870		4110	3945		4160	3995	4100	4190	4090		4280	mV
V _{OL}	Output LOW Voltage ^{1,2}	3050		3385	3050		3370	3050	3250	3370	3050		3405	mV
I _{CC}	Power Supply Current ³			24			24			24			25	mA

- Output parameters vary 1:1 with V_{CC}.
- Each output is terminated through a 50Ω resistor to V_{CC} - 2V.
- I_{CC} measurements must be done with outputs open.

100K LVPECL DC Characteristics (GND = 0.0V, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	2160		2420	2205		2420	2235	2345	2420	2255		2420	mV
V _{OL}	Output LOW Voltage ^{1,2}	1470		1745	1490		1680	1490	1595	1680	1490		1680	mV
I _{CC}	Power Supply Current ³			24			24			24			25	mA

- Output parameters vary 1:1 with V_{CC}.
- Each output is terminated through a 50Ω resistor to V_{CC} - 2V.
- I_{CC} measurements must be done with outputs open.

100K PECL DC Characteristics (GND = 0.0V, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	3860		4120	3905		4120	3935	4045	4120	3955		4120	mV
V _{OL}	Output LOW Voltage ^{1,2}	3170		3445	3190		3380	3190	3295	3380	3190		3380	mV
I _{CC}	Power Supply Current ³			24			24			24			25	mA

- Output parameters vary 1:1 with V_{CC}.
- Each output is terminated through a 50Ω resistor to V_{CC} - 2V.
- I_{CC} measurements must be done with outputs open.

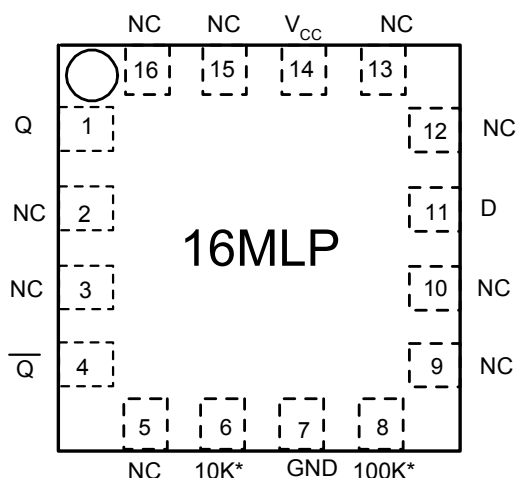
AZ10ELT20

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AC CHARACTERISTICS (GND = 0.0V, V_{CC} = +3.0V to +5.5V)

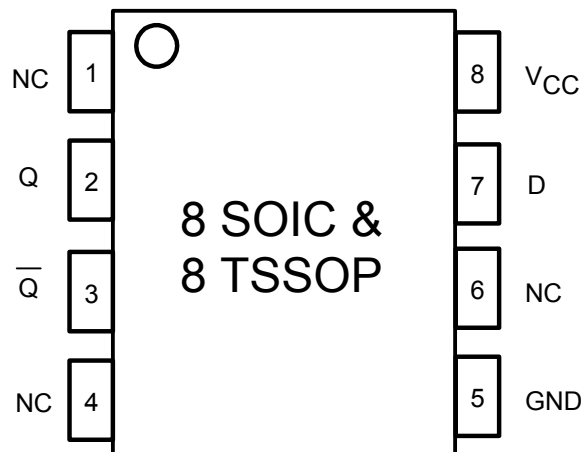
Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Max	Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay ¹	0.2	0.7	0.2	0.7	0.2	0.4	0.7	0.2	0.7	ns	
t _{PHL}	Propagation Delay ¹	0.2	0.7	0.2	0.7	0.2	0.4	0.7	0.2	0.7	ns	
t _r /t _f	Output Rise/Fall Time	0.25	0.7	0.25	0.7	0.25	0.4	0.7	0.25	0.7	ns	20-80%
f _{MAX}	Maximum Frequency ²	350		350		350			350		MHz	
f _{MAX}	Maximum Frequency ³	670		800		800			800		MHz	

1. Propagation delay is measured from +1.5V on the input to 50% of the PECL output swing. Input rise/fall times are < 1ns/V.
2. Full swing PECL output.
3. Output at -3 dB.



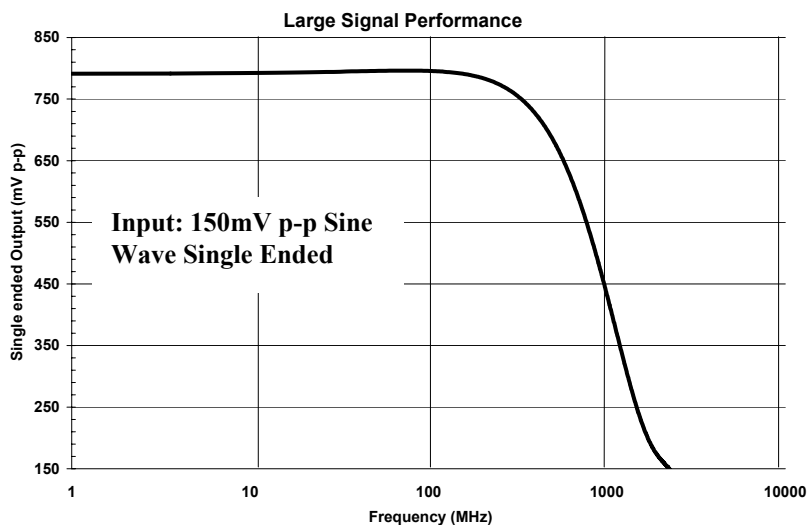
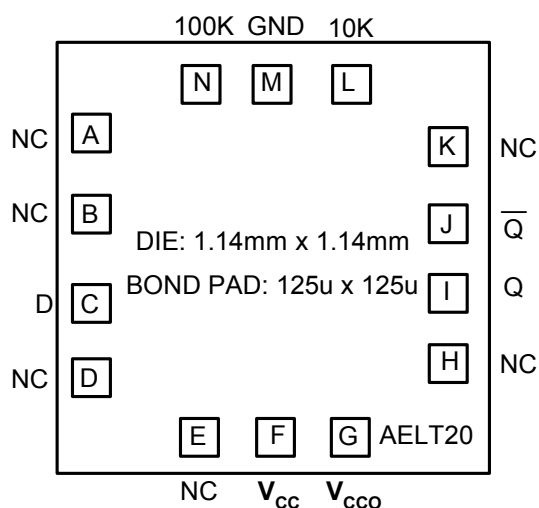
16MLP/ DIE: 10K/100K Selection

Connect pin/pad 10K to GND and float (NC) pin/pad 100K to select 10K operation.
Connect 100K to GND and float (NC) pin/pad 10K to select 100K operation. GND connections must be less than 1Ω.

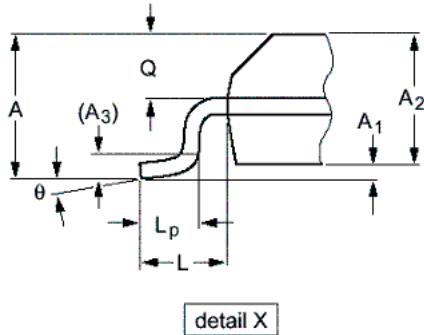
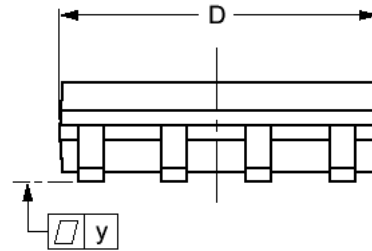
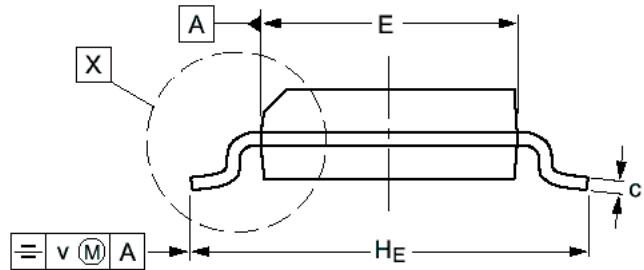
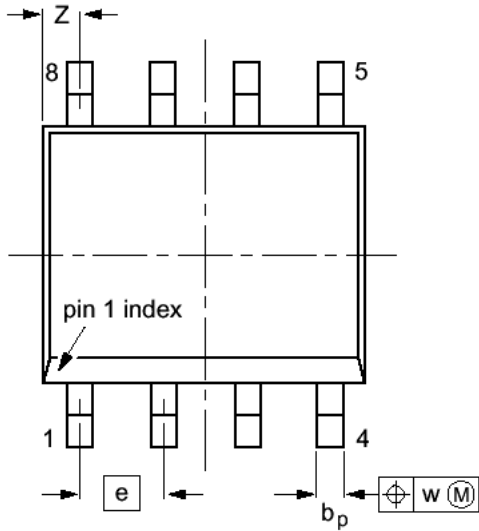


* For 10K: Connect 6 to 7

* For 100K: Connect 8 to 7



**PACKAGE DIAGRAM
SOIC 8**

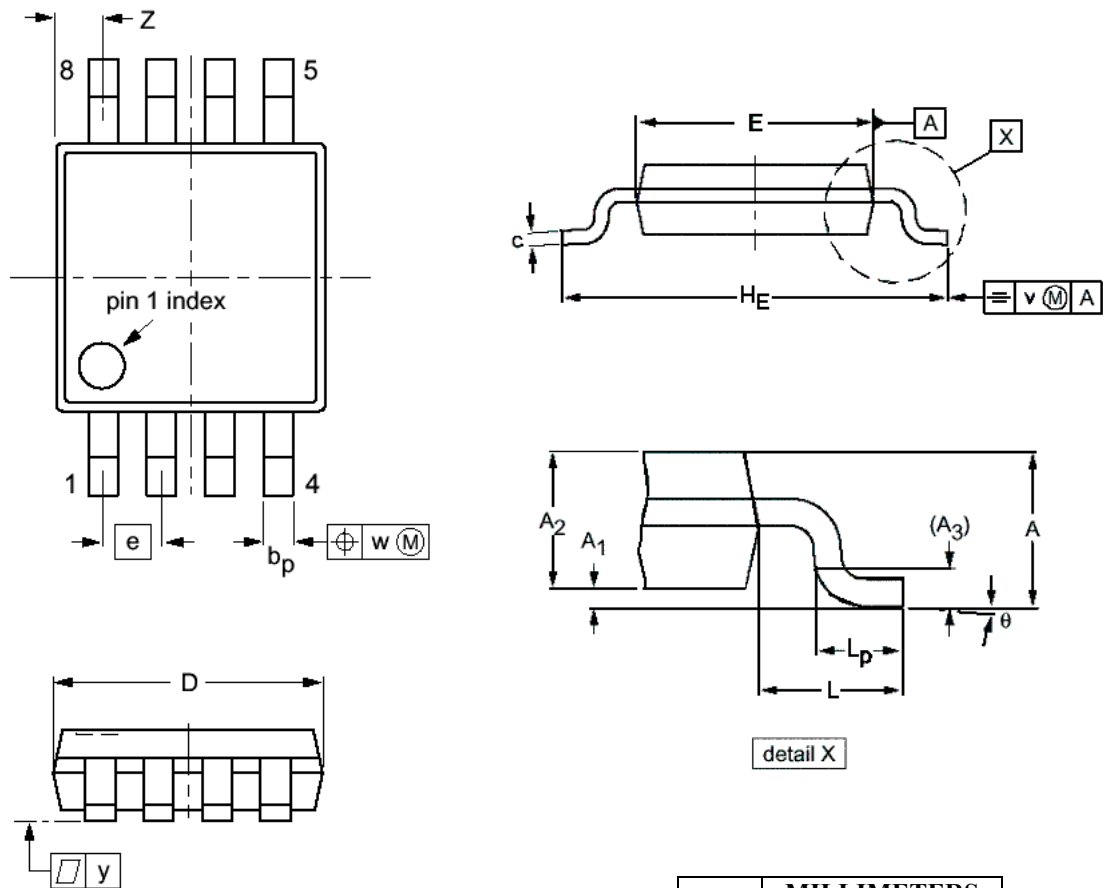


NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	.053	0.069
A ₁	0.10	0.25	0.004	0.010
A ₂	1.28	1.57	0.050	0.062
A ₃	0.25		0.01	
b _p	0.36	0.49	0.014	0.019
c	0.19	0.25	0.0075	0.0100
D	4.80	5.00	0.19	0.20
E	3.80	4.00	0.15	0.16
e	1.27		0.050	
H _E	5.80	6.20	0.228	0.244
L	1.05		0.041	
L _p	0.40	1.27	0.016	0.050
Q	0.60	0.70	0.024	0.028
v	0.25		0.01	
w	0.25		0.01	
y	0.10		0.004	
Z	0.30	0.70	0.012	0.028
θ	0°	8°	0°	8°

PACKAGE DIAGRAM
TSSOP 8

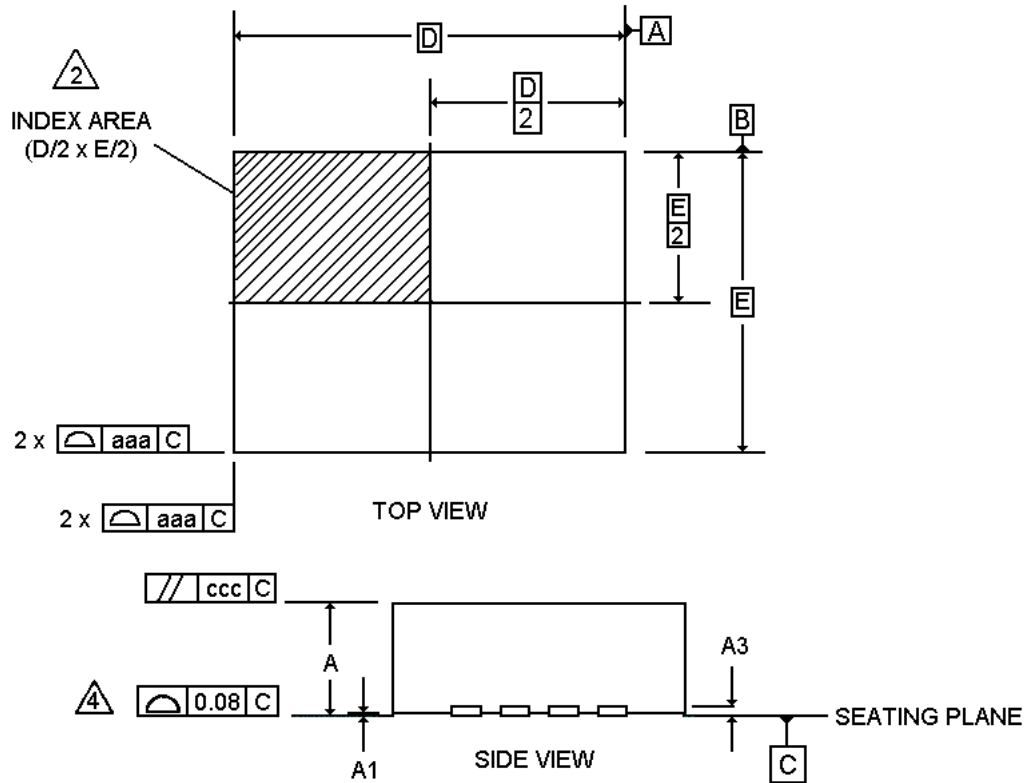


NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A ₁	0.05	0.15
A ₂	0.75	0.95
A ₃	0.25	
b _p	0.22	0.40
c	0.13	0.23
D	2.90	3.10
E	2.90	3.10
e	0.65	
H _E	4.75	5.05
L	0.95	
L _p	0.40	0.70
v	0.10	
w	0.08	
y	0.10	
Z	0.38	0.64
θ	0°	6°

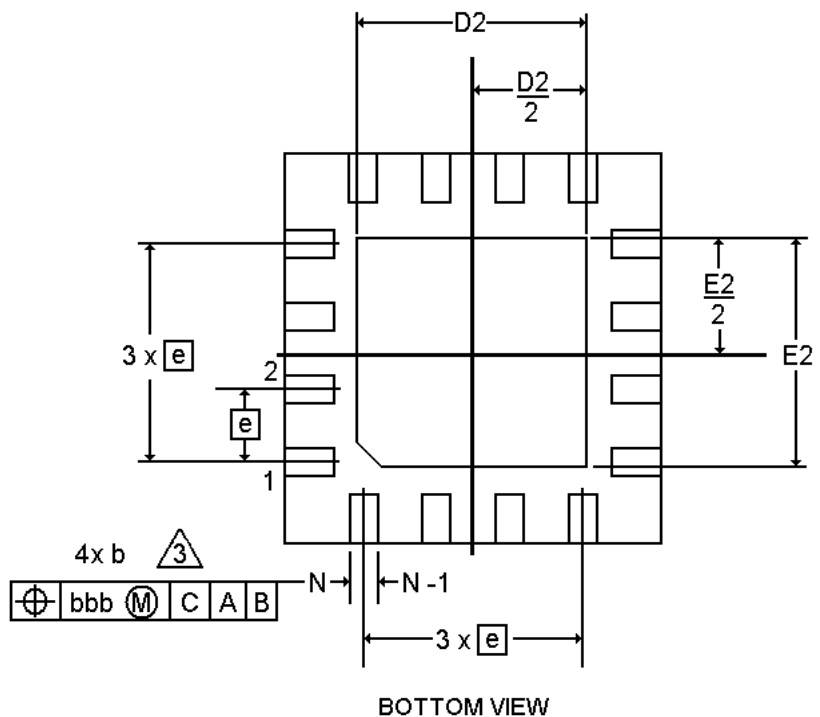
PACKAGE DIAGRAM
MLP 16



NOTES

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
2. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
3. DIMENSION b APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM PAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.18	0.30
D	2.90	3.10
D2	.25	1.95
E	2.90	3.10
E2	.25	1.95
e	0.50 BSC	
L	0.30	0.50
aaa	0.25	
bbb	0.10	
ccc	0.10	



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