



# IMPORTANT NOTICE

10 December 2015

## 1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

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Thank you for your cooperation and understanding,

WeEn Semiconductors

## 1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT186A (TO-220F) "full pack" plastic package intended for use in applications requiring high thermal cycling performance and high junction temperature capability ( $T_{j(max)} = 150\text{ }^{\circ}\text{C}$ ).

## 2. Features and benefits

- High junction operating temperature capability
- High thermal cycling performance
- High voltage capability
- Planar passivated for voltage ruggedness and reliability

### 3. Applications

- Ignition circuits
- Motor control
- Protection circuits e.g. SMPS inrush current
- Voltage regulation

## 4. Quick reference data

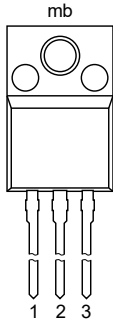

### Table 1. Quick reference data

[illegible]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$ ; $T_j = 150\text{ }^{\circ}\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit		500	-	-	V/ $\mu\text{s}$

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 <p>TO-220F (SOT186A)</p>	
2	A	anode		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

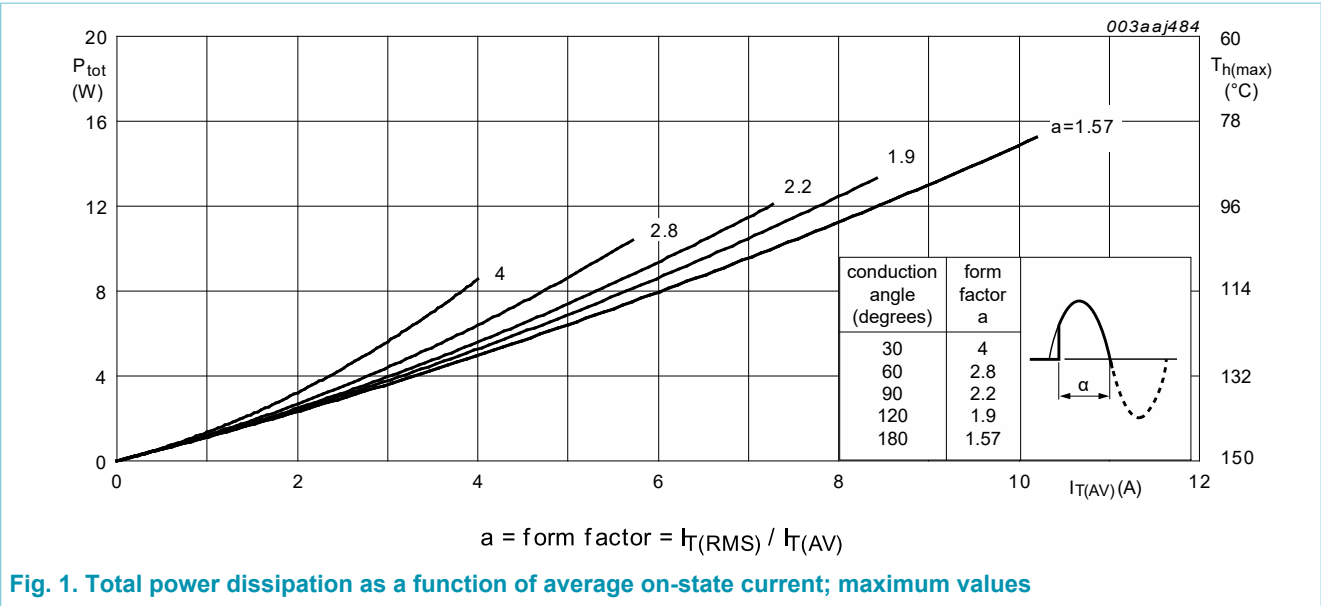
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
TYN16X-600CT	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values  
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	600	V
$V_{RRM}$	repetitive peak reverse voltage		-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_h \leq 81\text{ }^{\circ}\text{C}$ ; Fig. 1	-	10.2	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_h \leq 81\text{ }^{\circ}\text{C}$ ; Fig. 2; Fig. 3	-	16	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 10\text{ ms}$ ; Fig. 4; Fig. 5	-	180	A
		half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 8.3\text{ ms}$	-	198	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; SIN	-	162	$\text{A}^2\text{s}$
$di_T/dt$	rate of rise of on-state current	$I_T = 40\text{ A}$ ; $I_G = 200\text{ mA}$ ; $di_G/dt = 200\text{ mA}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
$I_{GM}$	peak gate current		-	4	A
$V_{RGM}$	peak reverse gate voltage		-	5	V
$P_{GM}$	peak gate power		-	10	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	1	W
$T_{stg}$	storage temperature		-40	150	$^{\circ}\text{C}$
$T_j$	junction temperature		-	150	$^{\circ}\text{C}$



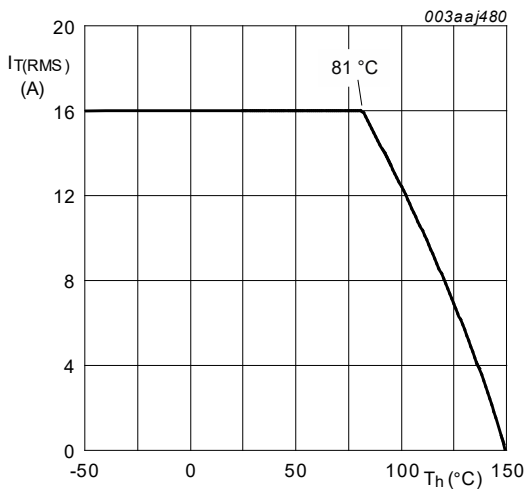
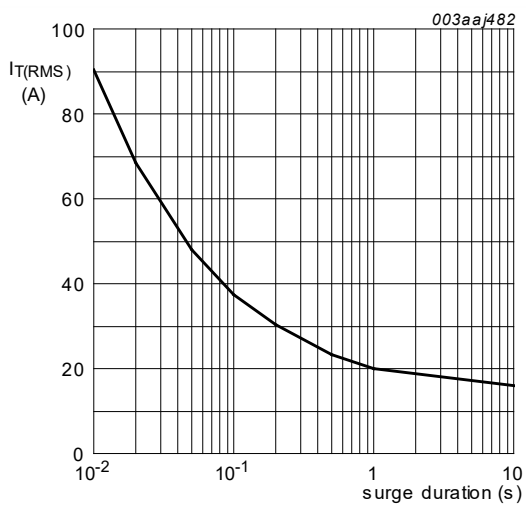
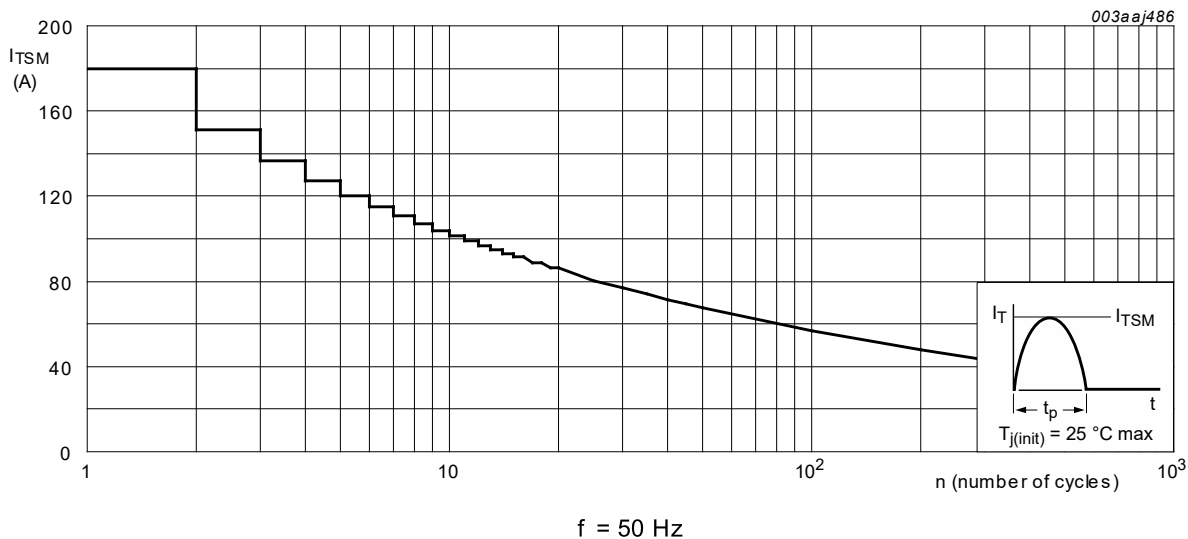


Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values



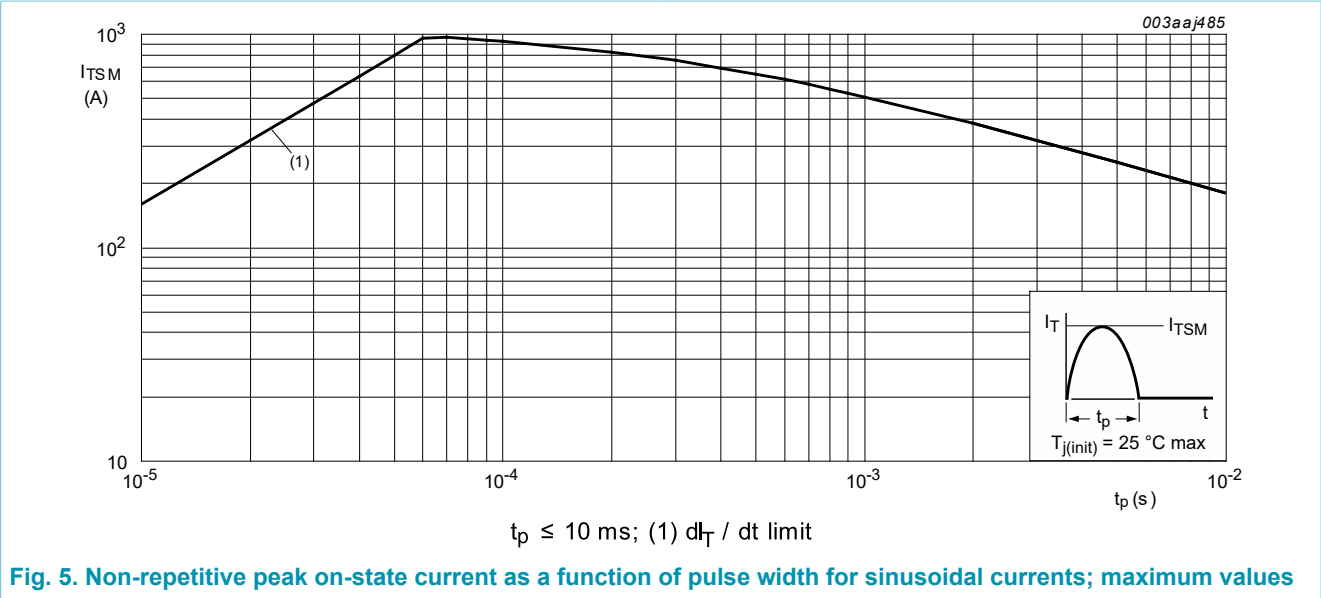
$f = 50 \text{ Hz}; T_h = 81 \text{ °C}$

Fig. 3. RMS on-state current as a function of surge duration; maximum values



$f = 50 \text{ Hz}$

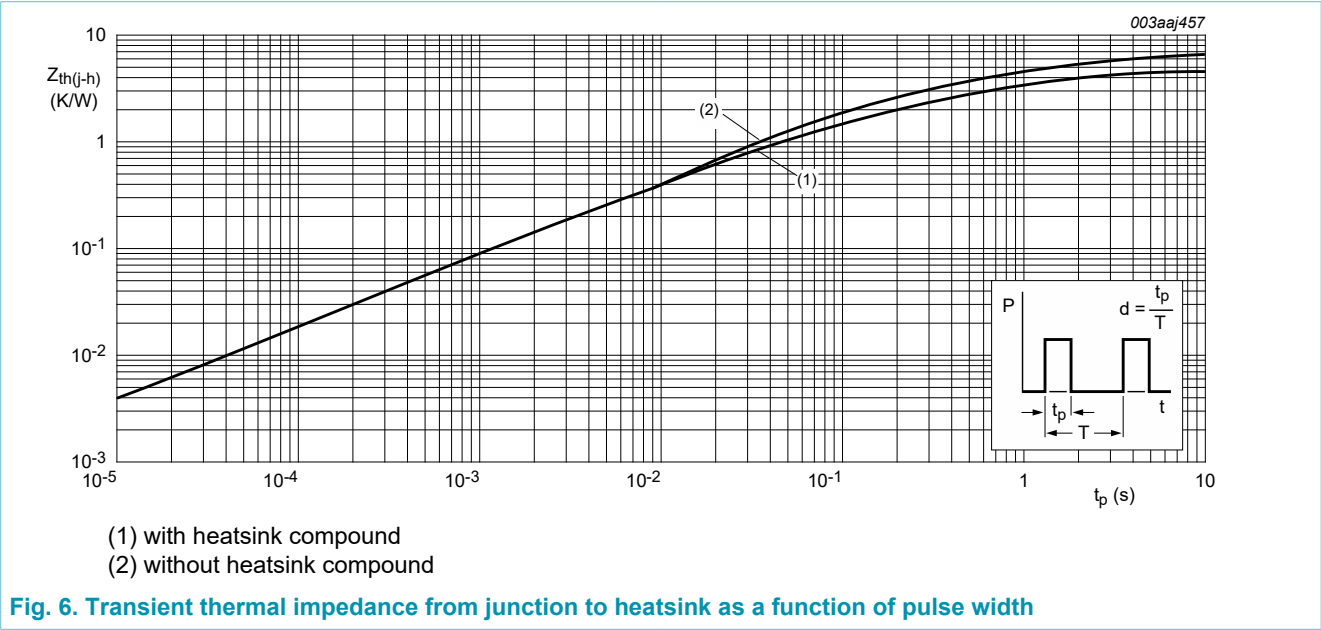
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; Fig. 6	-	-	4.5	K/W
		without heatsink compound; Fig. 6	-	-	6.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	55	-	K/W



9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T <sub>h</sub> = 25 °C	-	-	2500	V
$C_{isol}$	isolation capacitance	from anode to external heatsink; f = 1 MHz; T <sub>h</sub> = 25 °C	-	10	-	pF

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 7	-	-	15	mA
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 8	-	-	60	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 9	-	-	40	mA
$V_T$	on-state voltage	$I_T = 32\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 10	-	1.2	1.6	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 11	-	0.7	1.3	V
		$V_D = 400\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 150\text{ }^\circ\text{C}$ ; Fig. 11	0.2	0.4	-	V
$I_D$	off-state current	$V_D = 600\text{ V}$ ; $T_j = 150\text{ }^\circ\text{C}$	-	0.2	1	mA
$I_R$	reverse current	$V_R = 600\text{ V}$ ; $T_j = 150\text{ }^\circ\text{C}$	-	0.2	1	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$ ; $T_j = 150\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit	500	-	-	V/ $\mu\text{s}$
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 40\text{ A}$ ; $V_D = 600\text{ V}$ ; $I_G = 100\text{ mA}$ ; $dI_G/dt = 5\text{ A}/\mu\text{s}$ ; $T_j = 25\text{ }^\circ\text{C}$	-	2	-	$\mu\text{s}$
$t_q$	commutated turn-off time	$V_{DM} = 402\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $I_{TM} = 20\text{ A}$ ; $V_R = 25\text{ V}$ ; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$ ; $dV_D/dt = 50\text{ V}/\mu\text{s}$ ; $R_{GK(ext)} = 100\text{ }\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ )	-	70	-	$\mu\text{s}$

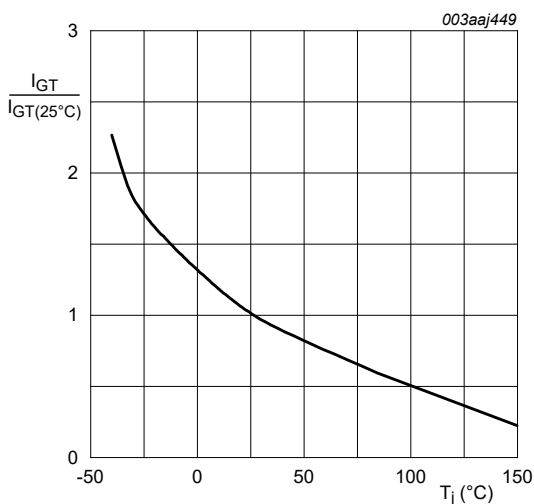


Fig. 7. Normalized gate trigger current as a function of junction temperature

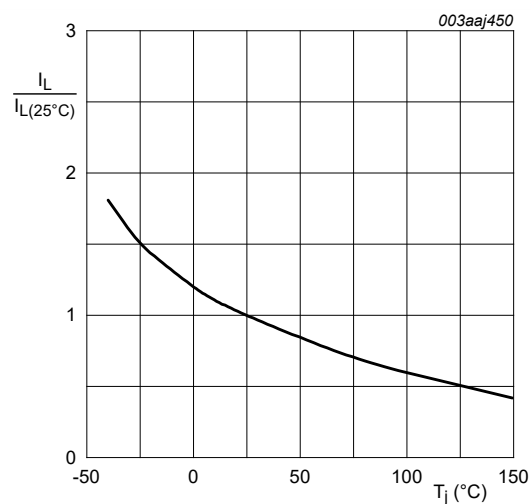


Fig. 8. Normalized latching current as a function of junction temperature

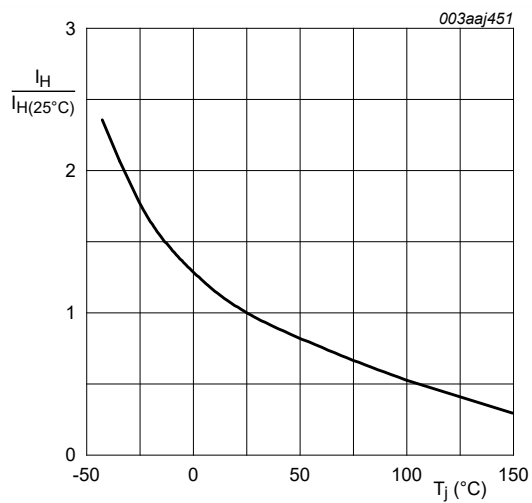


Fig. 9. Normalized holding current as a function of junction temperature

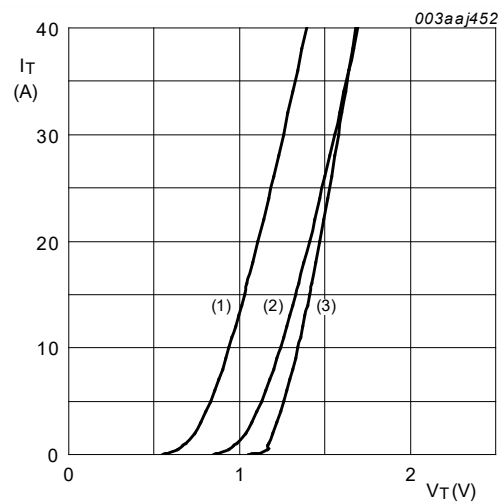


Fig. 10. On-state current as a function of on-state voltage

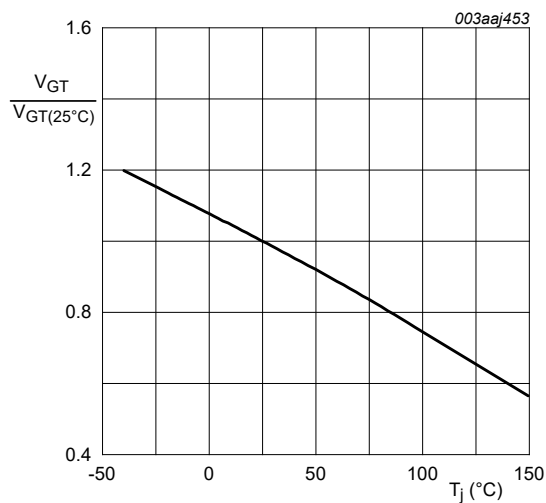


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

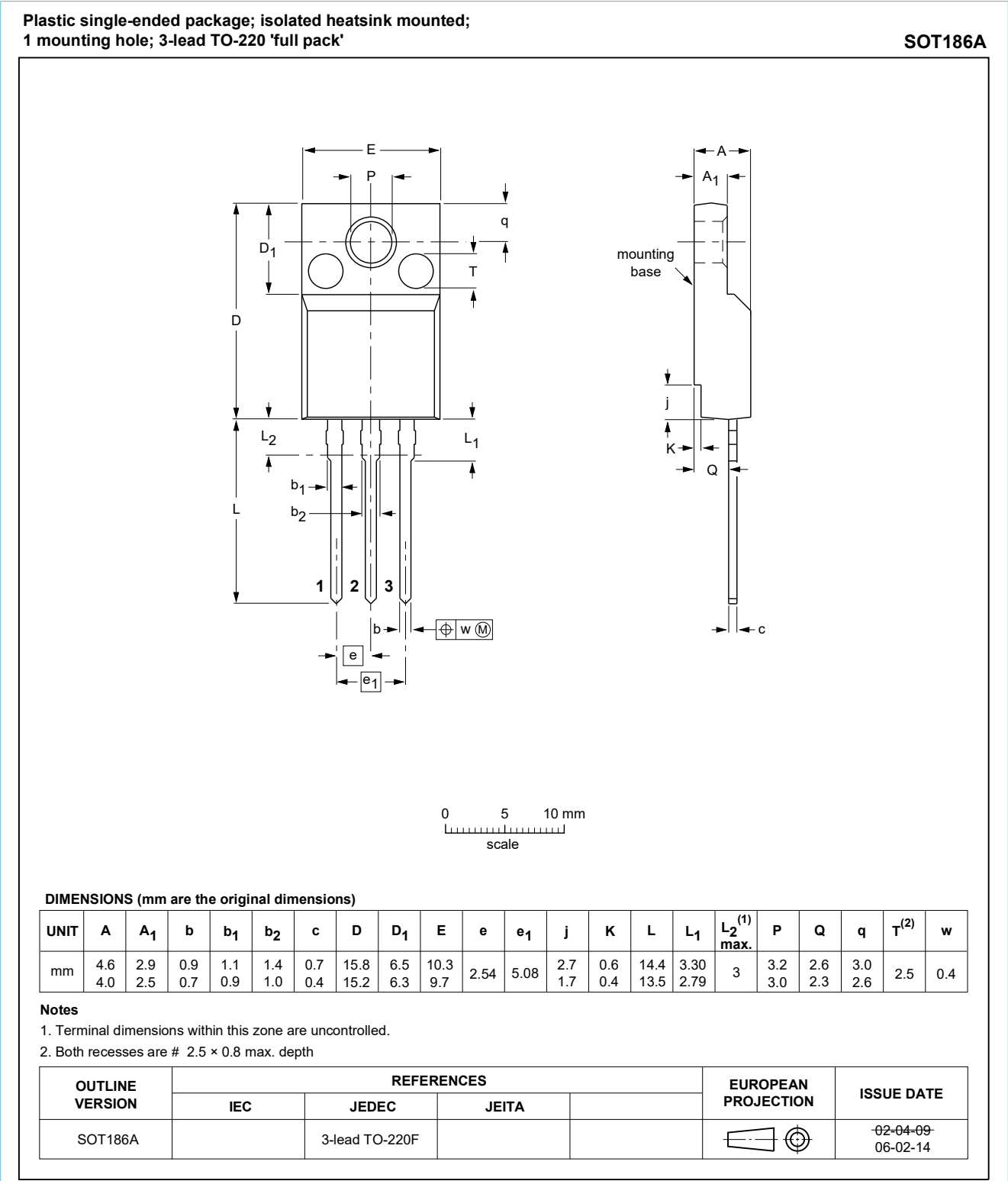


Fig. 12. Package outline TO-220F (SOT186A)

## 12. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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