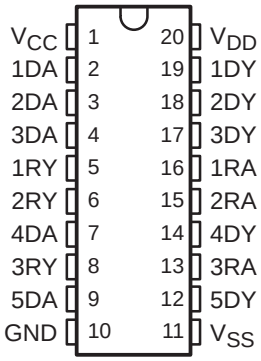
- **Single Chip With Easy Interface Between UART and Serial-Port Connector of an External Modem or Other Computer Peripheral**
- **Five Drivers and Three Receivers Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28**
- **Designed to Support Data Rates up to 120 kbit/s**
- **ESD Protection Meets Or Exceeds 10 kV on RS-232 Pins and 5 kV on All Other Pins (Human-Body Model)**
- **Complement to the SN75185**
- **Pin-to-Pin Replacement for the Goldstar GD75323**
- **Functional Replacement for the MC145405**

DW OR N PACKAGE
(TOP VIEW)



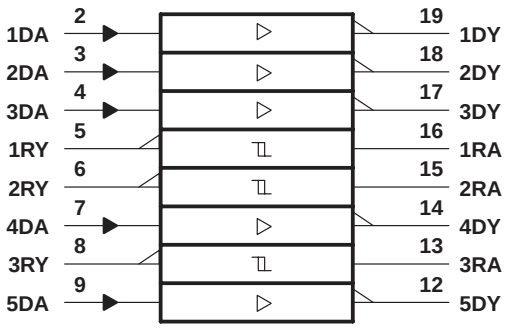
description

The SN75196 combines five drivers and three receivers from the trade-standard SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The flow-through design of the SN75196 decreases the part count, reduces the board space required, and allows easy interconnection of the UART and serial-port connector. The all-bipolar circuits and processing of the SN75196 provide a rugged, low-cost solution for this function.

The SN75196 complies with the requirements of TIA/EIA-232-F and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and peripheral at signal rates of up to 20 kbit/s. The switching speeds of the SN75196 are fast enough to support rates of up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates of up to 120 kbit/s, use of TIA/EIA-423-B (ITU V.10) and TIA/EIA-422-B (ITU V.11) standards are recommended.

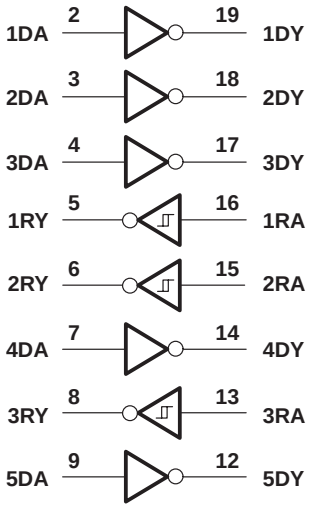
The SN75196 is characterized for operation over a temperature range of 0°C to 70°C.

logic symbol†

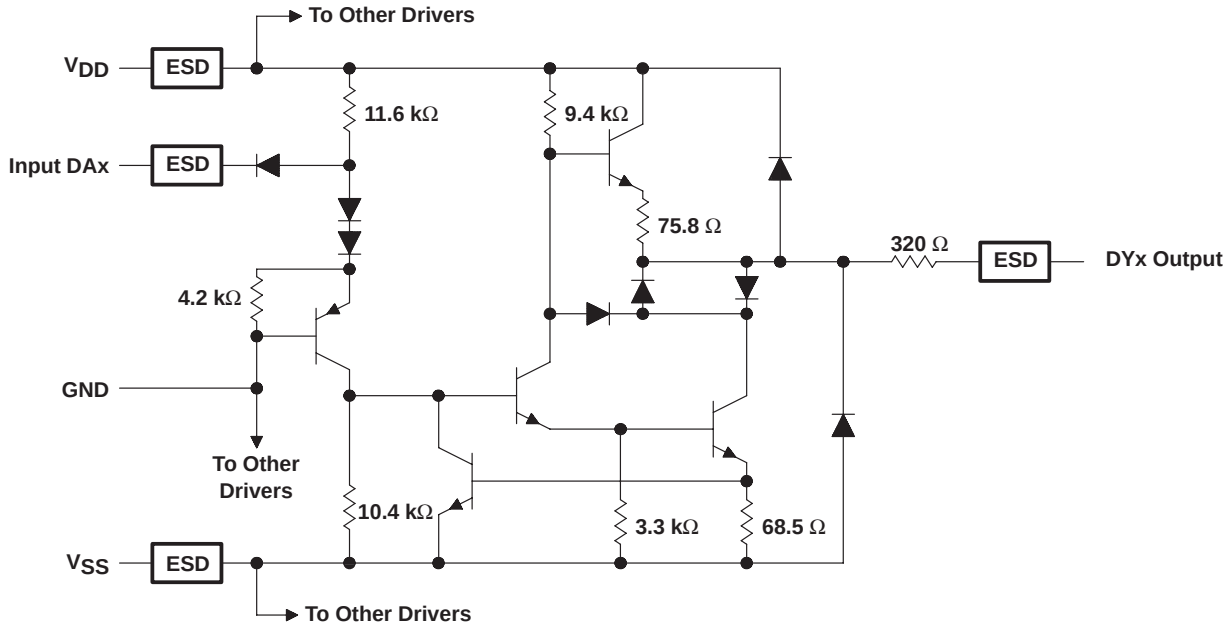


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

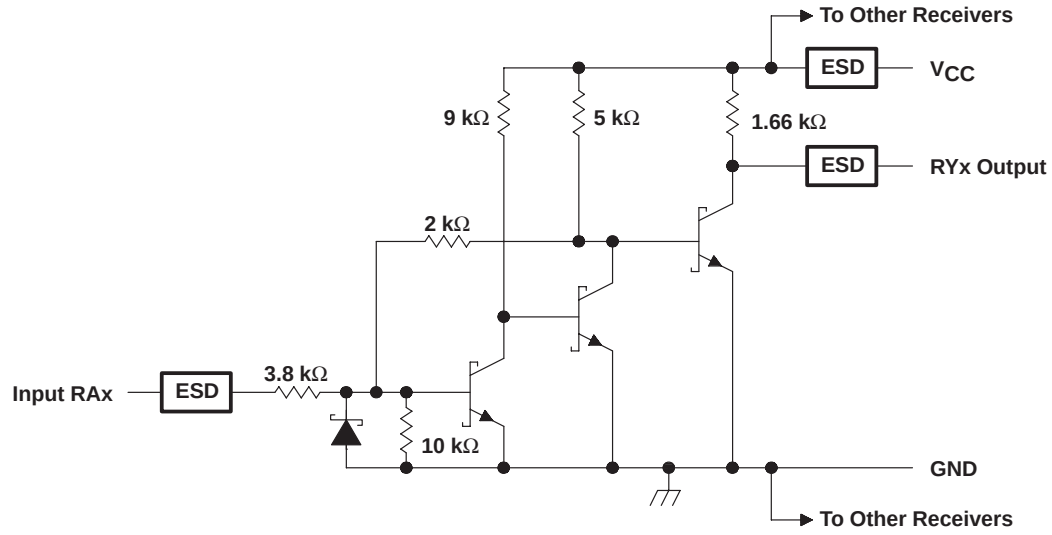


schematic of each driver



Resistor values shown are nominal.

schematic of each receiver



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 10 V
Supply voltage, V_{DD} (see Note 1) . . . . . 15 V
Supply voltage, V_{SS} (see Note 1) . . . . . –15 V
Input voltage range, V_I: Driver . . . . . –15 V to 7 V
Receiver . . . . . –30 V to 30 V
Output voltage range, V_O (Driver) . . . . . – 15 V to 15 V
Low-level output current, I_{OL} (Receiver) . . . . . 20 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Electrostatic discharge: DY and RA to GND (see Note 2) . . . . . Class 3, A: 10 kV, B: 500 V
All pins (see Note 2) . . . . . Class 3, A: 5 kV, B: 300 V
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to the network ground terminal.
2. Per MIL-PRF-38535, Method 3015.7

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

‡ This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		7.5	9	13.5	V
Supply voltage, V_{SS}		–7.5	–9	–13.5	V
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	Driver	1.9			V
Low-level input voltage, V_{IL}	Driver			0.8	V
High-level output current, I_{OH}	Driver			–6	mA
	Receiver			–0.5	
High-level output current, I_{OL}	Driver			6	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C

supply currents over operating free-air temperature range

PARAMETER		TEST CONDITIONS				MIN	MAX	UNIT
I_{DD}	Supply current from V_{DD}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = –9 V		25	mA
				V_{DD} = 12 V,	V_{SS} = –12 V		32	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = –9 V		7.5	
				V_{DD} = 12 V,	V_{SS} = –12 V		9.5	
I_{SS}	Supply current from V_{SS}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = –9 V		–25	mA
				V_{DD} = 12 V,	V_{SS} = –12 V		–32	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = –9 V		–5.3	
				V_{DD} = 12 V,	V_{SS} = –12 V		–5.3	
I_{CC}	Supply current from V_{CC}	V_{CC} = 5 V,	All inputs at 5 V,	No load			20	mA

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 9 V, V_{SS} = –9 V, V_{CC} = 5 V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	R_L = 3 kΩ,	See Figure 1	6	7.5		V
V_{OL}	Low-level output voltage (see Note 3)	V_{IH} = 1.9 V,	R_L = 3 kΩ,	See Figure 1		–7.5	–6	V
I_{IH}	High-level input current	V_I = 5 V,	See Figure 2				10	μA
I_{IL}	Low-level input current	V_I = 0,	See Figure 2				–1.6	mA
$I_{OS(H)}$	High-level short-circuit output current (see Note 4)	V_{IL} = 0.8 V,	V_O = 0,	See Figure 1	–4.5	–9	–19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current (see Note 4)	V_{IH} = 2 V,	V_O = 0,	See Figure 1	4.5	9	19.5	mA
r_o	Output resistance (see Note 5)	V_{CC} = V_{DD} = V_{SS} = 0,		V_O = –2 V to 2 V	300			Ω

NOTES: 3. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if –10 V is a maximum, the typical value is a more negative voltage.
4. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
5. Test conditions are those specified by TIA/EIA-232-F and as listed above.

switching characteristics, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ±10%, T_A = 25°C

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF,	See Figure 3			315	500	ns
t_{PHL}	Propagation delay time, high- to low-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF,	See Figure 3			75	175	ns
t_{TLH}	Transition time, low- to high-level output (see Note 6)	R_L = 3 kΩ to 7 kΩ	C_L = 15 pF,	See Figure 3			60	100	ns
			C_L = 2500 pF,	See Figure 3 and Note 6			1.7	2.5	μs
t_{THL}	Transition time, high- to low-level output (see Note 7)	R_L = 3 kΩ to 7 kΩ	C_L = 15 pF,	See Figure 3			40	75	ns
			C_L = 2500 pF,	See Figure 3 and Note 7			1.5	2.5	μs

NOTES: 6. Measured between –3-V and 3-V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied either high or low.
7. Measured between 3-V and –3-V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied either high or low.

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Figure 5	T_A = 25°C		1.75	1.9	2.3	V
			T_A = 0°C to 70 °C		1.55		2.3	
$V_{IT–}$	Negative-going input threshold voltage	See Figure 5			0.75	0.97	1.25	V
V_{hys}	Input hysteresis ($V_{IT+} – V_{IT–}$)	See Figure 5			0.5			V
V_{OH}	High-level output voltage	I_{OH} = –0.5 mA,	See Figure 5	V_{IH} = 0.75 V	2.6	4	5	V
				Inputs open	2.6			
V_{OL}	Low-level input voltage	I_{OL} = 10 mA,	V_I = 3 V,	See Figure 5		0.2	0.45	V
I_{IH}	High-level input current	V_I = 25 V			3.6		8.3	mA
		V_I = 3 V			0.43			
I_{IL}	Low-level input current	V_I = –25 V			–3.6		–8.3	mA
		V_I = –3 V			–0.43			
I_{OS}	Short-circuit output current	See Figure 4				–3.4	–12	mA

† All typical values are at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 9 V, and V_{SS} = –9 V.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF,	R_L = 5 kΩ,	See Figure 6		107	500	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 50 pF,	R_L = 5 kΩ,	See Figure 6		42	150	ns
t_{TLH}	Transition time, low- to high-level output	C_L = 50 pF,	R_L = 5 kΩ,	See Figure 6		175	525	ns
t_{THL}	Transition time, high- to low-level output	C_L = 50 pF,	R_L = 5 kΩ,	See Figure 6		16	60	ns

PARAMETER MEASUREMENT INFORMATION

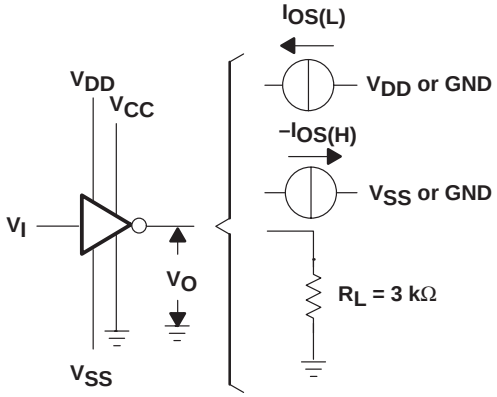


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

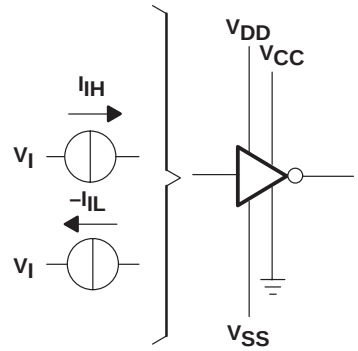
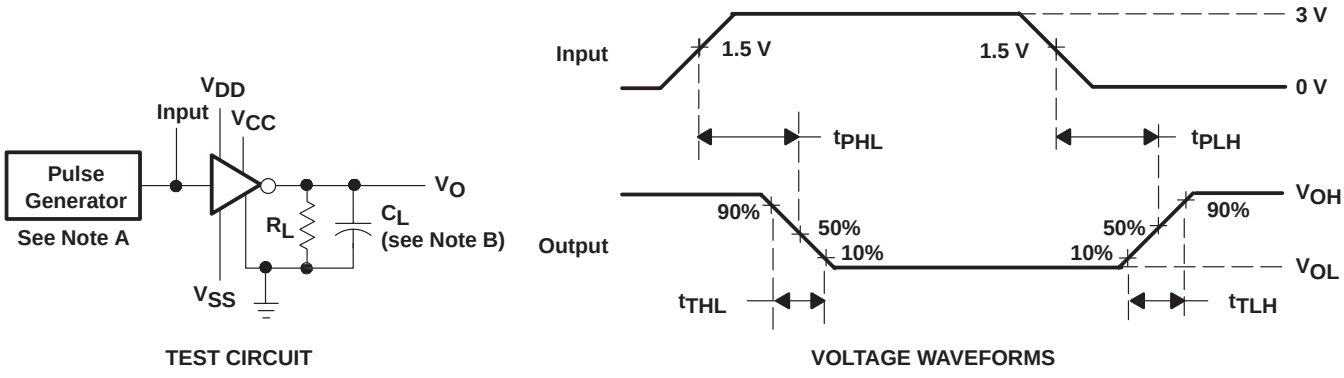


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



NOTES: A. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

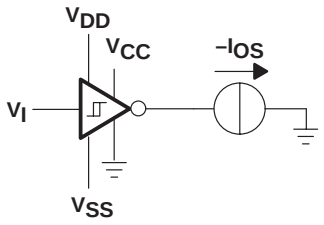


Figure 4. Receiver Test Circuit for I_{OS}

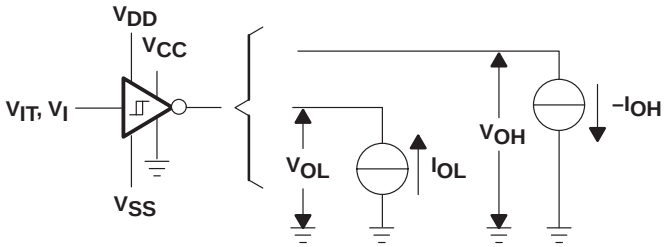
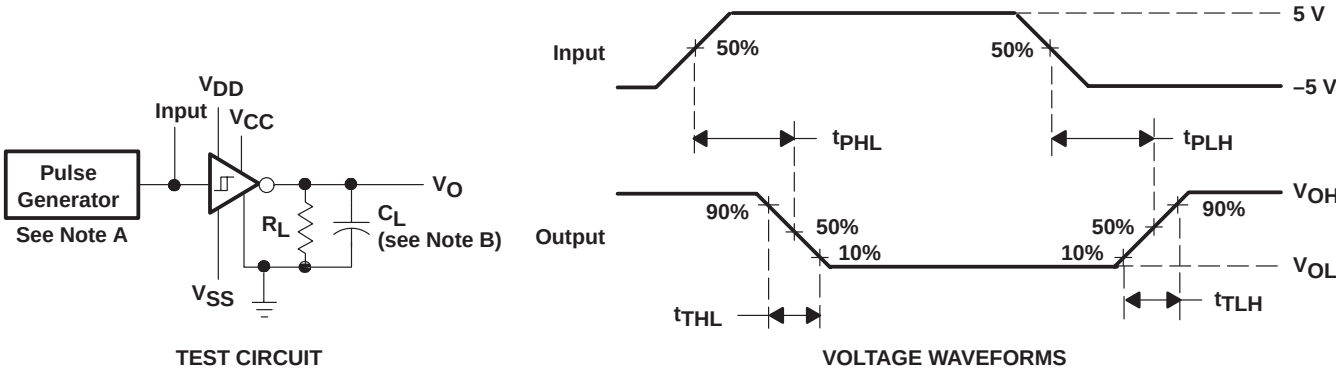


Figure 5. Receiver Test Circuit for V_{IT}, V_{OH}, and V_{OL}



NOTES: A. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER SECTION

VOLTAGE TRANSFER CHARACTERISTICS

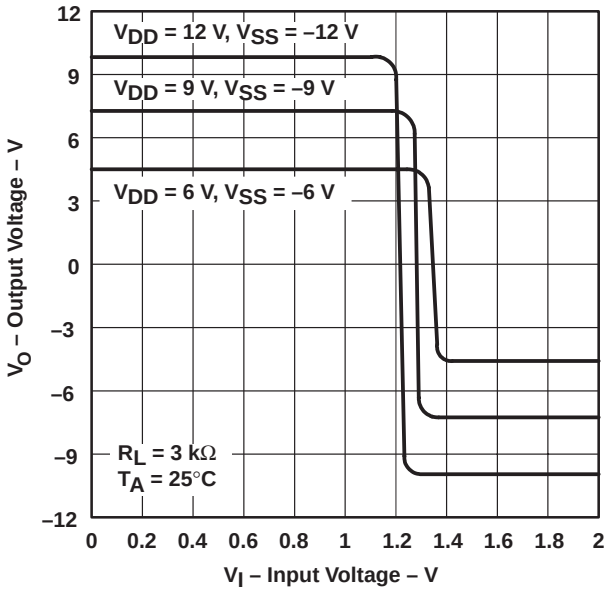


Figure 7

OUTPUT CURRENT vs OUTPUT VOLTAGE

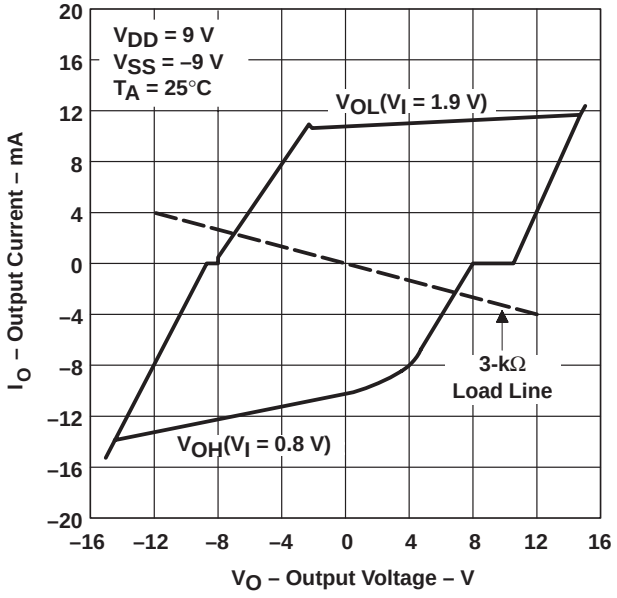


Figure 8

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

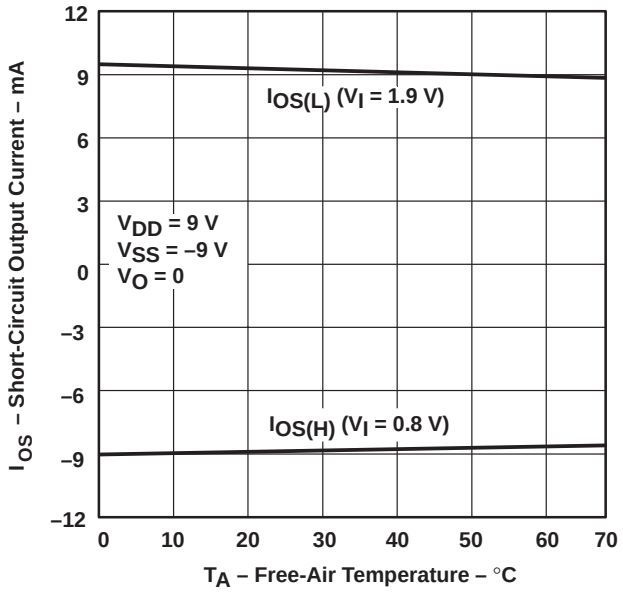


Figure 9

SLEW RATE vs LOAD CAPACITANCE

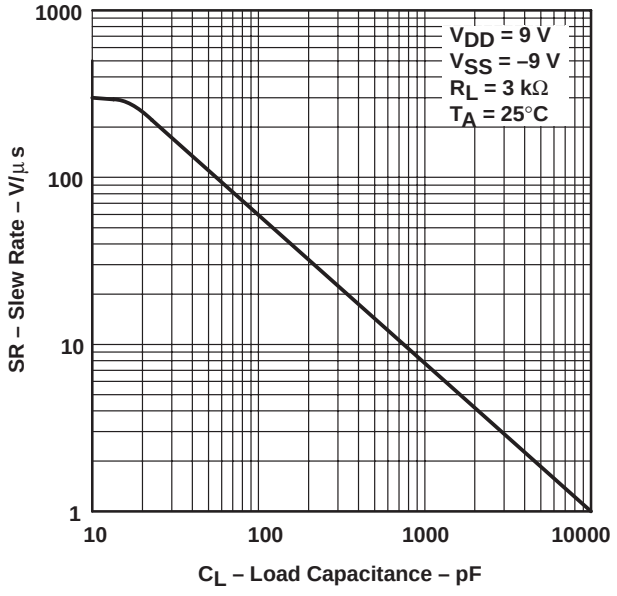


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER SECTION

INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

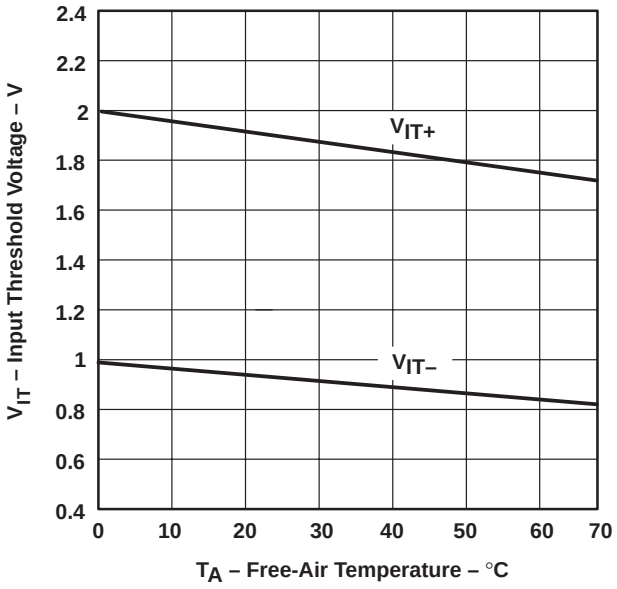


Figure 11

INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

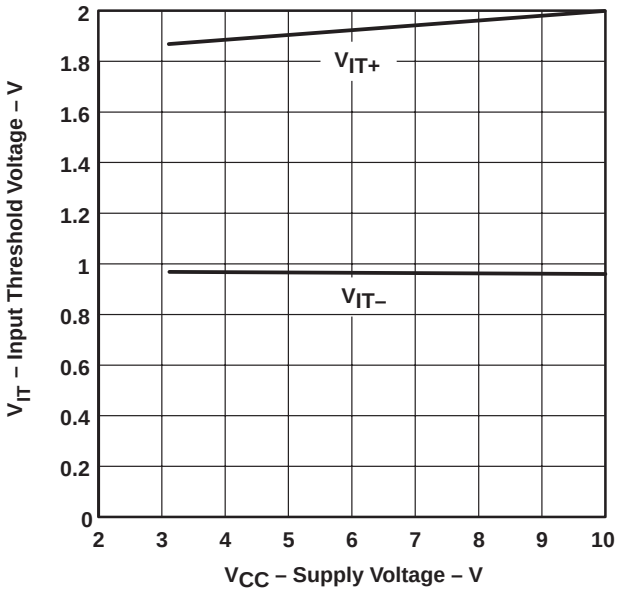
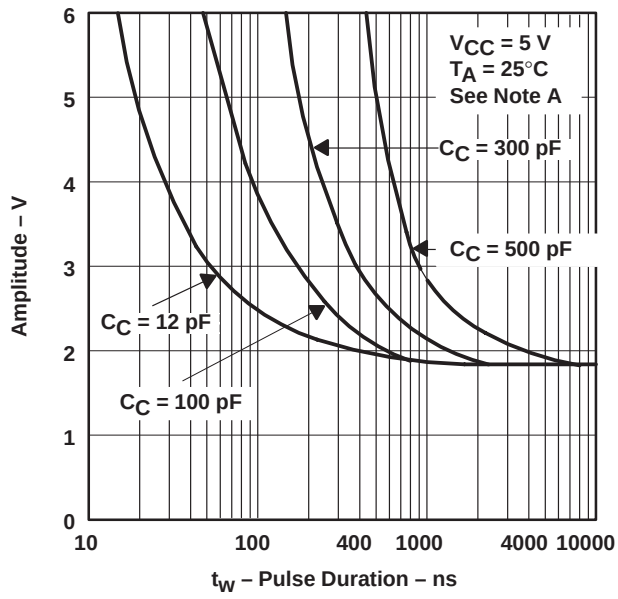


Figure 12

NOISE REJECTION



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, does not cause a change of the output level.

Figure 13

MAXIMUM SUPPLY VOLTAGE vs FREE-AIR TEMPERATURE

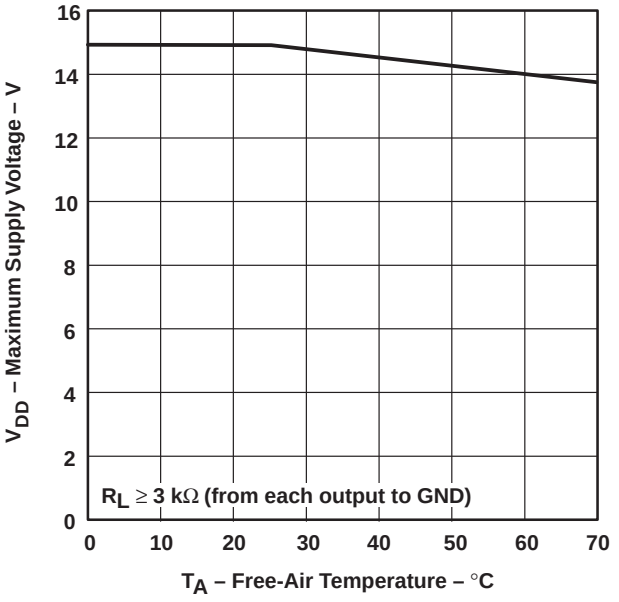


Figure 14

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} terminals protect the SN75196 in the fault condition when the device outputs are shorted to V_{DD} or V_{SS} and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

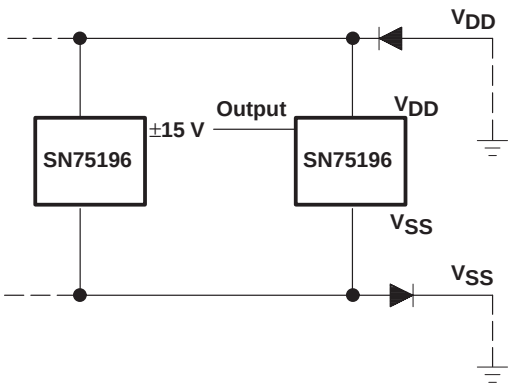
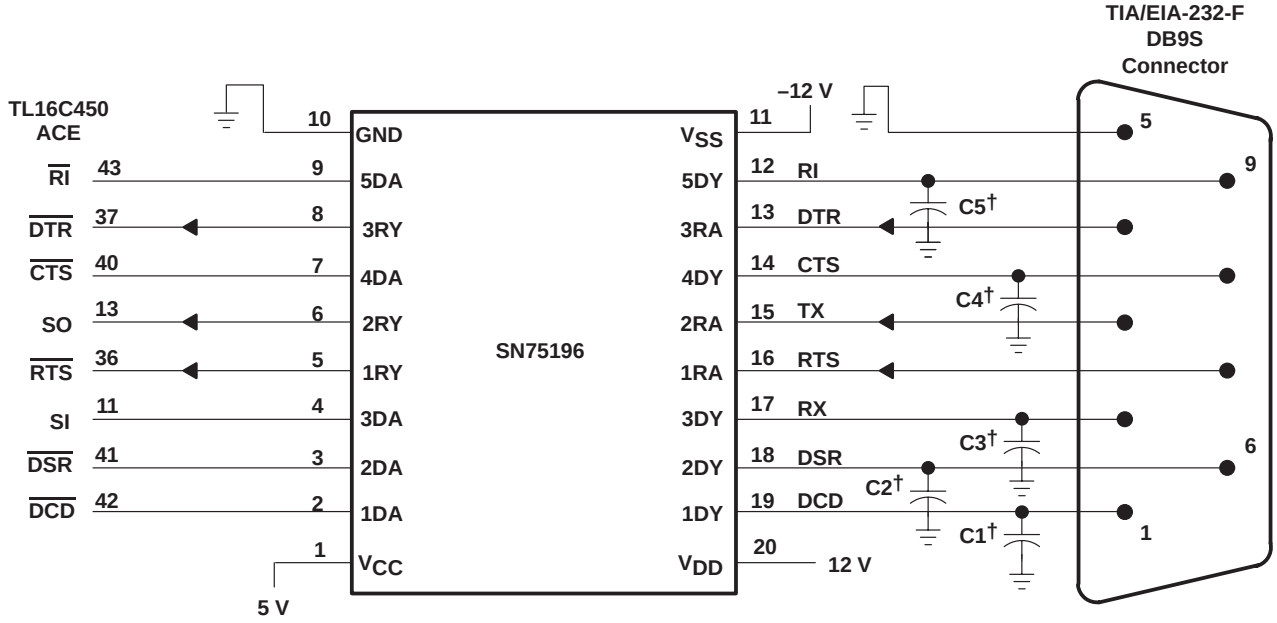


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F



† See Figure 10 to select the correct values for the loading capacitors (C1, C2, C3, C4, and C5), which may be required to meet the RS-232 maximum slew-rate requirement of 30 V/µs. The value of the loading capacitors required depends upon the line length and desired slew rate, but is typically 330 pF.

NOTE A: To use the receivers only, V_{DD} and V_{SS} must both be powered or tied to ground.

Figure 16. Typical TIA/EIA-232-F Connection

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75196DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75196	Samples
SN75196DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75196	Samples
SN75196DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75196	Samples
SN75196N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75196N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

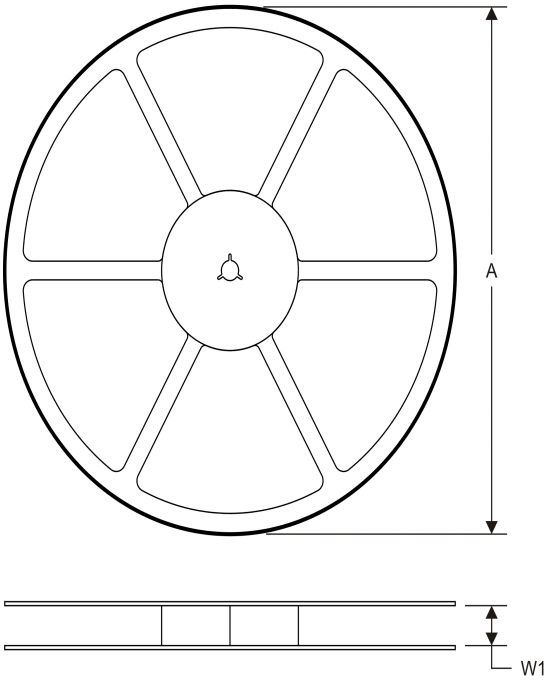
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

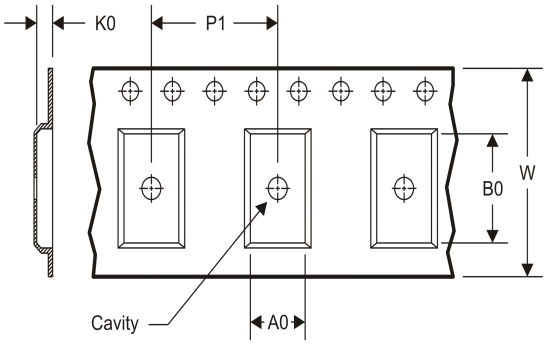
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



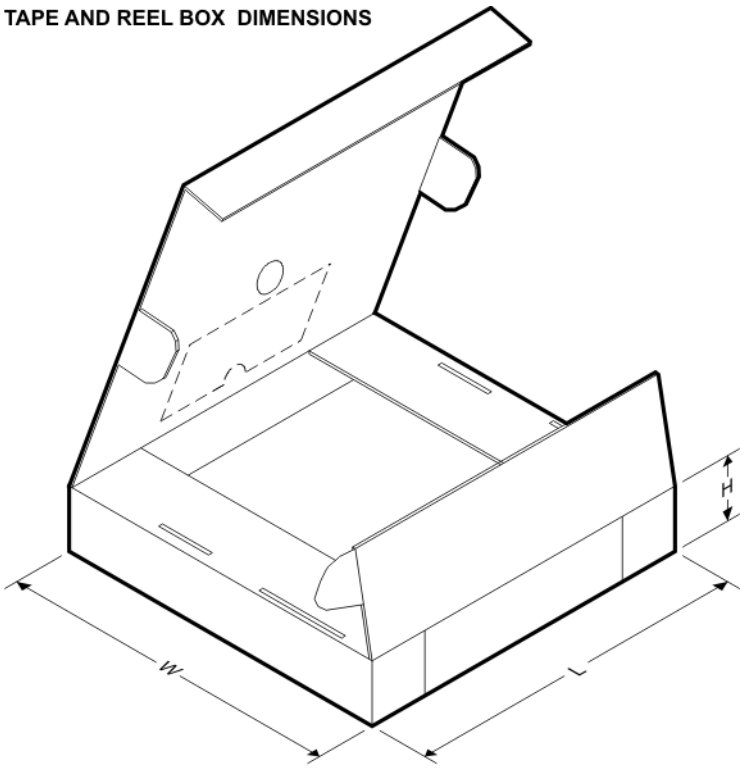
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75196DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



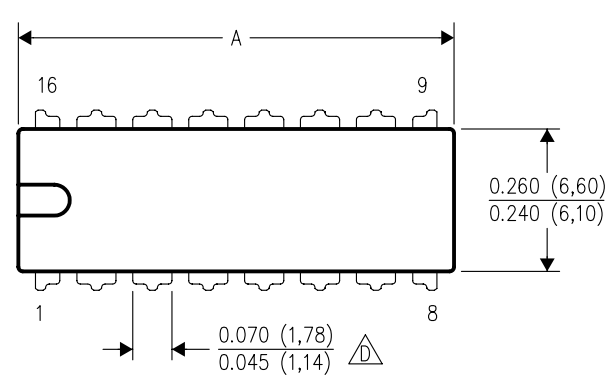
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75196DWR	SOIC	DW	20	2000	367.0	367.0	45.0

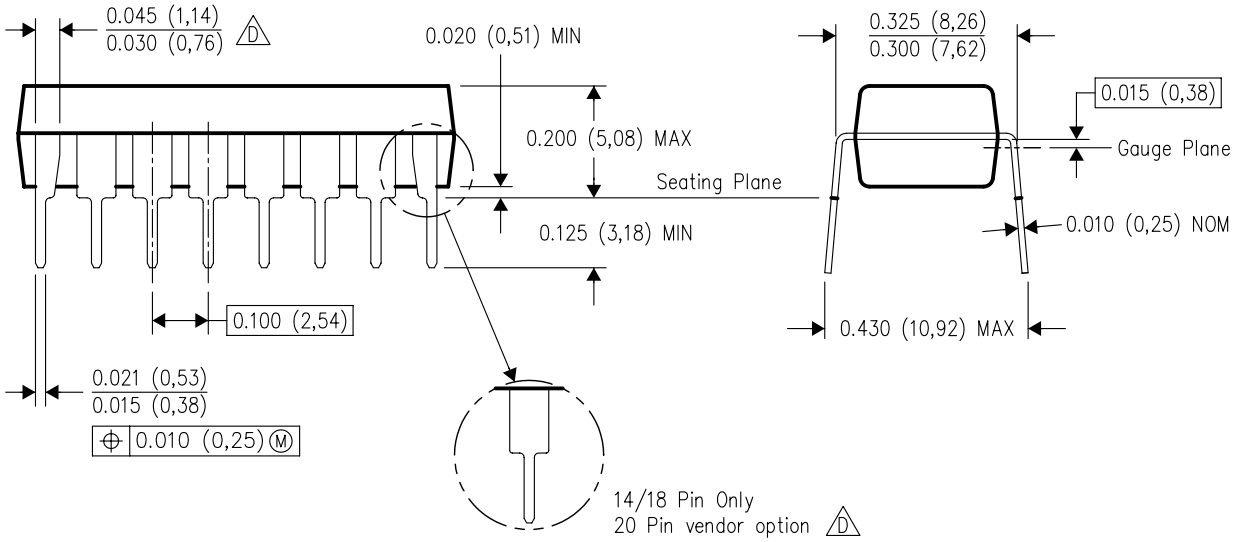
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



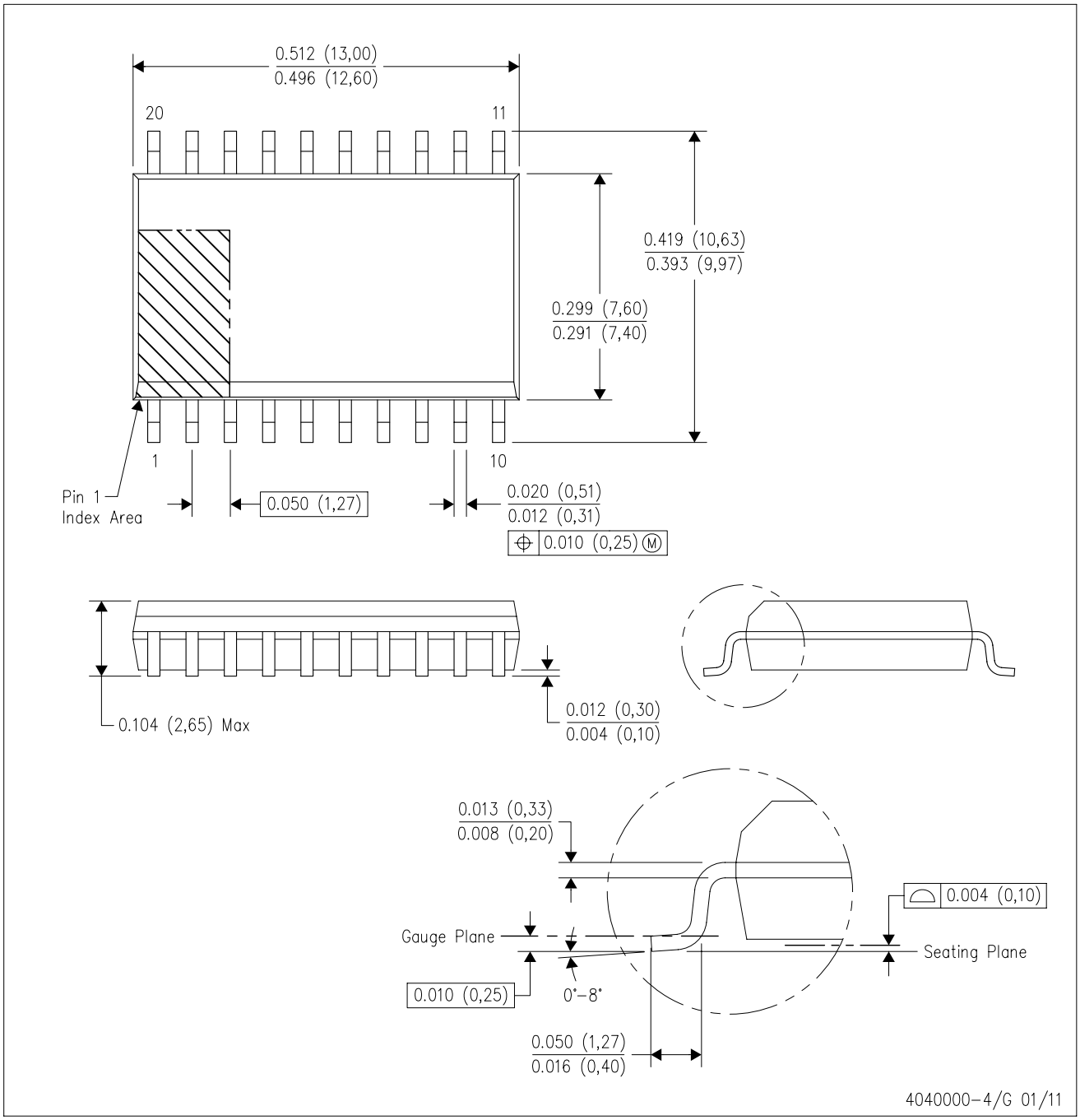
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

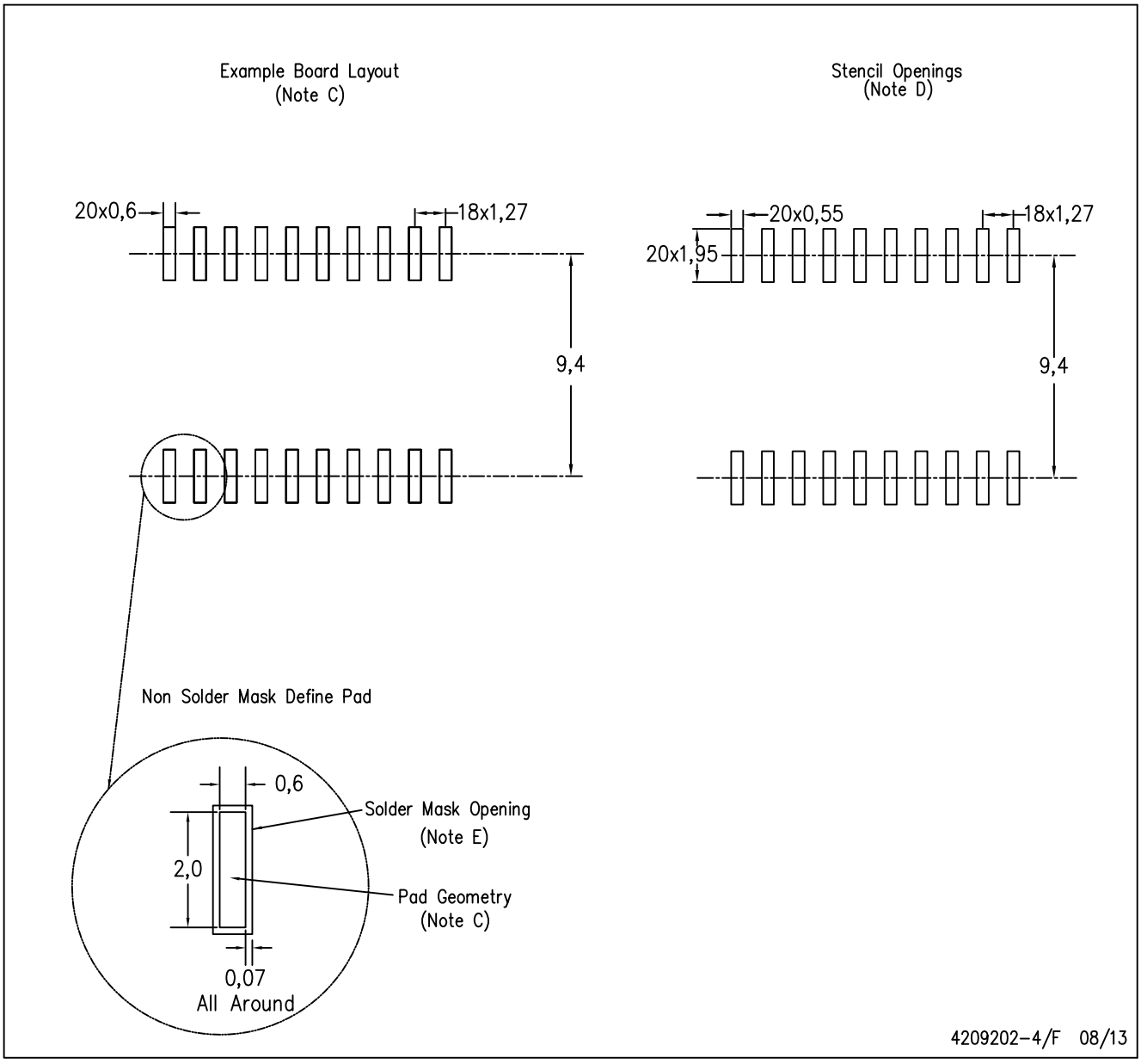
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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