

TC74AC393P,TC74AC393F,TC74AC393FN,TC74AC393FT**Dual Binary Counter**

The TC74AC393 is an advanced high speed CMOS 4-BIT BINARY COUNTER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It contains two independent counter circuits in one package, so that counting or frequency division of eight binary bits can be achieved with one IC.

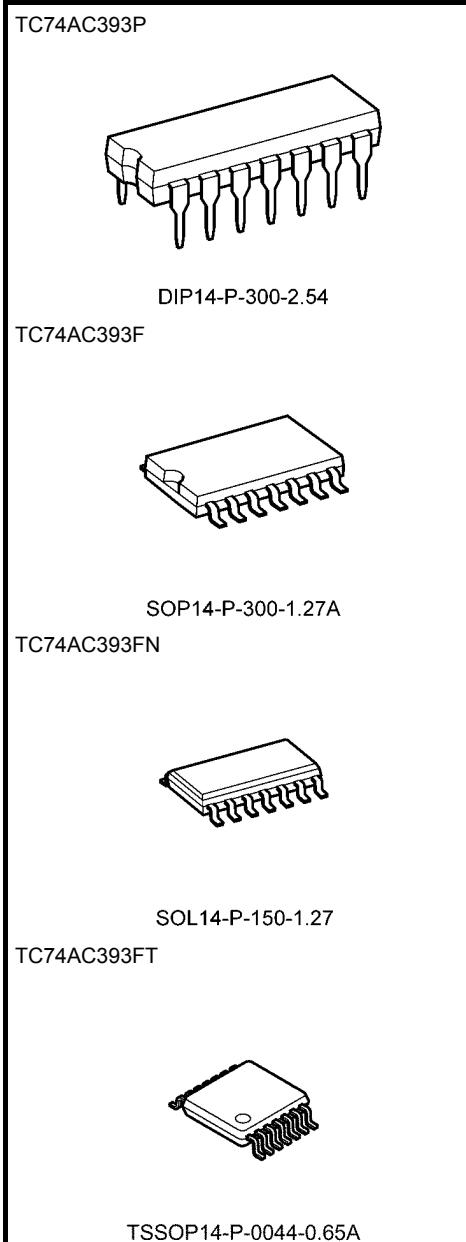
This device changes state on the negative going transition of the CLOCK pulse. The counter can be reset to "0" (QA to QD = "L") by a high at the CLEAR input regardless of other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

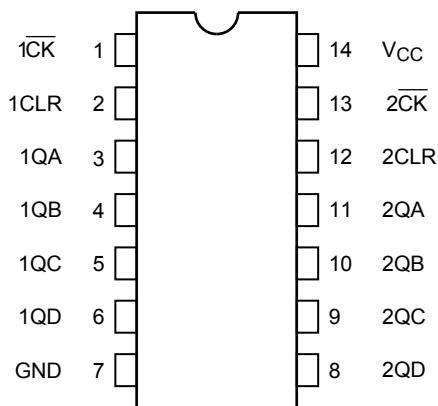
- High speed: $f_{max} = 180$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 8 \mu A$ (max) at $T_a = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 24$ mA (min)
Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 5.5 V
- Pin and function compatible with 74F393

Note: xxxFN (JEDEC SOP) is not available in Japan.



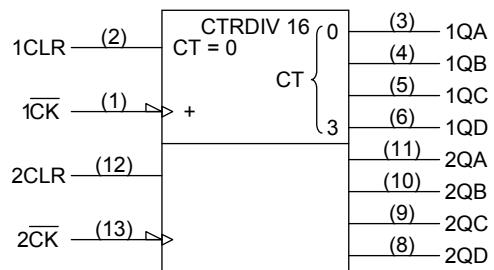
Weight	
DIP14-P-300-2.54	: 0.96 g (typ.)
SOP14-P-300-1.27A	: 0.18 g (typ.)
SOL14-P-150-1.27	: 0.12 g (typ.)
TSSOP14-P-0044-0.65A	: 0.06 g (typ.)

Pin Assignment



(top view)

IEC Logic Symbol

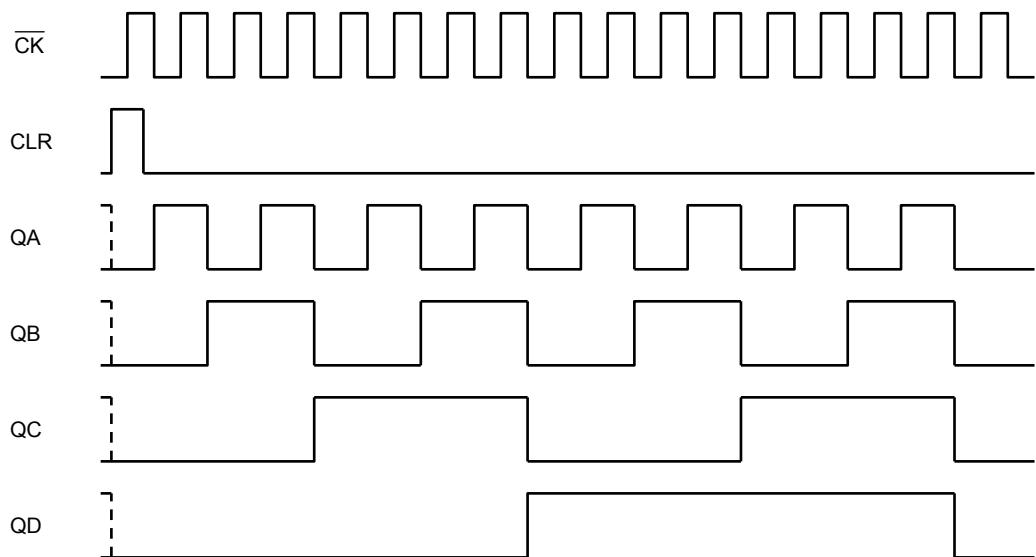


Truth Table

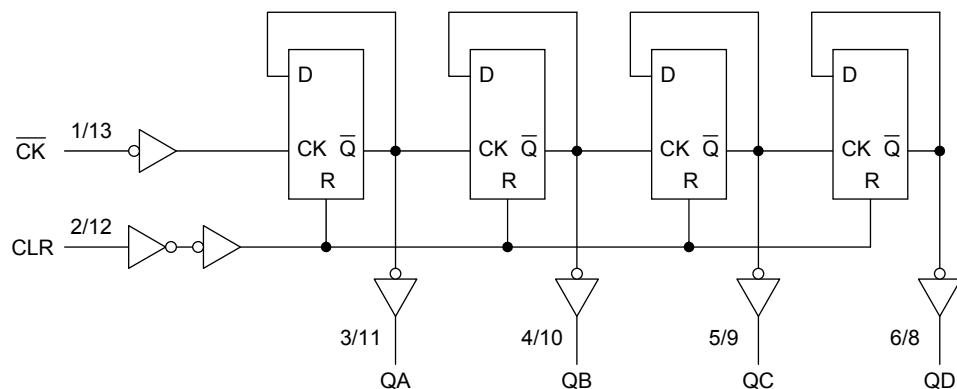
Inputs		Outputs			
\overline{CK}	CLR	QA	QB	QC	QD
X	H	L	L	L	L
	L	Count Up			
	L	No Change			

X: Don't care

Timing Chart



System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5 to 7.0	V
DC input voltage	V _{IN}	-0.5 to V _{CC} + 0.5	V
DC output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}	±20	mA
Output diode current	I _{OK}	±50	mA
DC output current	I _{OUT}	±50	mA
DC V _{CC} /ground current	I _{CC}	±200	mA
Power dissipation	P _D	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	T _{STG}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of $-10 \text{ mW/}^\circ\text{C}$ should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V _{CC} (V)	Ta = 25°C			Ta = -40 to 85°C		Unit	
					Min	Typ.	Max	Min	Max		
High-level input voltage	V _{IH}	—		2.0	1.50	—	—	1.50	—	V	
				3.0	2.10	—	—	2.10	—		
				5.5	3.85	—	—	3.85	—		
Low-level input voltage	V _{IL}	—		2.0	—	—	0.50	—	0.50	V	
				3.0	—	—	0.90	—	0.90		
				5.5	—	—	1.65	—	1.65		
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 µA	2.0	1.9	2.0	—	1.9	—	V	
				3.0	2.9	3.0	—	2.9	—		
				4.5	4.4	4.5	—	4.4	—		
			I _{OH} = -4 mA I _{OH} = -24 mA I _{OH} = -75 mA (Note)	3.0	2.58	—	—	2.48	—		
				4.5	3.94	—	—	3.80	—		
				5.5	—	—	—	3.85	—		
				2.0	—	0.0	0.1	—	0.1		
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 µA	3.0	—	0.0	0.1	—	0.1	V	
				4.5	—	0.0	0.1	—	0.1		
			I _{OL} = 12 mA I _{OL} = 24 mA I _{OL} = 75 mA (Note)	3.0	—	—	0.36	—	0.44		
				4.5	—	—	0.36	—	0.44		
				5.5	—	—	—	—	1.65		
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		5.5	—	—	±0.1	—	±1.0	µA	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	8.0	—	80.0	µA	

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition			V _{CC} (V)	Ta = 25°C		Ta = -40 to 85°C		Unit
						Limit	Limit	Limit	Limit	
Minimum pulse width (CK)	t _w (H) t _w (L)	—			3.3 ± 0.3	7.0	7.0	ns	ns	
					5.0 ± 0.5	5.0	5.0			
Minimum pulse width (CLR)	t _w (H)	—			3.3 ± 0.3	7.0	7.0	ns	ns	
					5.0 ± 0.5	5.0	5.0			
Minimum removal time	t _{rem}	—			3.3 ± 0.3	6.0	6.0	ns	ns	
					5.0 ± 0.5	3.0	3.0			

AC Characteristics ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Ta = 25°C			Ta = -40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
Propagation delay time (\overline{CK} - QA)	t_{pLH}	—	3.3 ± 0.3	—	8.0	13.2	1.0	15.0	ns
	t_{pHL}		5.0 ± 0.5	—	5.0	8.3	1.0	9.5	
Propagation delay time (\overline{CK} - QB)	t_{pLH}	—	3.3 ± 0.3	—	10.1	16.7	1.0	19.0	ns
	t_{pHL}		5.0 ± 0.5	—	5.9	10.5	1.0	12.0	
Propagation delay time (\overline{CK} - QC)	t_{pLH}	—	3.3 ± 0.3	—	12.0	20.2	1.0	23.0	ns
	t_{pHL}		5.0 ± 0.5	—	6.8	12.3	1.0	14.0	
Propagation delay time (\overline{CK} - QD)	t_{pLH}	—	3.3 ± 0.3	—	13.0	23.0	1.0	26.0	ns
	t_{pHL}		5.0 ± 0.5	—	7.5	13.2	1.0	15.0	
Propagation delay time (CLR-Q _n)	t_{pHL}	—	3.3 ± 0.3	—	8.0	13.2	1.0	15.0	ns
			5.0 ± 0.5	—	5.1	8.8	1.0	10.0	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	65	125	—	65	—	MHz
Input capacitance	C_{IN}	—	5.0 ± 0.5	100	160	—	100	—	pF
Power dissipation capacitance	C_{PD}	(Note)			—	36	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

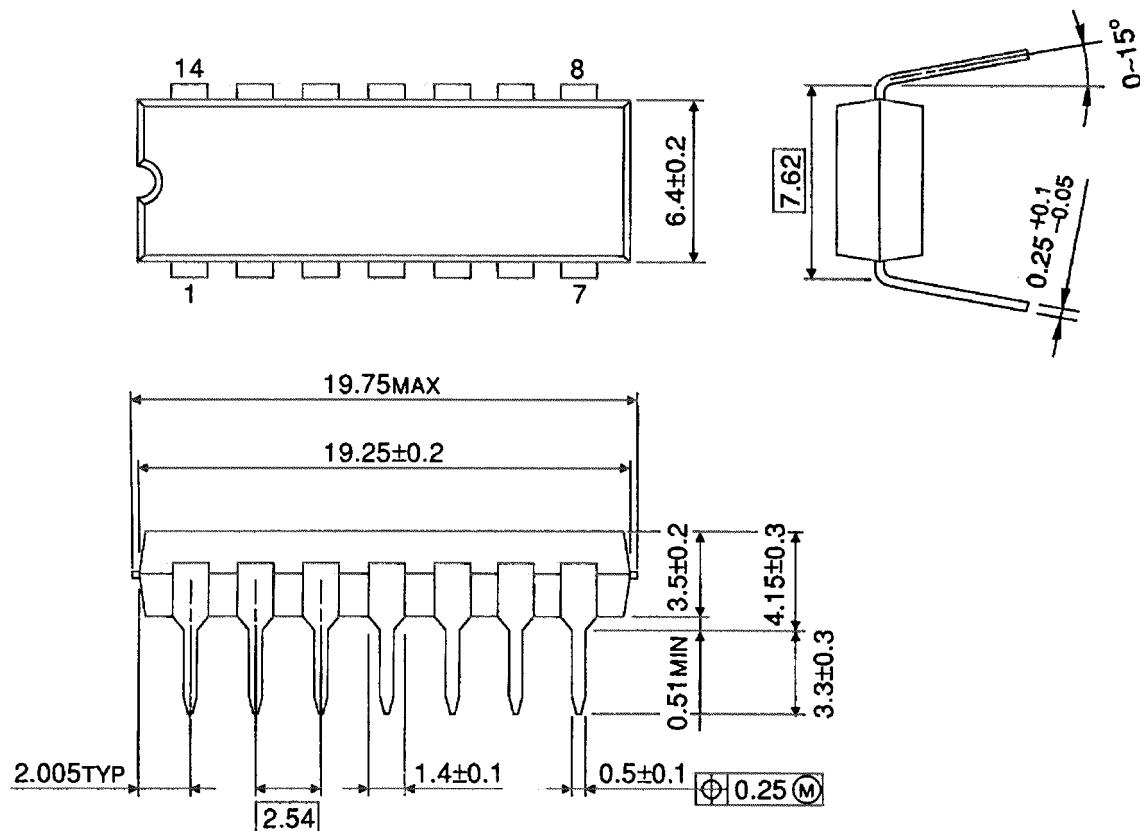
Average operating current can be obtained by the equation:

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per counter)}$$

Package Dimensions

DIP14-P-300-2.54

Unit : mm

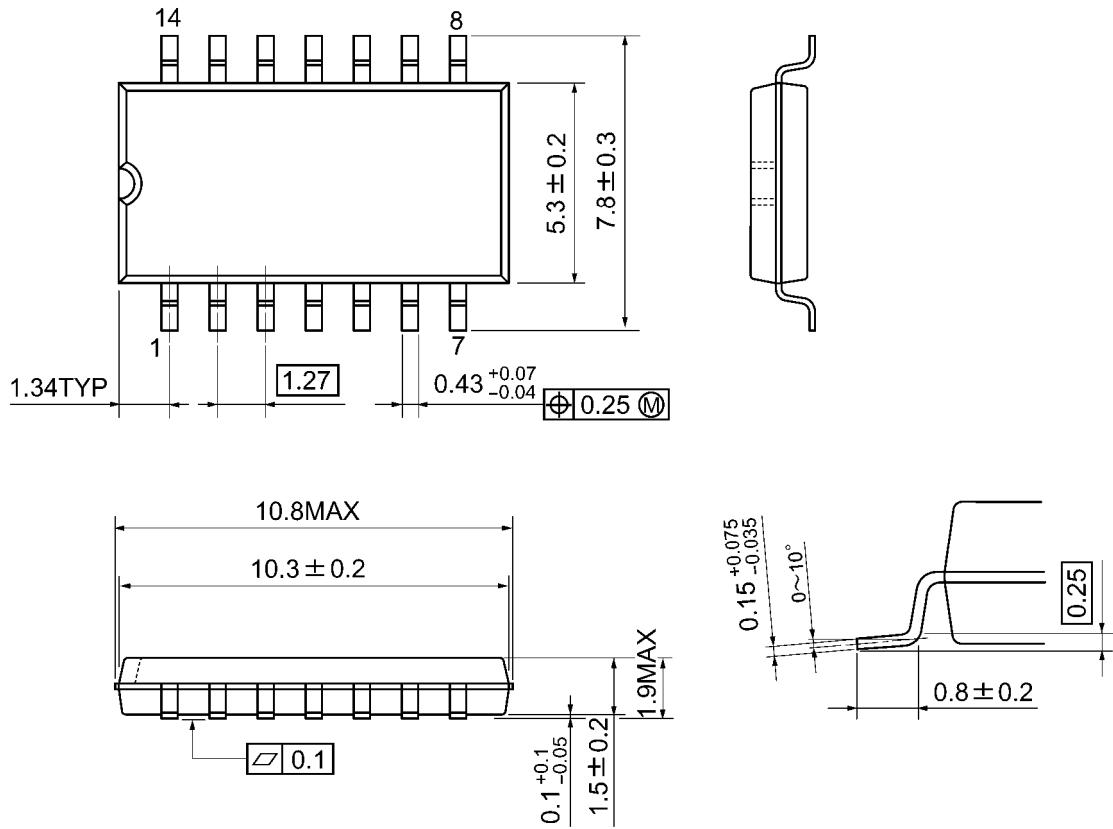


Weight: 0.96 g (typ.)

Package Dimensions

SOP14-P-300-1.27A

Unit: mm

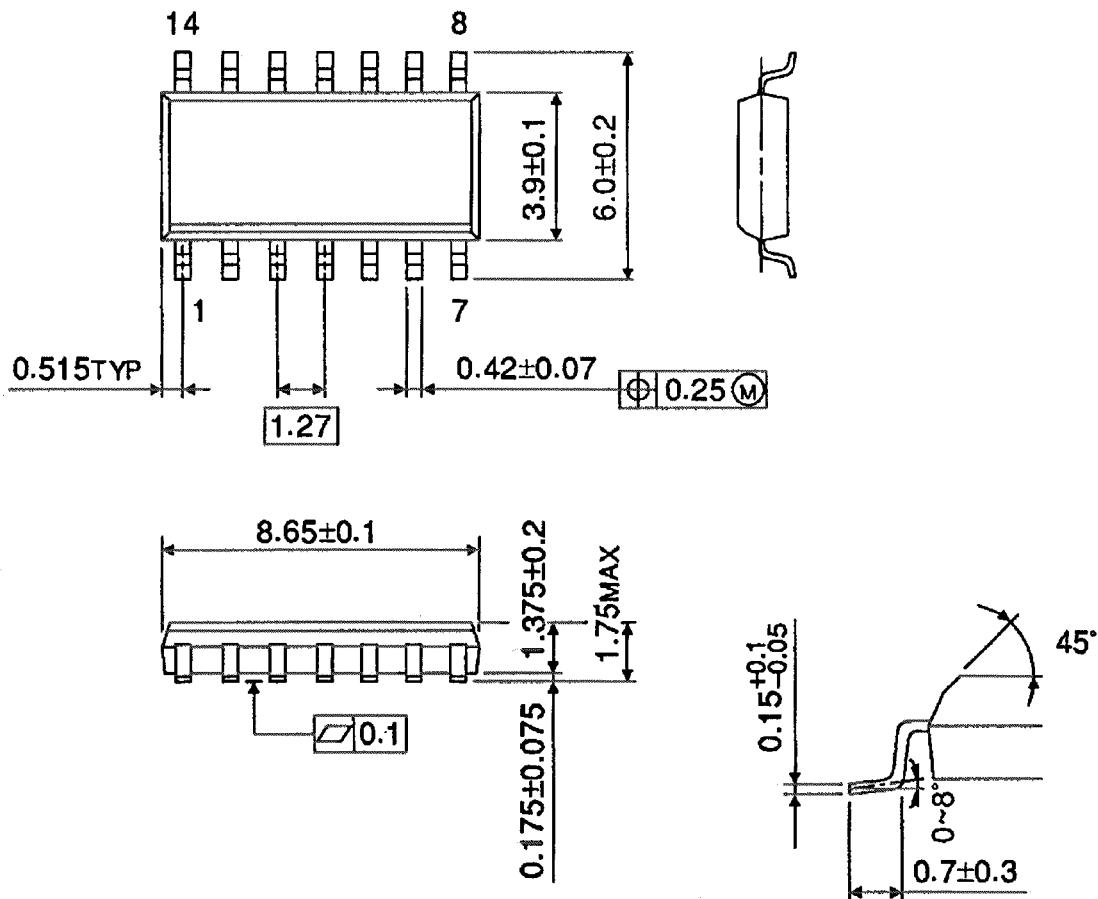


Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL14-P-150-1.27

Unit : mm



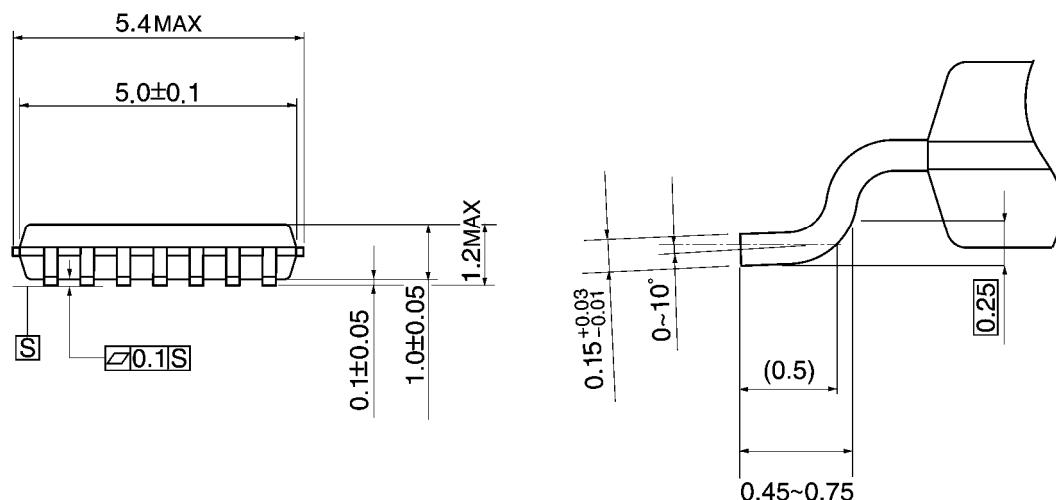
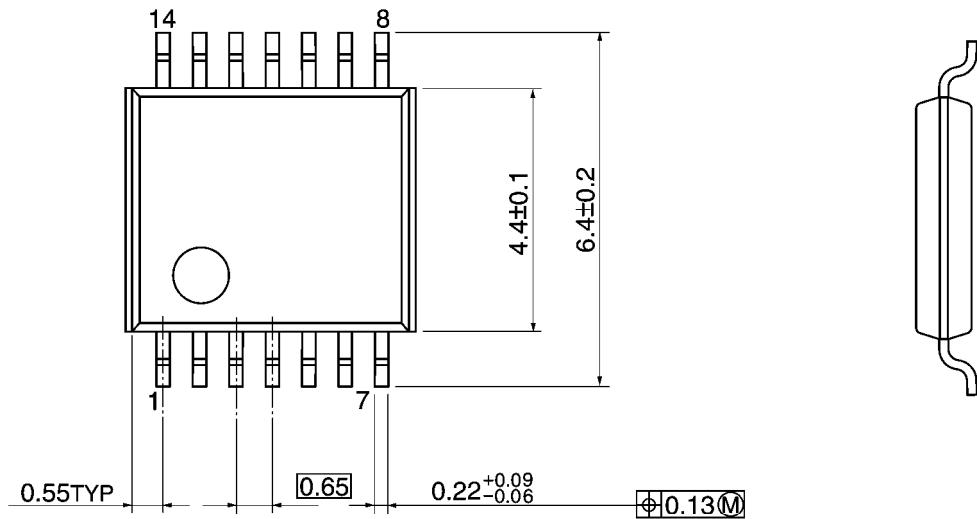
Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

Package Dimensions

TSSOP14-P-0044-0.65A

Unit: mm



Weight: 0.06 g (typ.)

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