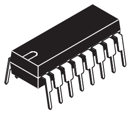


# LOW VOLTAGE DIFFERENTIAL (LVD) SCSI 9-LINE TERMINATOR

## FEATURES

- **Complies with SCSI, SCSI-2 and SPI-2 Standards**
- **5-pF Channel Capacitance During Disconnect**
- **Meets SCSI Hot Plugging**
- **−400-mA Sourcing Current for Termination**
- **+100-mA Sinking Current for Active Negation**
- **1-V Dropout Voltage Regulator**
- **Logic High Command Disconnects all Termination Lines**
- **100-µA Supply Current In Disconnect Mode**
- **Trimmed Termination Current to 5%**
- **Trimmed Impedance to 5%**
- **Low Thermal Resistance Surface Mount Packages**

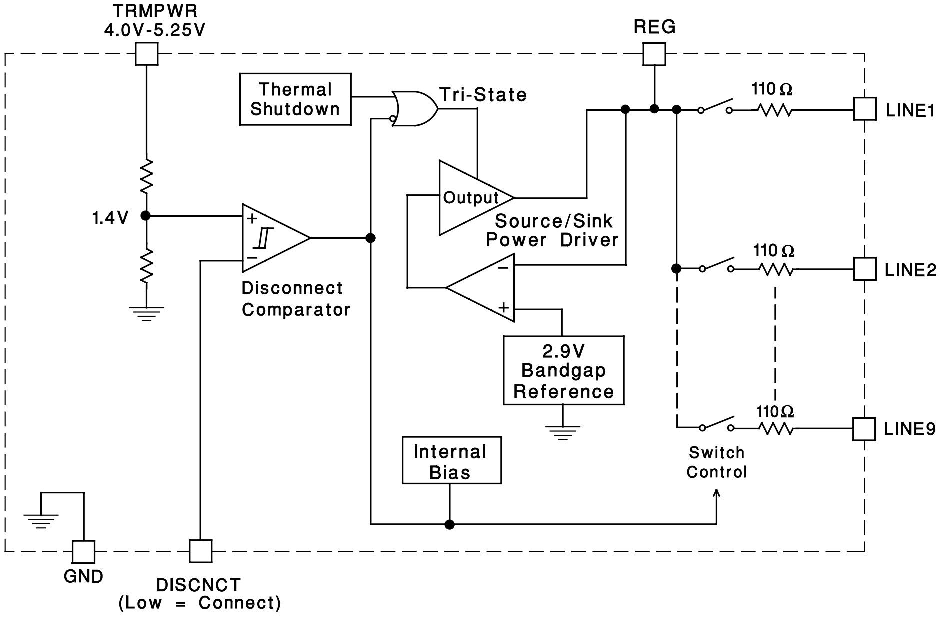
## DESCRIPTION

The UC5612 provides 9 lines of active termination for a small computer systems interface (SCSI) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The only functional differences between the UC5603 and UC5612 is the absence of the negative clamps on the output lines. Parametrically, the UC5612 has a 5% tolerance on impedance and current compared to a 3% tolerance on the UC5603. Custom power packages are utilized to allow normal operation at full power at 2 W.

The UC5612 provides a disconnect feature which, when opened or driven high, disconnects all terminating resistors, disables the regulator and greatly reduces standby power consumption. The output channels remain high impedance even without TERMPWR applied. A low channel capacitance of 5 pF allows interim points of the bus to have little to no effect on the signal integrity.

## BLOCK DIAGRAM



UDG−94133

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2003, Texas Instruments Incorporated

## DESCRIPTION (CONT.)

Internal circuit trimming is utilized, first to trim the impedance to a 5% tolerance, and then most importantly, to trim the output current to a 5% tolerance, as close to the maximum SCSI specification as possible. This maximizes the noise margin in fast SCSI operation. Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16-pin narrow body SOIC, 16-pin DIL and 24-pin TSSOP.

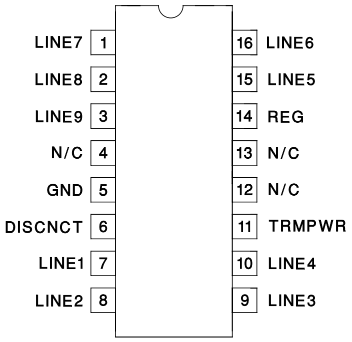
## ORDERING INFORMATION

| $T_A$ | PACKAGED DEVICE† | PACKAGED DEVICE† | PACKAGED DEVICE† |
|---|---|---|---|
| | **DIL-16 (N)** | **SOIC-16 (DP)** | **TSSOP-24 (PWP)** |
| 0°C to 70°C | UC5612N | UC5612DP | UC5612PWP |

† The TSSOP packages are available taped and reeled. Add TR suffix to device type (e.g. UC5612PWPTR) to order quantities of 2,000 devices per reel.

## CONNECTION DIAGRAM

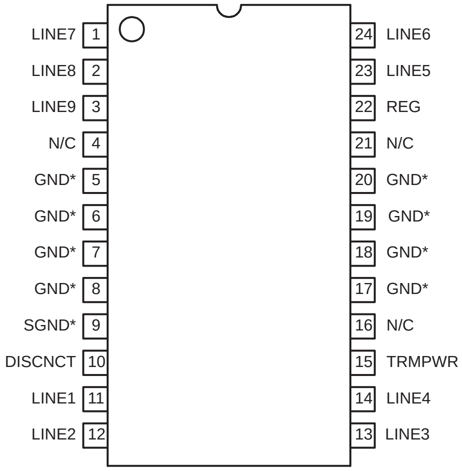
**DIL-16 (Top View)**
**N Package**



**SOIC-16 (Top View)**
**DP Package**

* DP package pin 5 serves as signal ground; pins 4, 12, and 13 serve as heatsink/ground.

**TSSOP-24 (Top View)**
**PWP Package**



* PWP package pin 9 serves as signal ground; pins 5, 6, 7, 8, 17, 18, 19 and 20 serve as heatsink/ground.

## RECOMMENDED OPERATING CONDITIONS

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| TRMPWR voltage | 3.8 | | 5.25 | V |
| Signal line voltage | 0 | | 5.0 | |
| Disconnect input voltage | 0 | | 6.0 | |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted†‡

| | UCC5640 | UNIT |
|---|---|---|
| TRMPWR voltage | 7 | V |
| Signal line voltage | 0 to 7.0 | |
| Regulator output current | 0.6 | A |
| Storage temperature, $T_{stg}$ | −65 to 150 | °C |
| Operating junction temperature, $T_J$ | –55 to 150 | |
| Lead temperature (soldering, 10 sec.) | 300 | |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

## ELECTRICAL CHARACTERISTICS

$T_A$ = 0°C to 70°C, TRMPWR = 4.75 V, $T_A$ = $T_J$, (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Supply Current Section** | | | | | | |
| Termpwr supply current | All termination lines = Open | | | 17 | 23 | mA |
| | All termination lines = 0.5 V | | | 200 | 225 | |
| Power down mode | DISCNCT = Open | | | 100 | 150 | µA |
| **Output Section (Termination Lines)** | | | | | | |
| Terminator impedance | $\Delta I_{LINE}$ = −5 mA to −15 mA | | 104.5 | 110 | 115.5 | Ω |
| Output high voltage | | | 2.65 | 2.9 | 3.1 | V |
| Max output current | $V_{LINE}$ = 0.5 V | $T_J$ = 25°C | −20.3 | −21.5 | −22.4 | mA |
| | | 0°C < $T_J$ < 70°C | −19.8 | −21.5 | −22.4 | |
| Max output current | $V_{LINE}$ = 0.5 V, TRMPWR = 4 V (1) | $T_J$ = 25°C | −19.5 | −21.5 | −22.4 | |
| | | 0°C < $T_J$ < 70°C | −19.0 | −21.5 | −22.4 | |
| | $V_{LINE}$ = 0.2V,<br>TRMPWR = 4 V to 5.25 V | 0°C < $T_J$ < 70°C | −21.6 | −24.0 | −25.4 | |
| Output leakage | DISCNCT = 4 V, REG = 0 V,<br>TRMPWR = 0 V to 5.25 V | $V_{LINE}$ = 0 V to 4 V | | 10 | 400 | nA |
| | | $V_{LINE}$ = 5.25 V | | | 100 | µA |
| | REG = Open | $V_{LINE}$ = 0 V to 5.25 V | | 10 | 400 | nA |
| Output capacitance | DISCNCT = Open, (DP package)(2) | | | 5 | 6 | pF |
| **Regulator Section** | | | | | | |
| Regulator output voltage | | | 2.7 | 2.9 | 3.1 | V |
| | All termination lines = 4 V | | 2.7 | 2.9 | 3.1 | |
| Line regulation | TRMPWR = 4 V to 6 V | | | 10 | 20 | mV |
| Drop out voltage | All termination lines = 0.5 V | | | 1.0 | 1.2 | V |
| Short circuit current | REG = 0 V | | −200 | −400 | −600 | mA |
| Sinking current capability | REG = 3.5 V | | 75 | 100 | 400 | |
| Thermal shutdown | | | | 170 | | °C |
| Thermal shutdown hysteresis | | | | 10 | | |
| **Disconnect Section** | | | | | | |
| Disconnect threshold | | | 1.1 | 1.4 | 1.7 | V |
| Input current | DISCNCT = 0 V | | | −10 | −20 | µA |

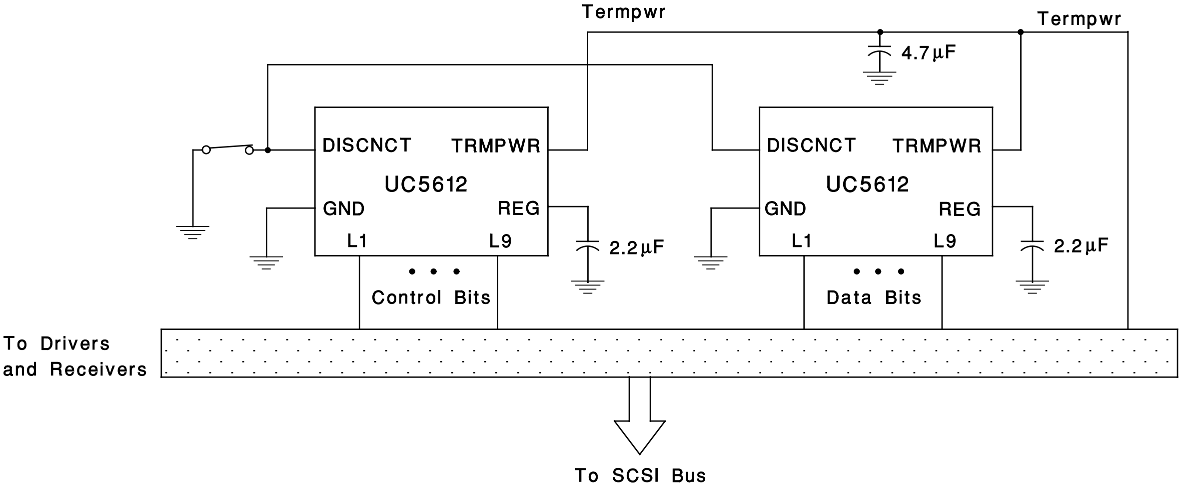
NOTE: (1) Measuring each termination line while other eight are low.
(2) Ensured by design. Not production tested.

## TERMINAL FUNCTIONS(1)

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DISCNCT | 6 | | Taking this pin high or leaving it open causes the nine channels to become high impedance and the chip to go into low-power mode; a low state allows the channels to provide normal termination. |
| GND | 5 | | Ground reference for the device |
| LINE1 − LINE9 | 1, 2, 3, 7, 8, 9, 10, 15, 16 | | 110-Ω termination channels. |
| REG | 14 | | Output of the internal 2.8-V regulator. |
| TRMPWR | 11 | | Power for the device. |

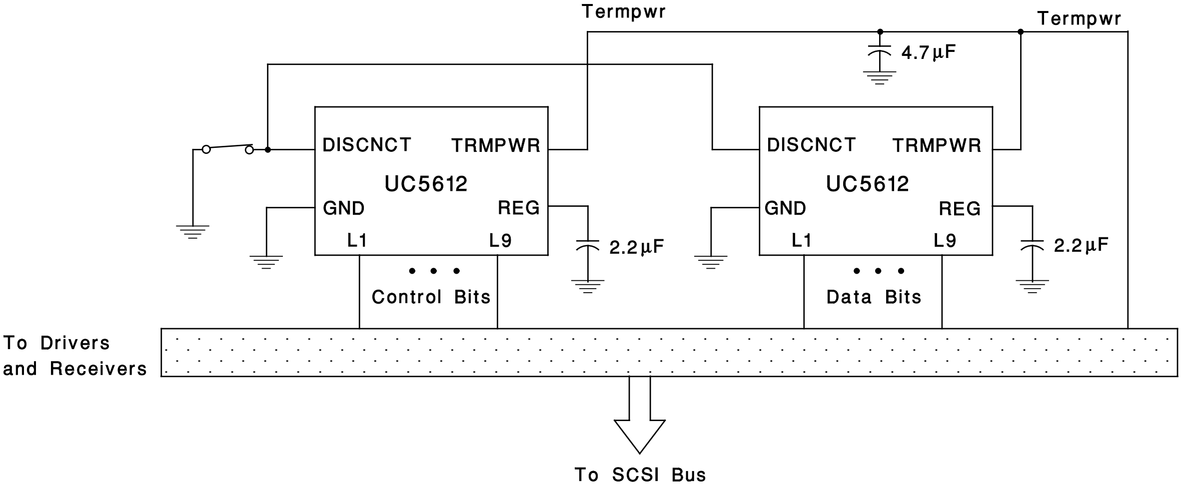
NOTE: (1) N package.

## APPLICATION INFORMATION



UDG−94134

Figure 1. Typical SCSI Bus Configurations Utilizing Two UC5612 Devices



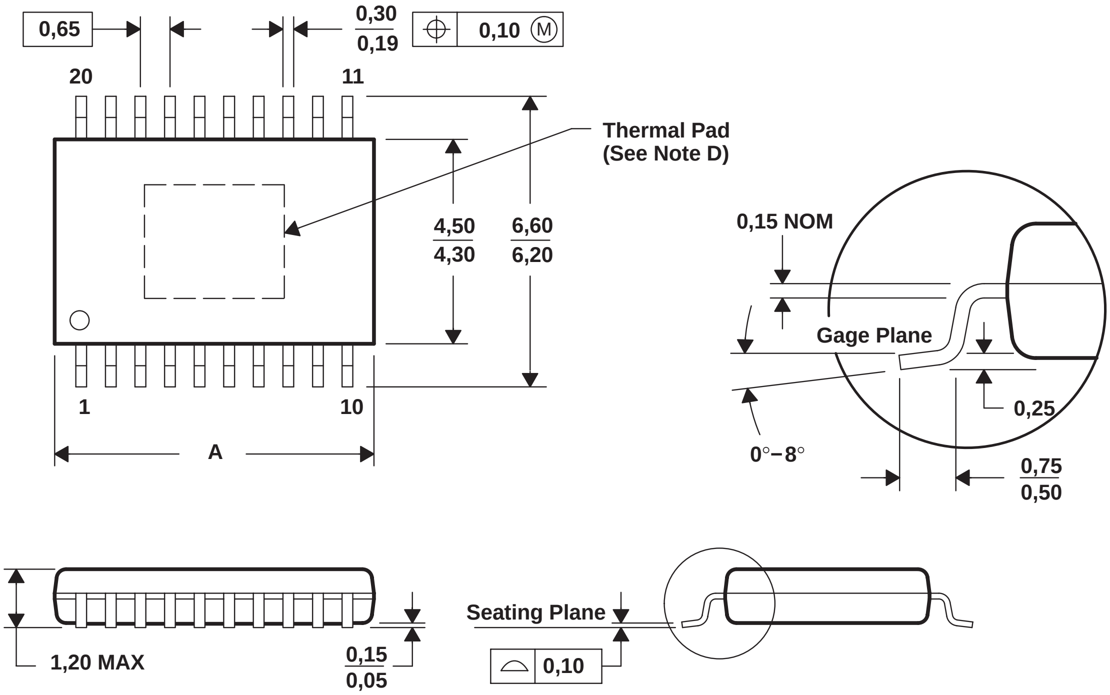
UDG−94135

Figure 2. Typical Wide SCSI Bus Configurations Utilizing Three UC5612 Devices

## MECHANICAL DATA

**PWP (R-PDSO-G**)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

**20 PINS SHOWN**



| PINS ** / DIM | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|
| **A MAX** | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| **A MIN** | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4073225/F 10/98**

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions.
- D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
- E. Falls within JEDEC MO-153

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| UC5612DP | ACTIVE | SOIC | D | 16 |  | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC5612DPG4 | ACTIVE | SOIC | D | 16 |  | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC5612DPTR | ACTIVE | SOIC | D | 16 |  | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC5612DPTRG4 | ACTIVE | SOIC | D | 16 |  | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC5612PWP | ACTIVE | TSSOP | PW | 24 |  | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC5612PWPG4 | ACTIVE | TSSOP | PW | 24 |  | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC5612PWPTR | ACTIVE | TSSOP | PW | 24 |  | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC5612PWPTRG4 | ACTIVE | TSSOP | PW | 24 |  | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

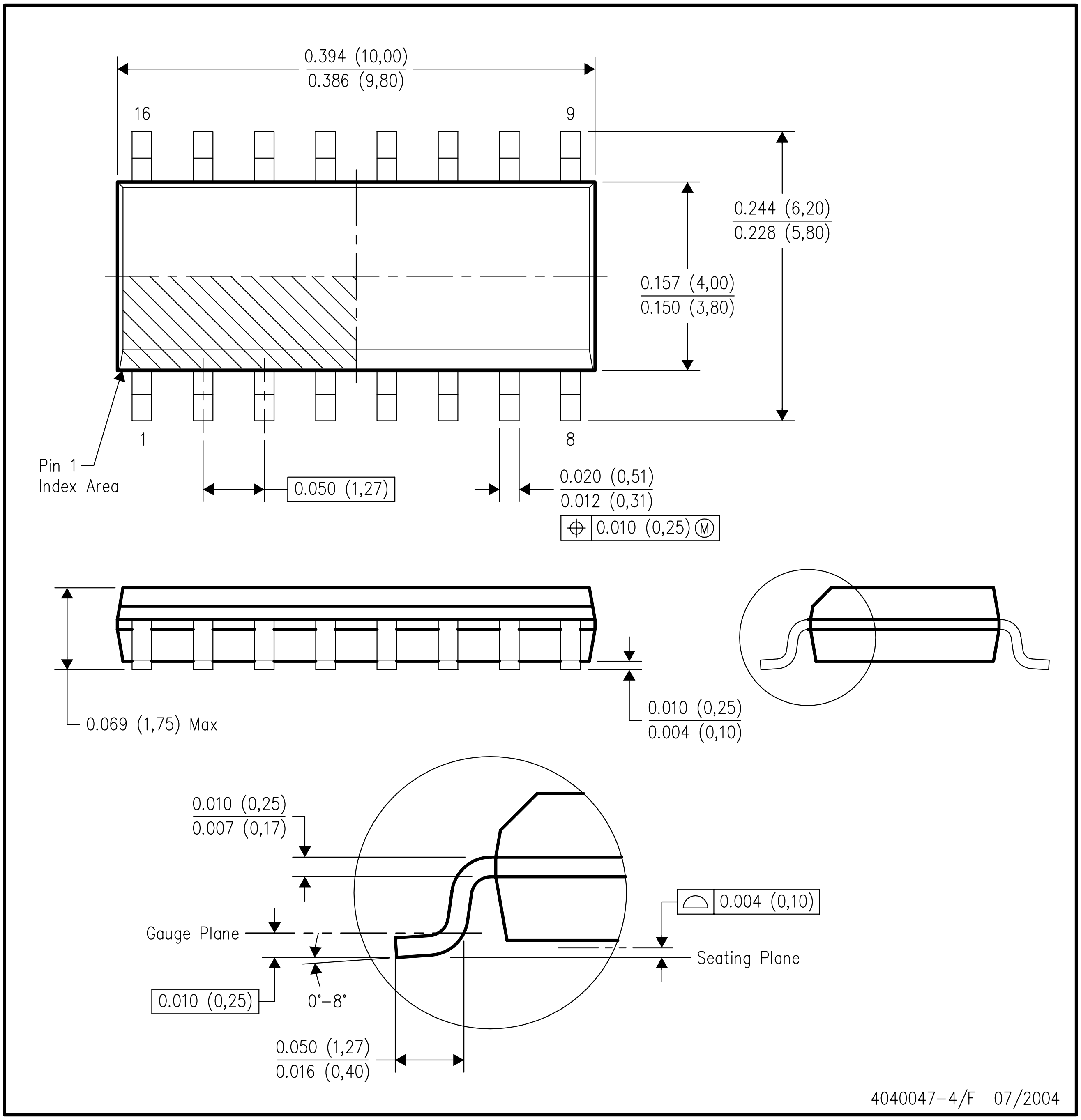
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

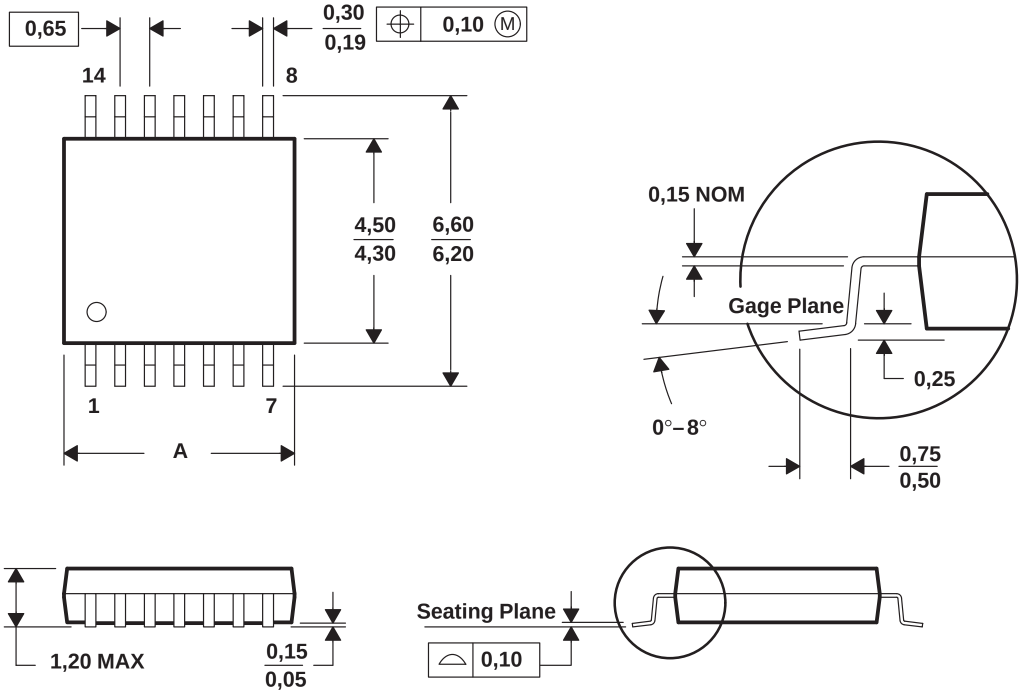
## D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–012 variation AC.

## PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

**14 PINS SHOWN**



| PINS ** / DIM | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated