

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC4049AP, TC74HC4049AF, TC74HC4049AFN, TC74HC4049AFT  
TC74HC4050AP, TC74HC4050AF, TC74HC4050AFN, TC74HC4050AFT

TC74HC4049AP/AF/AFN/AFT HEX BUFFER / CONVERTER ( INVERTING )  
TC74HC4050AP/AF/AFN/AFT HEX BUFFER / CONVERTER

The TC74HC4049A and TC74HC4050A are high speed CMOS HEX BUFFERS fabricated with silicon gate C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC4049A is an inverting buffer, while the TC74HC4050A is a non - inverting buffer. The internal circuits are composed of 3 - stages ( HC4049A ) or 2 - stages ( HC4050A ) of inverters, which provided high noise immunity and stable output.

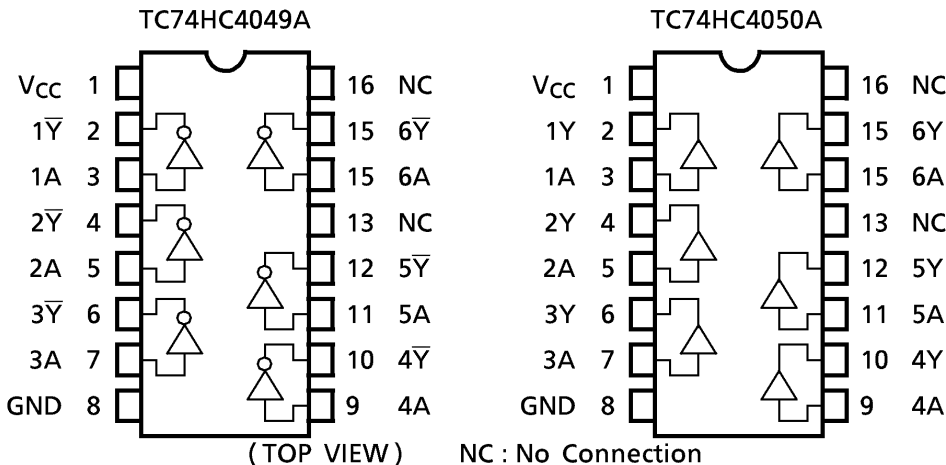
Input protection circuits are different from those of other high speed CMOS IC's. They eliminate the diodes on the V<sub>CC</sub> side thus providing of logic - level conversion from high - level volages up to 15V to low - level voltages.

They are useful for battery back up circuits, because input voltage can be applied on IC's which are not biased by V<sub>CC</sub>.

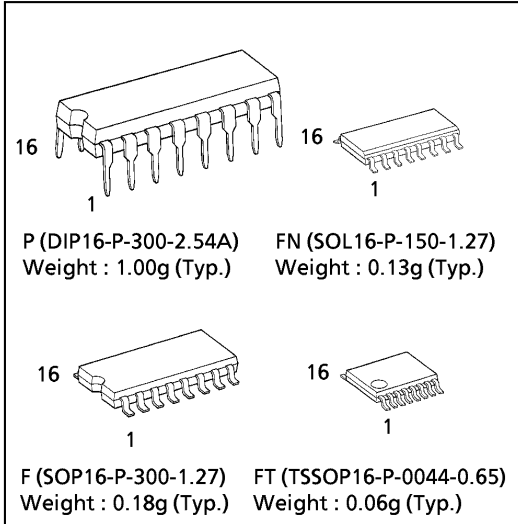
FEATURES :

- High Speed.....t<sub>pd</sub> = 9ns(typ.) at V<sub>CC</sub> = 5V
- Low Power Dissipation.....I<sub>CC</sub> = 1μA(Max.) at Ta = 25°C
- High Noise Immunity.....V<sub>NIH</sub> = V<sub>NIL</sub> = 28% V<sub>CC</sub> (Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance...| I<sub>OH</sub> | = I<sub>OL</sub> = 6mA (Min.)
- Balanced Propagation Delays.....t<sub>pLH</sub> ≈ t<sub>pHL</sub>
- Wide Operating Voltage Range...V<sub>CC</sub> (opr.) = 2V ~ 6V
- Pin and Function Compatible with 4049B / 4050B

PIN ASSIGNMENT



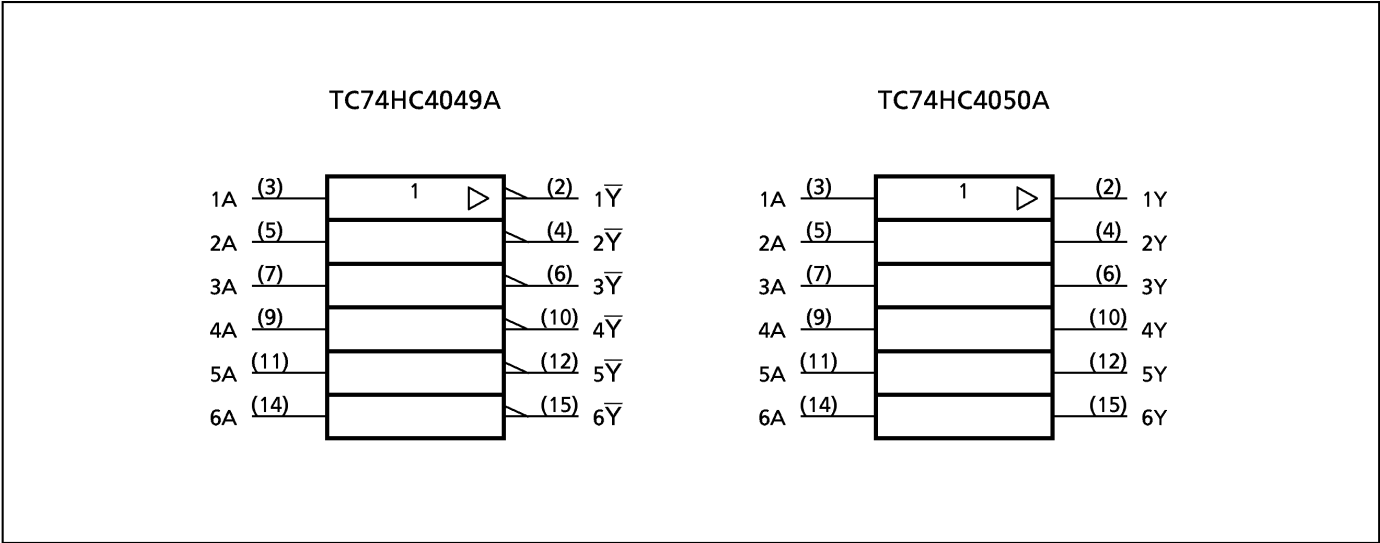
(Note) The JEDEC SOP (FN) is not available in Japan.



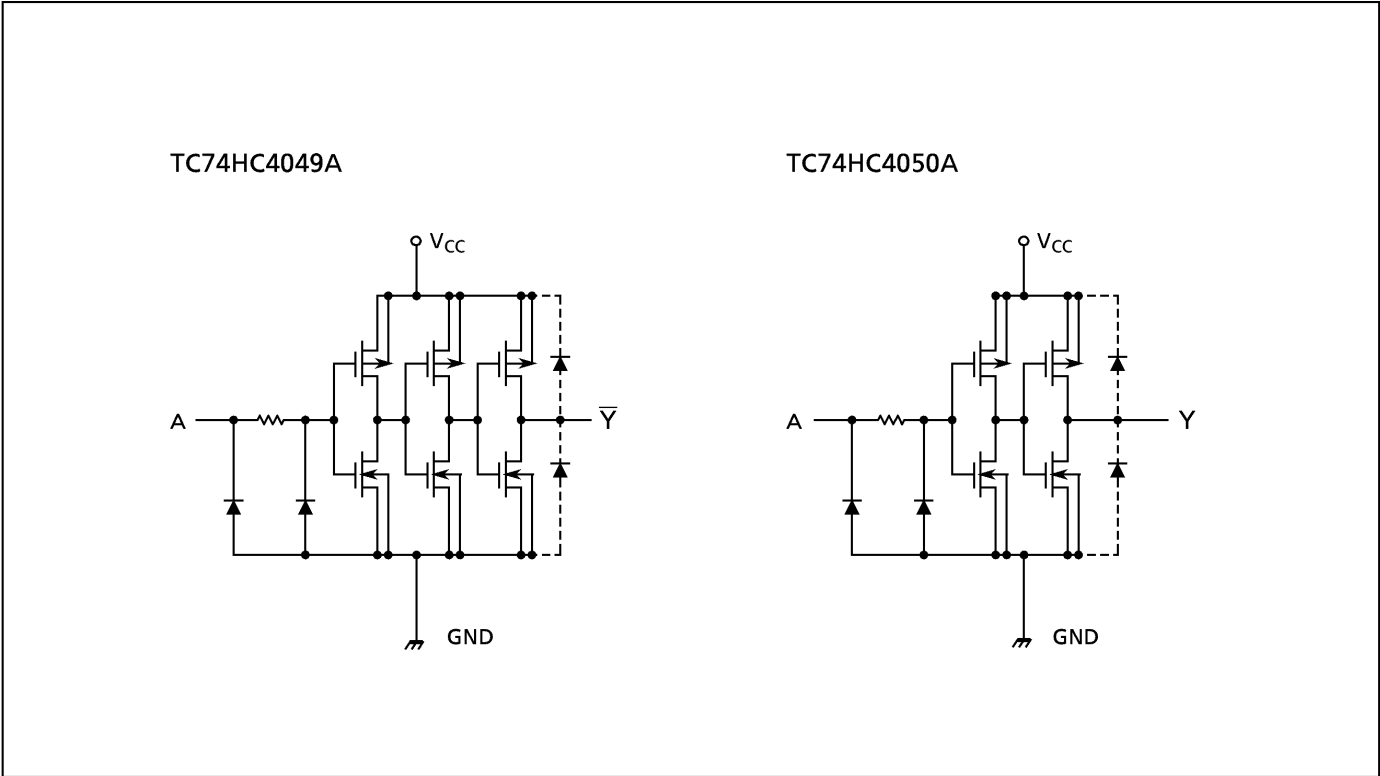
TRUTH TABLE

A	Y ( 4049A )	Y ( 4050A )
L	H	L
H	L	H

IEC LOGIC SYMBOL



INPUT and OUTPUT EQUIVALENT CIRCUIT



## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	$-0.5 \sim 7$	V
DC Input Voltage	$V_{IN}$	$-0.5 \sim 18^*$	V
DC Output Voltage	$V_{OUT}$	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	$-20$	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 35$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 75$	mA
Power Dissipation	$P_D$	500(DIP)**/180 (SOP,TSSOP)	mW
Storage Temperature	$T_{stg}$	$-65 \sim 150$	$^{\circ}\text{C}$

Note) \* DC input voltage ( $V_{IN}$ ) specified is measured to GND and is not related to  $V_{CC}$ .

Recommended operating range is 0V to 15V and it is possible to convert logic-levels from 15V to 5V or 5V to 2V.

\*\* 500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  shall be applied until 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	$2 \sim 6$	V
Input Voltage	$V_{IN}$	$0 \sim 15$	V
Output Voltage	$V_{OUT}$	$0 \sim V_{CC}$	V
Operating Temperature	$T_{opr}$	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	$t_r, t_f$	$0 \sim 1000$ ( $V_{CC} = 2.0\text{V}$ ) $0 \sim 500$ ( $V_{CC} = 4.5\text{V}$ ) $0 \sim 400$ ( $V_{CC} = 6.0\text{V}$ )	ns

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	$V_{IH}$		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	$V_{IL}$		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	V
			$I_{OH} = -6 \text{ mA}$ $I_{OH} = -7.8 \text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	V
			$I_{OL} = 6 \text{ mA}$ $I_{OL} = 7.8 \text{ mA}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$
		$V_{IN} = 15\text{V}$	6.0	—	—	$\pm 0.5$	—	$\pm 5.0$	
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	1.0	—	10.0	

AC ELECTRICAL CHARACTERISTICS ( Input  $t_r = t_f = 6\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	$t_{TLH}$ $t_{THL}$		50	2.0	—	25	60	—	75	ns
				4.5	—	6	12	—	15	
				6.0	—	5	10	—	13	
Propagation Delay Time	$t_{PLH}$ $t_{PHL}$		50	2.0	—	30	75	—	95	
				4.5	—	9	15	—	19	
				6.0	—	8	13	—	16	
			150	2.0	—	45	100	—	145	
				4.5	—	14	20	—	29	
				6.0	—	12	17	—	25	
Input Capacitance	C <sub>IN</sub>				—	5	10	—	10	pF
Power Dissipation Capacitance	C <sub>PD</sub> (1)				—	26	—	—	—	

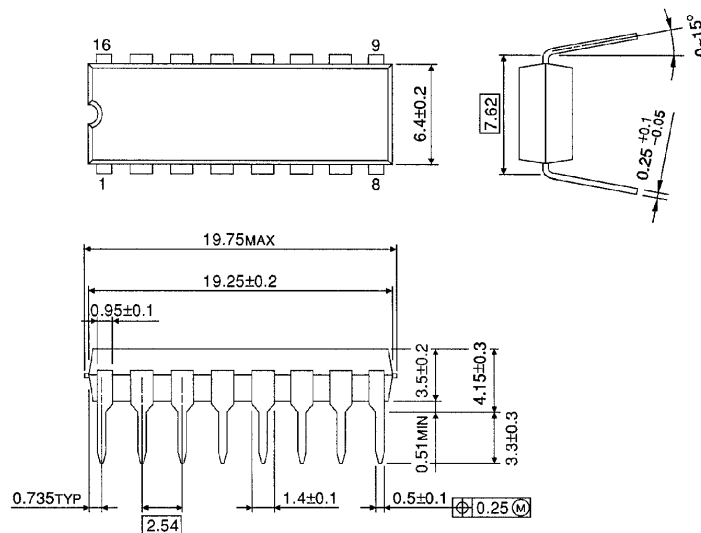
Note (1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ ( per Gate )}$$

## DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

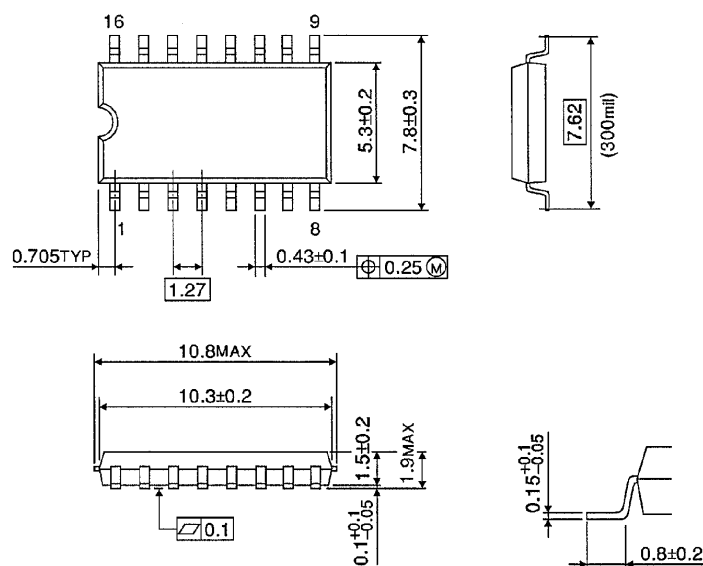
Unit in mm



Weight : 1.00g (Typ.)

## SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm

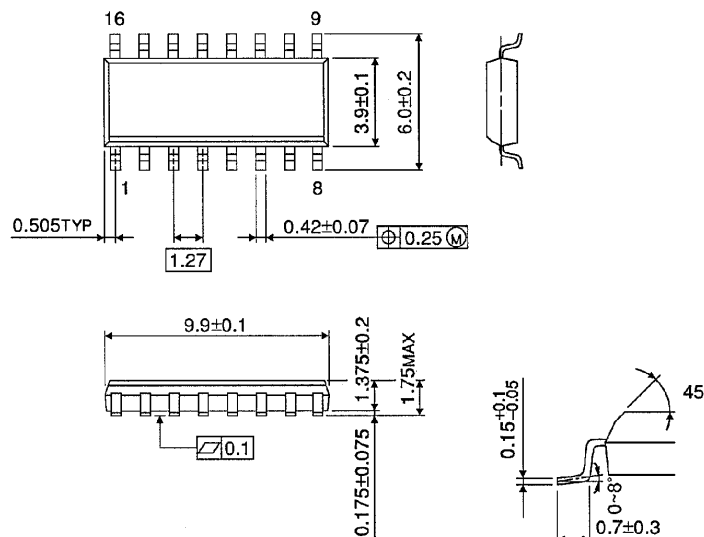


Weight : 0.18g (Typ.)

## SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)

Unit in mm

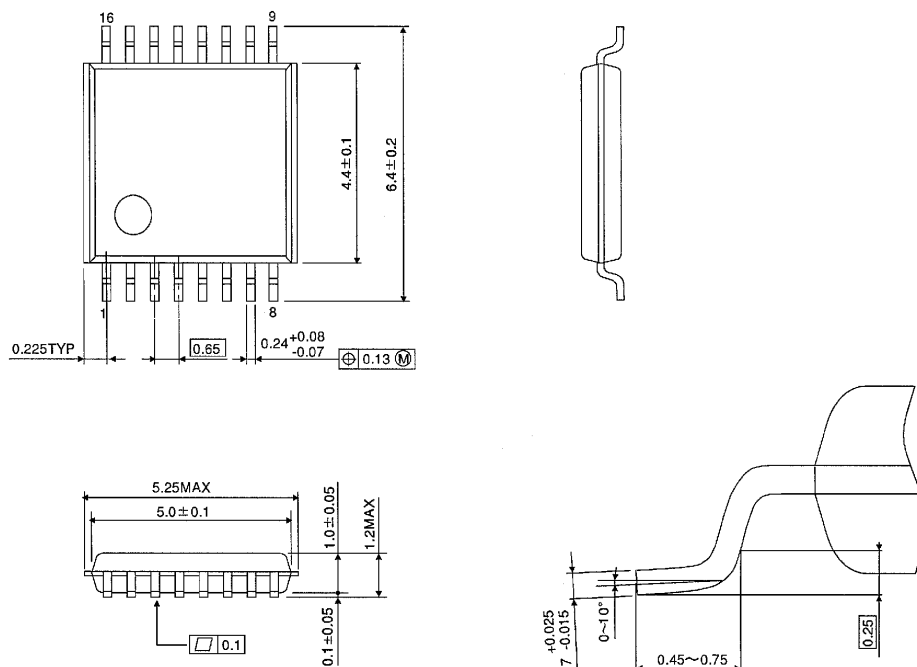
(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

## TSSOP 16PIN PACKAGE DIMENSIONS (TSSOP16-P-0044-0.65)

Unit in mm



Weight : 0.06g (Typ.)

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