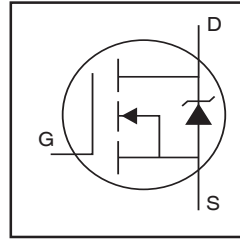


AUIRF3004WL

WIDELEAD HEXFET® Power MOSFET

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 50% Lower Lead Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *



$V_{(BR)DSS}$	40V
$R_{DS(on)}$ typ.	1.27mΩ
max.	1.40mΩ
I_D (Silicon Limited)	386A ①
I_D (Package Limited)	240A

Description

Specifically design for automotive applications this Widelead TO-262 package part has the advantage of having over 50% lower lead resistance and delivering over 20% lower $R_{DS(on)}$ when compared with a traditional TO-262 package housing the same silicon die. This greatly helps in reducing condition losses, achieving higher current levels or enabling a system to run cooler and have improved efficiency. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive and other applications.



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	386①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	273①	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	240	
I_{DM}	Pulsed Drain Current ②	1544	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	375	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	470	mJ
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ②		mJ
dv/dt	Peak Diode Recovery ④	6.1	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	0.40	°C/W

HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>

Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.038	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.27	1.40	m Ω	$V_{GS} = 10V, I_D = 195A$ ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
gfs	Forward Transconductance	330	—	—	S	$V_{DS} = 10V, I_D = 195A$
R_G	Internal Gate Resistance	—	2.7	—	Ω	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 32V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	—	140	210	nC	$I_D = 232A$
Q_{gs}	Gate-to-Source Charge	—	53	—		$V_{DS} = 20V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	49	—		$V_{GS} = 10V$ ⑤
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	91	—		$I_D = 232A, V_{DS} = 0V, V_{GS} = 10V$ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	19	—	ns	$V_{DD} = 26V$
t_r	Rise Time	—	220	—		$I_D = 232A$
$t_{d(off)}$	Turn-Off Delay Time	—	90	—		$R_G = 2.7\Omega$
t_f	Fall Time	—	130	—		$V_{GS} = 10V$ ⑤
C_{iss}	Input Capacitance	—	9450	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1930	—		$V_{DS} = 32V$
C_{rss}	Reverse Transfer Capacitance	—	975	—		$f = 1.0MHz$, See Fig.5
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	2330	—		$V_{GS} = 0V, V_{DS} = 0V$ to $32V$ ⑦, See Fig.11
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	2815	—		$V_{GS} = 0V, V_{DS} = 0V$ to $32V$ ⑧

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	386①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	1544		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 195A, V_{GS} = 0V$ ⑤
t_{rr}	Reverse Recovery Time	—	41	62	ns	$T_J = 25^\circ\text{C}$ $V_R = 34V$,
		—	51	77		$T_J = 125^\circ\text{C}$ $I_F = 232A$
Q_{rr}	Reverse Recovery Charge	—	62	93	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ⑤
		—	99	149		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	2.3	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 240A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140

<http://www.irf.com/technical-info/appnotes/an-1140.pdf>

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.018mH$

$R_G = 50\Omega$, $I_{AS} = 232A$, $V_{GS} = 10V$. Part not recommended for use above this value.

④ $I_{SD} \leq 232A$, $di/dt \leq 907A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.

⑤ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

⑥ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑦ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑧ R_θ is measured at T_J approximately 90°C .

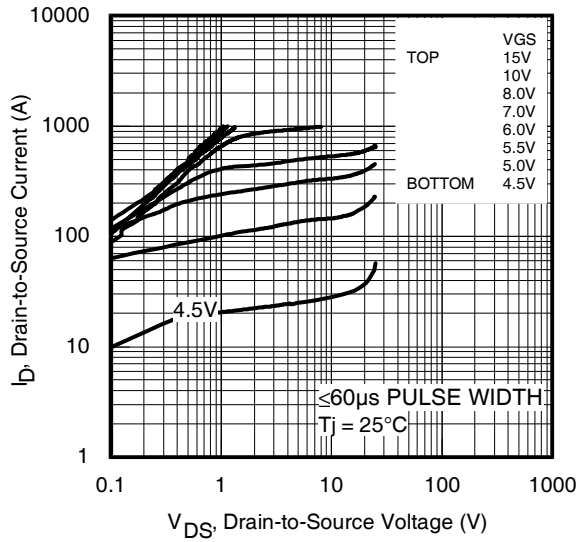


Fig 1. Typical Output Characteristics

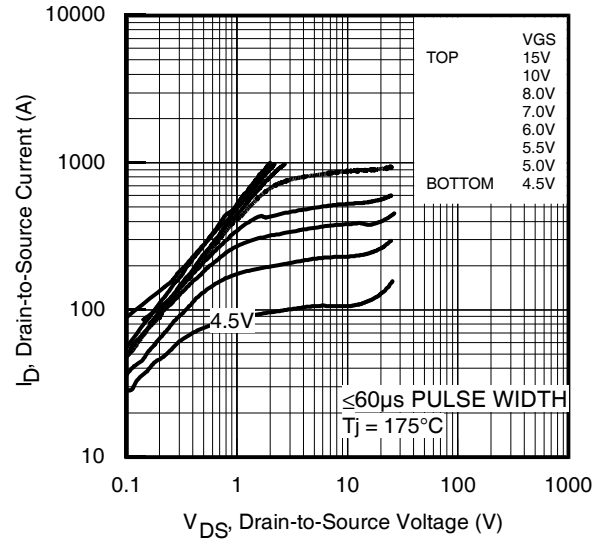


Fig 2. Typical Output Characteristics

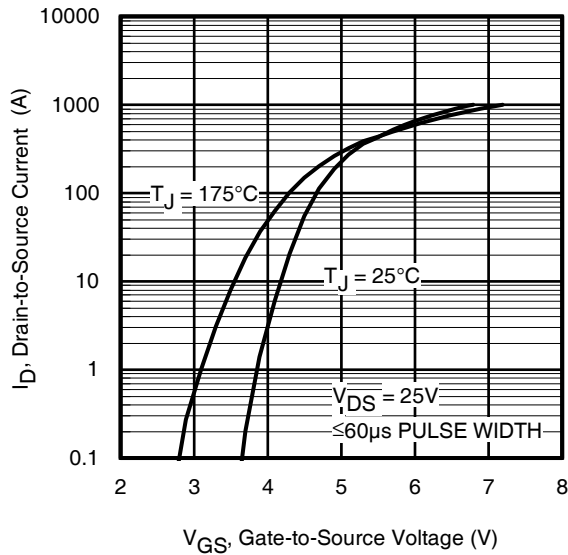


Fig 3. Typical Transfer Characteristics

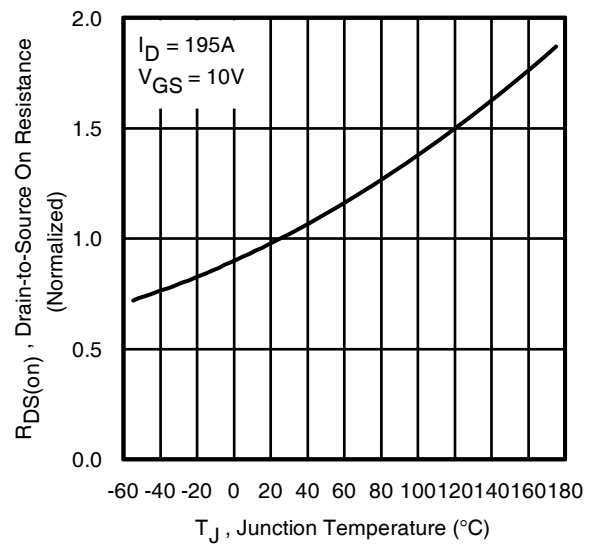


Fig 4. Normalized On-Resistance vs. Temperature

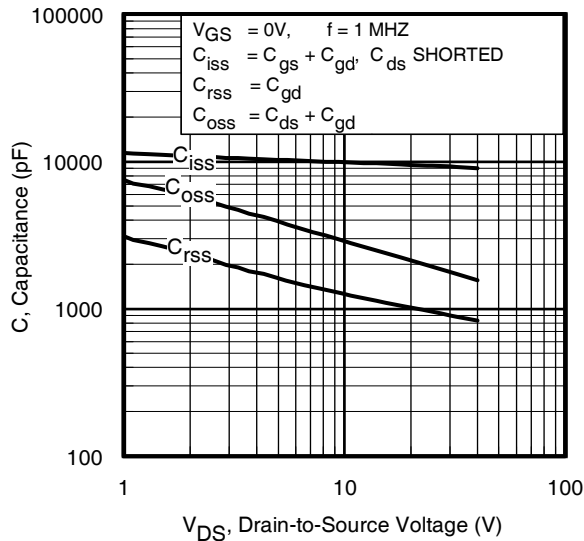


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

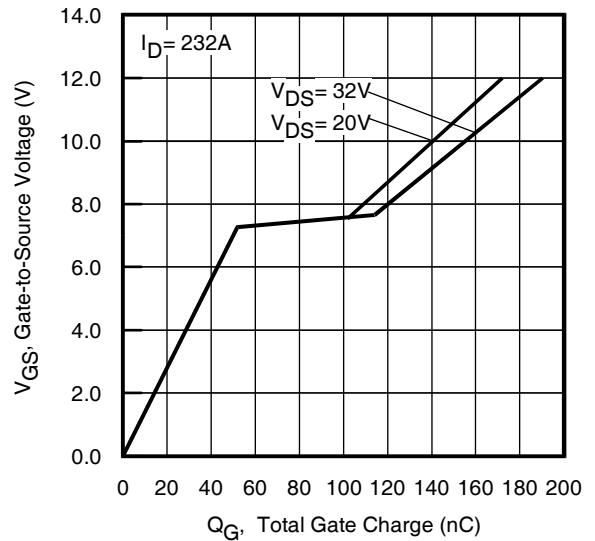


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

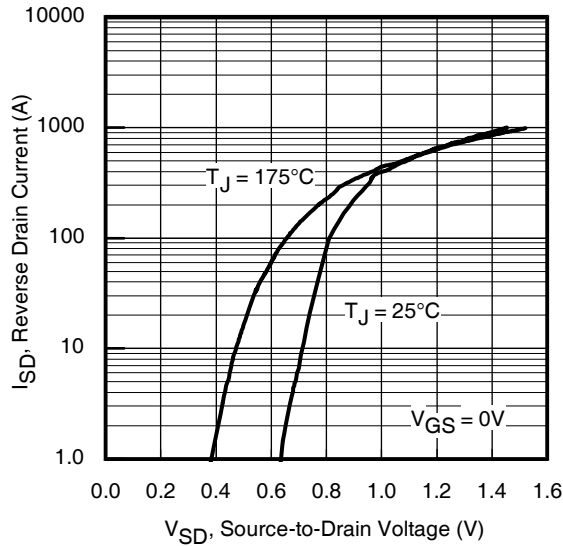


Fig 7. Typical Source-Drain Diode Forward Voltage

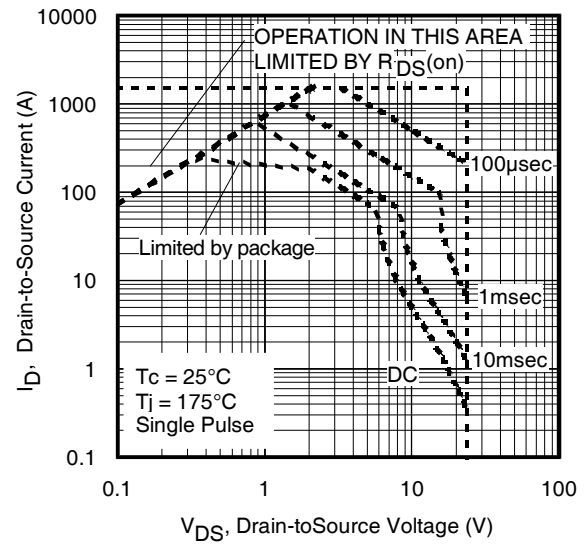


Fig 8. Maximum Safe Operating Area

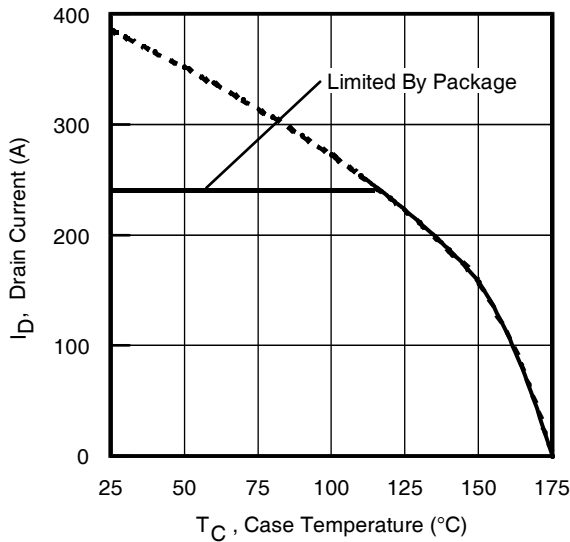


Fig 9. Maximum Drain Current vs. Case Temperature

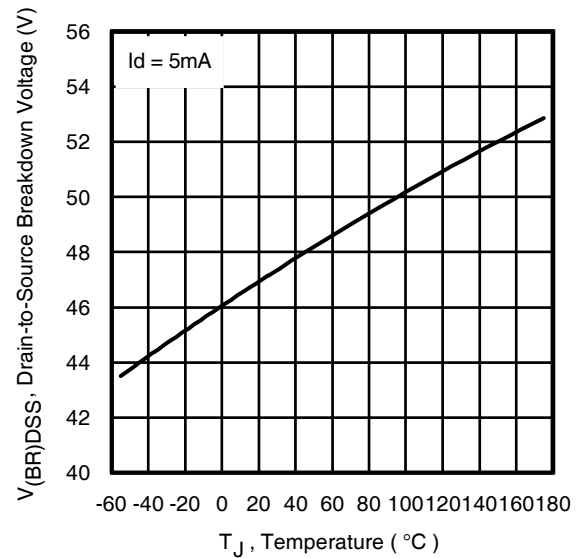


Fig 10. Drain-to-Source Breakdown Voltage

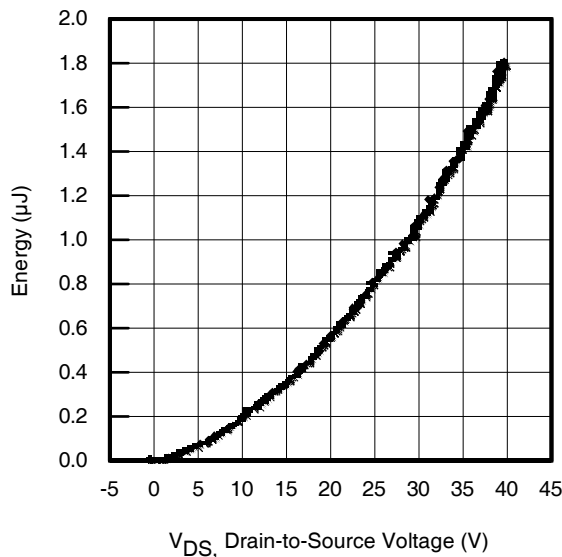


Fig 11. Typical C_{OSS} Stored Energy

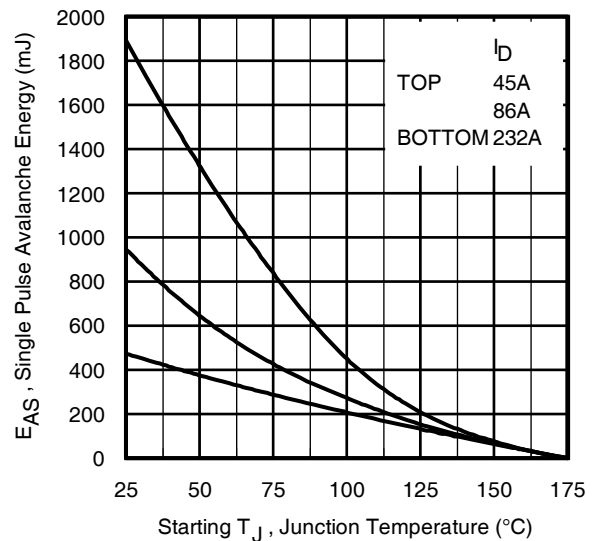


Fig 12. Maximum Avalanche Energy vs. Drain Current

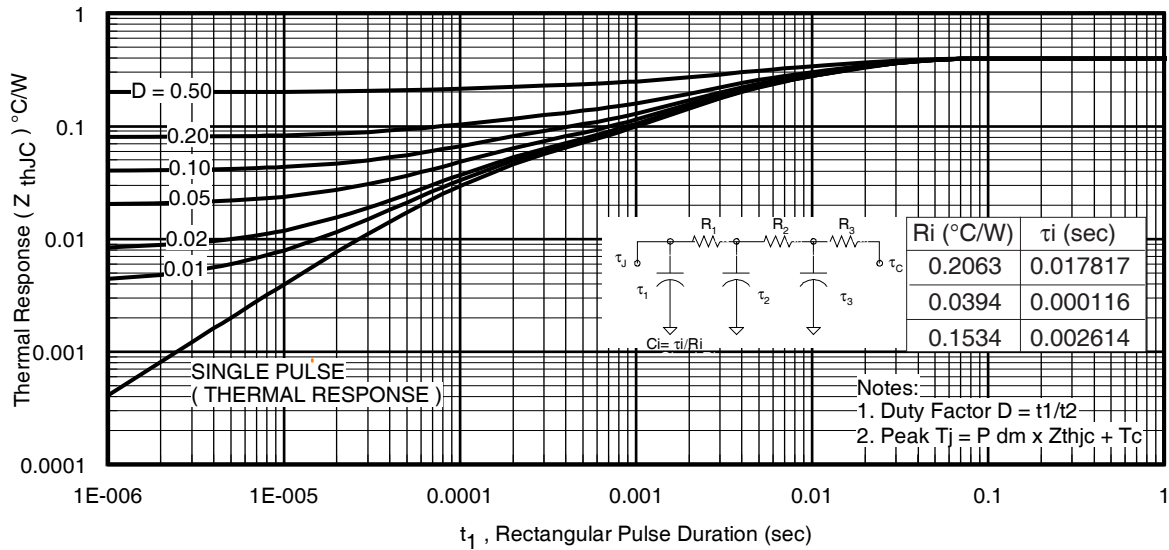


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

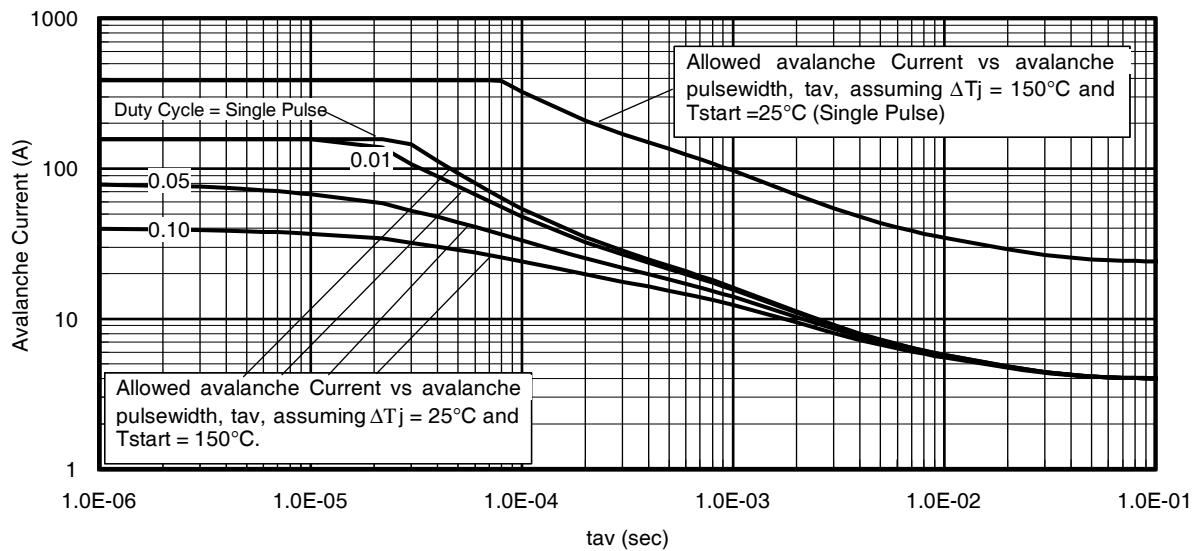
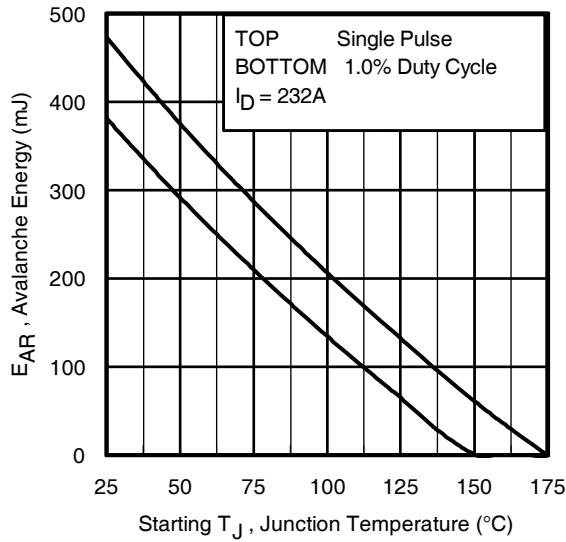


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figure 22a, 22b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = \frac{1}{2} (1.3 \cdot BV \cdot I_{av}) = \frac{\Delta T}{Z_{thJC}}$$

$$I_{av} = \frac{2\Delta T}{[1.3 \cdot BV \cdot Z_{th}]}$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

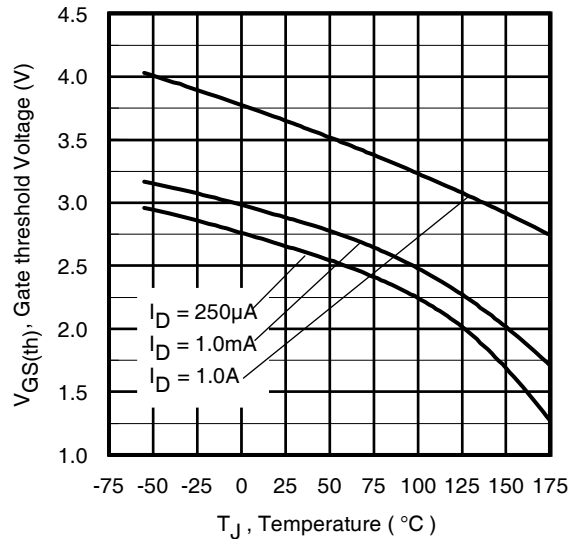
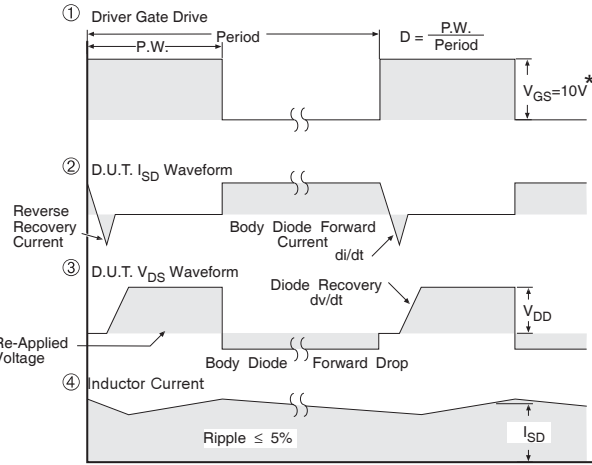
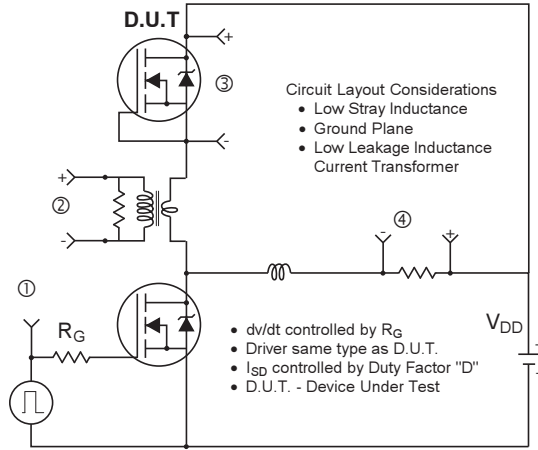


Fig 16. Threshold Voltage vs. Temperature



* $V_{GS} = 5V$ for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

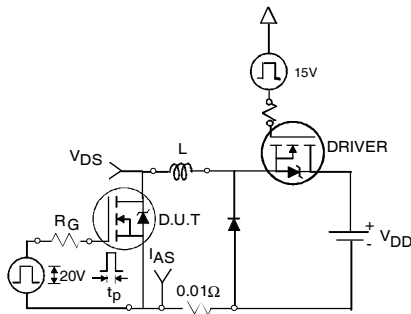


Fig 22a. Unclamped Inductive Test Circuit

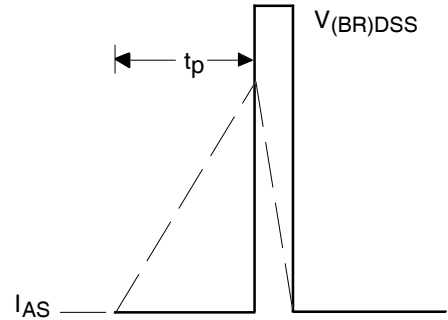


Fig 22b. Unclamped Inductive Waveforms

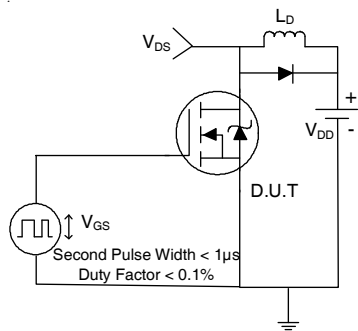


Fig 23a. Switching Time Test Circuit

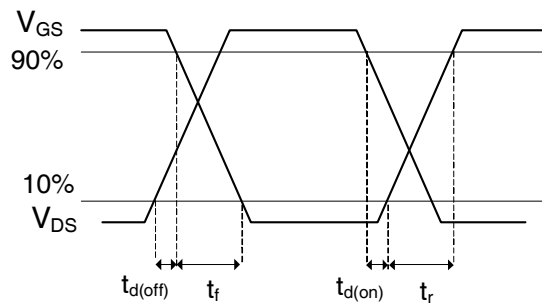


Fig 23b. Switching Time Waveforms

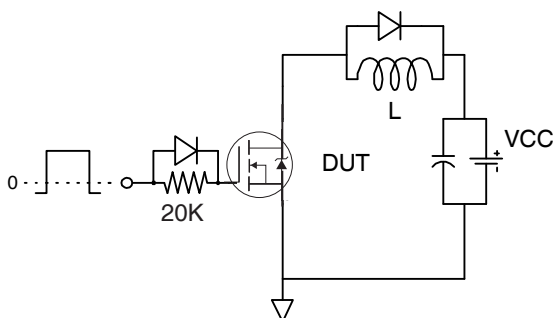


Fig 24a. Gate Charge Test Circuit

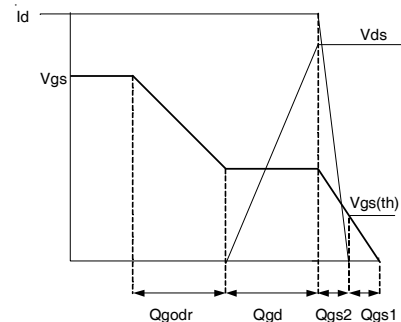
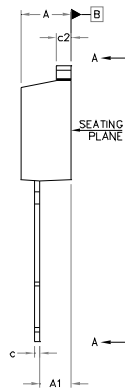
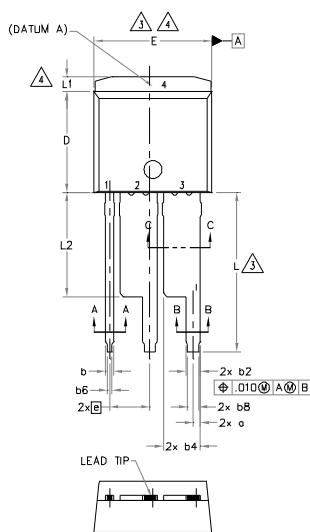


Fig 24b. Gate Charge Waveform

TO-262 WideLead Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	2.03	3.02	.080	.119	
a	0.20	0.51	.008	.020	
b	0.51	0.91	.020	.036	
b1	0.51	0.81	.020	.032	
b2	1.07	1.47	0.42	.058	5
b3	1.07	1.37	.042	.054	
b4	3.05	3.45	.120	.136	5
b5	3.05	3.35	.120	.132	
b6	0.25	0.61	.010	.024	5
b7	0.25	0.51	.010	.020	
b8	0.76	1.17	.030	.046	5
b9	0.76	1.07	.030	.022	
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	3
D	8.51	9.65	.335	.380	
D1	6.86	7.42	.270	.292	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	8.48	.245	.334	4
e	3.81 BSC		.150 BSC		4
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	
L2	8.64	9.40	.340	.370	

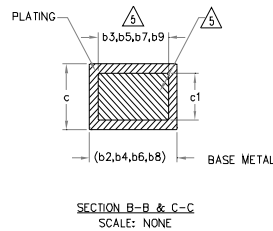
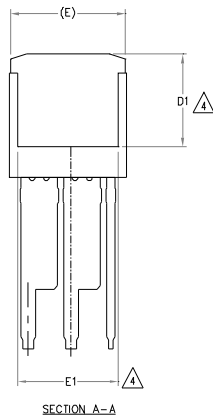
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b3, b5, b7, b9 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

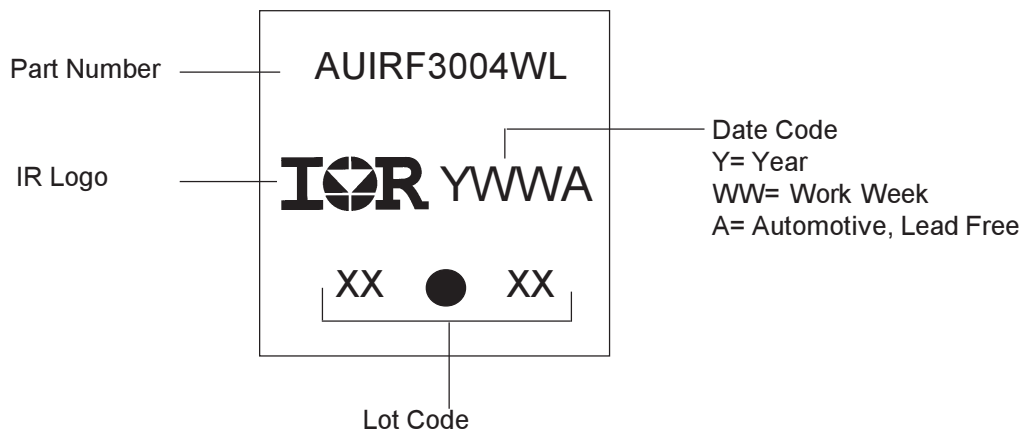
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE



SECTION B-B & C-C
SCALE: NONE

TO-262 WideLead Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRF3004WL	TO-262 WideLead	Tube	50	AUIRF3004WL

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