TDA7210V

ASK/FSK Single Conversion Receiver

Data Sheet

Revision 1.1, 2010-06-18

Wireless Sense & Control

Edition 2010-06-18

Published by
Infineon Technologies AG
81726 Munich, Germany

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TDA7210V ASK/FSK Single Conversion Receiver

Revision History: 2010-06-18, Revision 1.1

Previous Revision: 1.0

Page	Subjects (major changes since last revision)
29	Explanation regarding the Absolute Maximum Ratings

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1 Product Description

1.1 Overview

The IC is a very low power consumption single chip FSK/ASK Superheterodyne Receiver (SHR) for the frequency bands 810 to 870 MHz and 400 to 440 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a PLL FSK demodulator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

1.2 Features

Main features:

- Selectable frequency ranges 810-870 MHz and 400-440 MHz
- Low supply current (at 434 MHz Is = 5.7 mA typ. FSK mode, 5.0 mA typ. ASK mode)
- Power down mode with very low supply current (50 nA typ.)
- FSK and ASK demodulation capability
- RF input sensitivity ASK/FSK typ. –115 dBm/–112 dBm @ 1 kbit/s RF=434 MHz
- RF input sensitivity ASK/FSK typ. –111 dBm/–111 dBm @ 1 kbit/s RF=868 MHz
- Fully integrated VCO and PLL Synthesiser
- Limiter with RSSI generation, operating at 10.7 MHz
- Selectable reference frequency
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold
- Supply voltage range 5 V ±10%

1.3 Application

The TDA7210V is suitable for any kind of remote control system especially for low data rate wireless applications where low current consumption is important and where the line-of-sight limitation is driving the infra-red to RF replacement.

Main applications:

- Home automation
  - Lighting Control
  - Curtain, Roller Blind Control
  - Air Condition Control
- Set-top-boxes
- Garage Door Openers
- Alarm Systems
- Wireless Toys
- Remote Keyless Entry Systems

1.4 Ordering Information

Table 1 Ordering Info

Type	Ordering Code	Package[1)]
TDA7210V	SP000698080	VQFN-32

1) Samples available on tape and reel.

1.5 Package Outlines

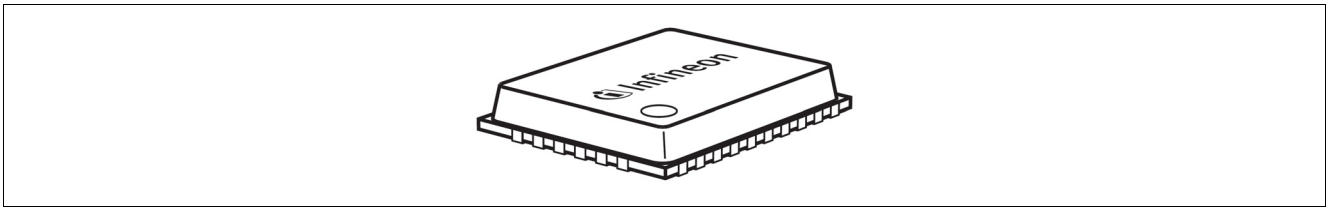


Figure 1 Package

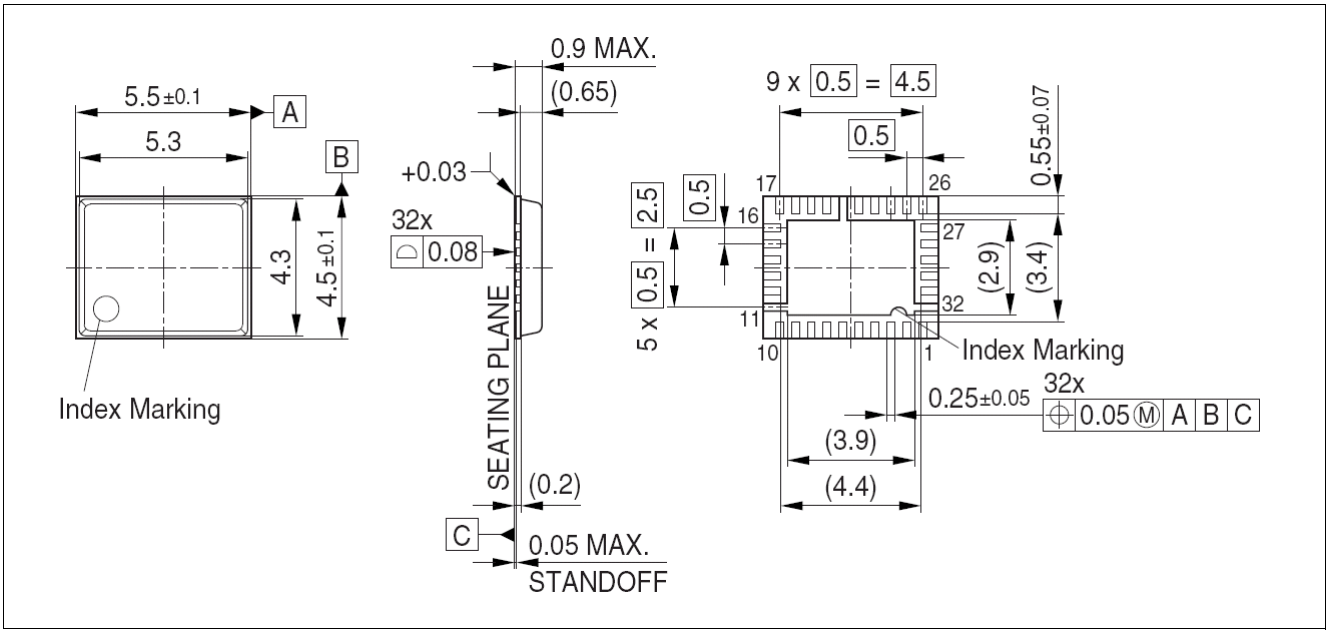


Figure 2 VQFN-32 Package Outlines

2 Functional Description

2.1 Pin Configuration

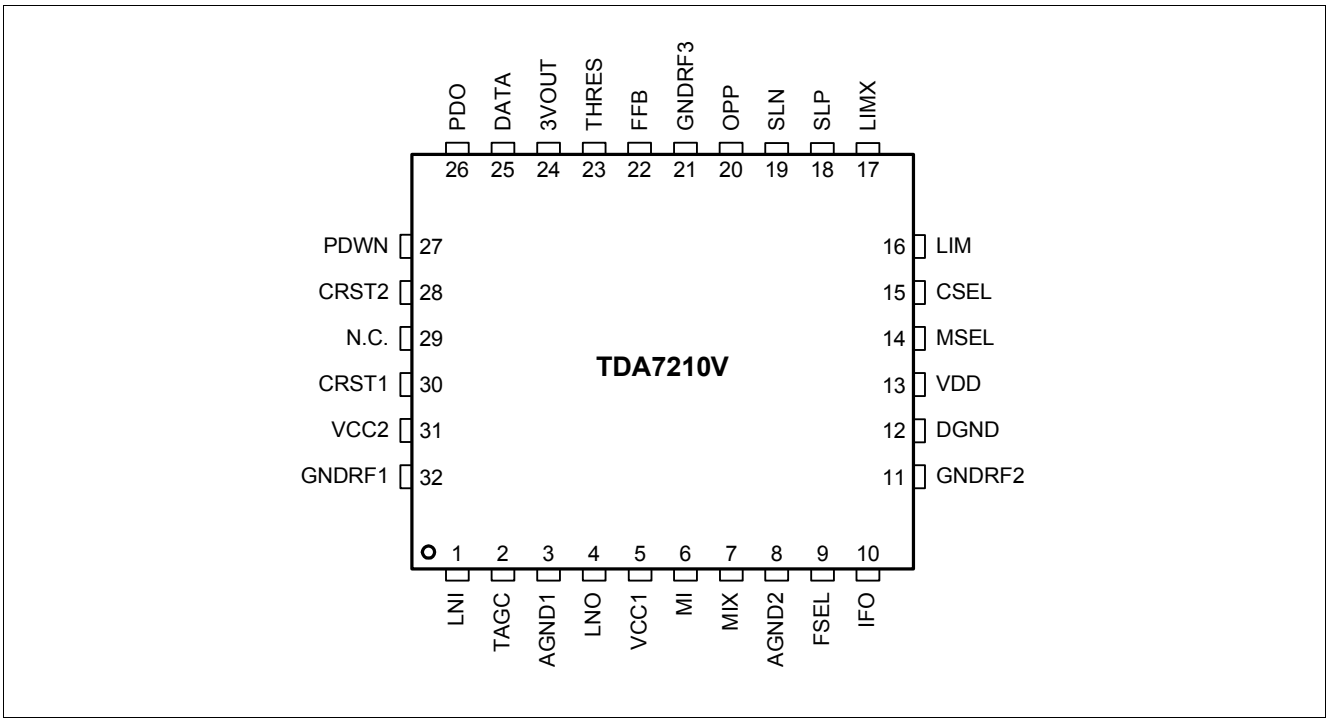


Figure 3 Pin Configuration TDA7210V

2.2 Pin Definition and Function

In the subsequent table the internal circuits connected to the pins of the device are shown. ESD-protection circuits are omitted to ease reading.

Table 2 Pin Definition and Function

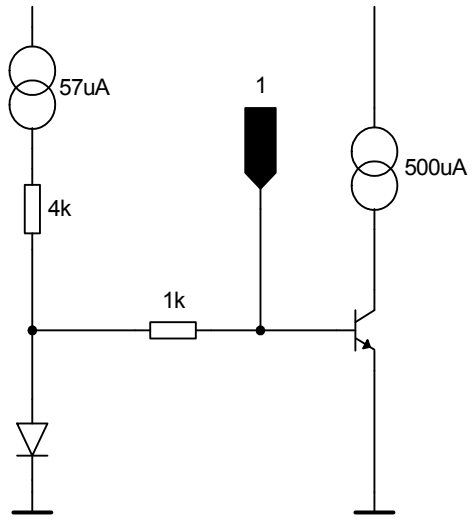
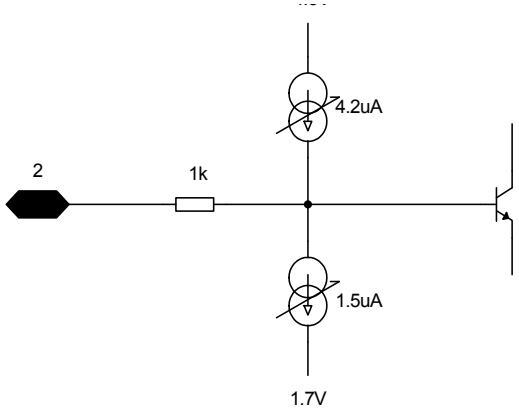
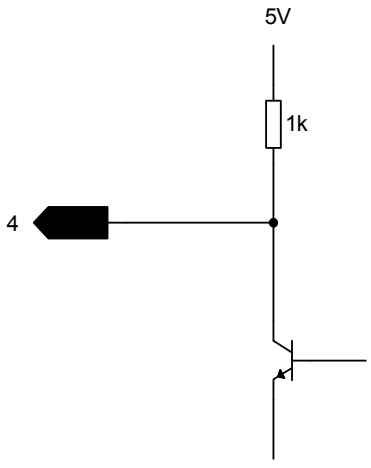
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	LNI		LNA Input
2	TAGC		AGC Time Constant Control
3	AGND1		Analogue Ground Return
4	LNO		LNA Output

Table 2 Pin Definition and Function (cont'd)

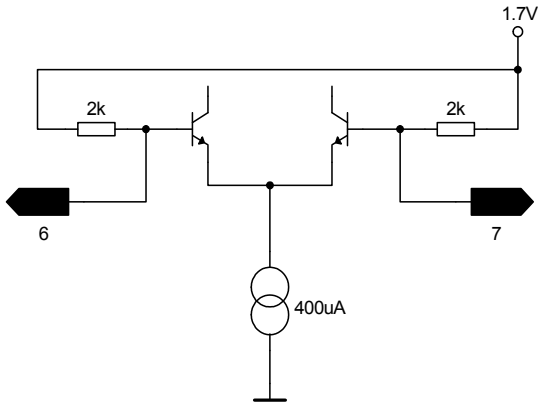
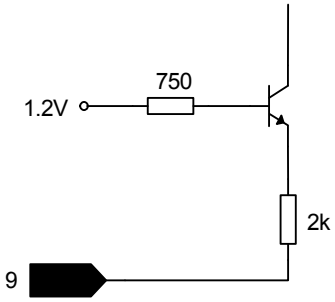
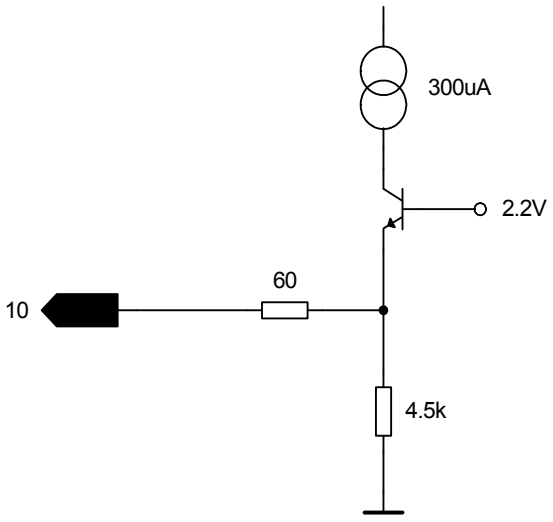
Pin No.	Symbol	Equivalent I/O-Schematic	Function
5	VCC1		5 V Supply
6	MI		Mixer Input
7	MIX		Complementary Mixer Input
8	AGND2		Analogue Ground Return
9	FSEL		868/434 MHz Operating Frequency Selector
10	IFO		10.7 MHz IF Mixer Output
11	GNDRF2		Internal GND Plane connected to RF-GND
12	DGND		Digital Ground Return
13	VDD		5 V Supply Digital

Table 2 Pin Definition and Function (cont'd)

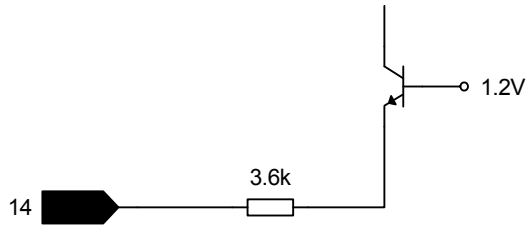
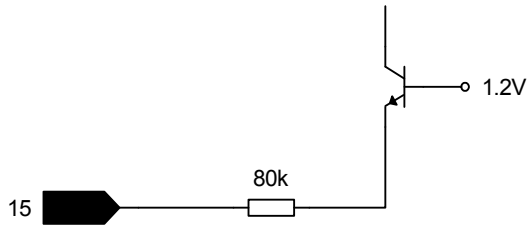
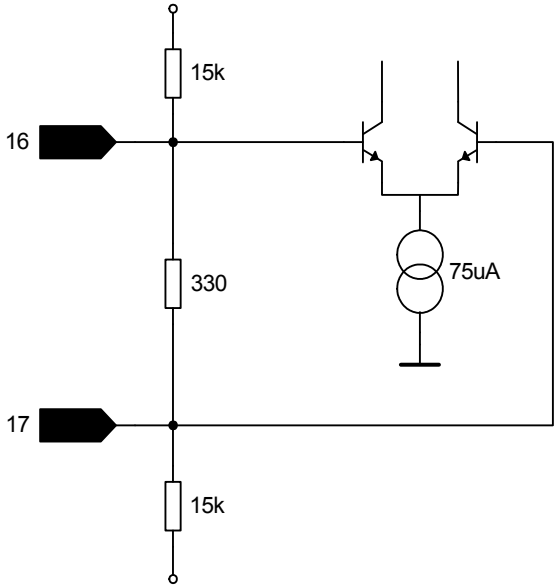
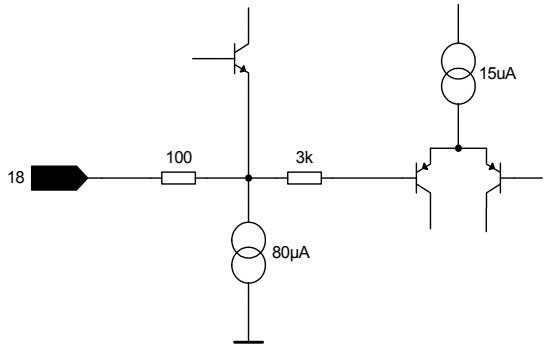
Pin No.	Symbol	Equivalent I/O-Schematic	Function
14	MSEL		ASK/FSK Modulation Format Selector
15	CSEL		6.xx or 13.xx MHz Quartz Selector
16	LIM		Limiter Input
17	LIMX		Complementary Limiter Input
18	SLP		Data Slicer Positive Input

Table 2 Pin Definition and Function (cont'd)

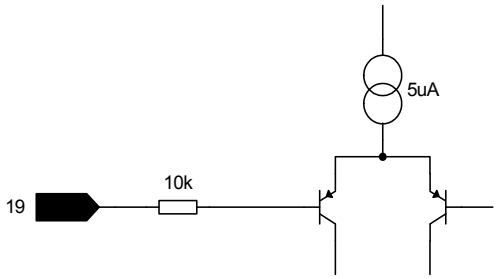
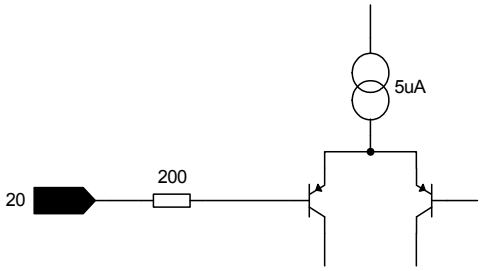
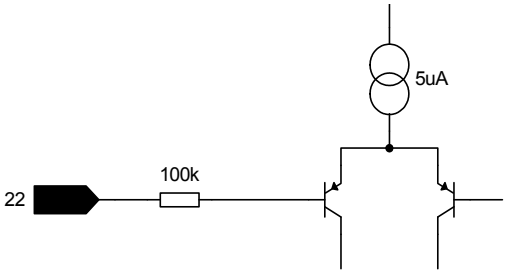
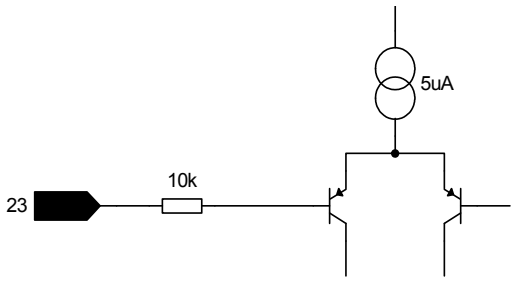
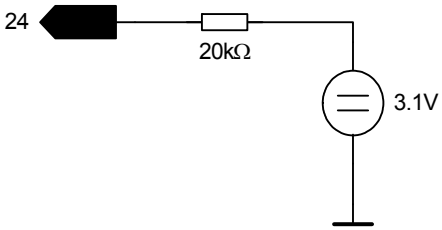
Pin No.	Symbol	Equivalent I/O-Schematic	Function
19	SLN		Data Slicer Negative Input
20	OPP		OpAmp Noninverting Input
21	GNDRF3		Internal GND Plane connected to RF-GND
22	FFB		Data Filter Feedback Pin
23	THRES		AGC Threshold Input
24	3VOUT		3 V Reference Output

Table 2 Pin Definition and Function (cont'd)

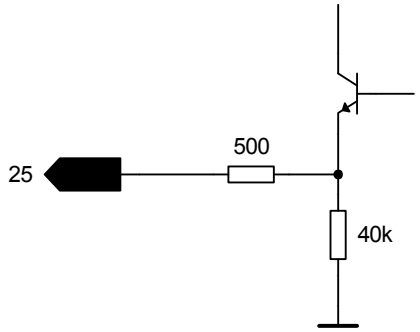
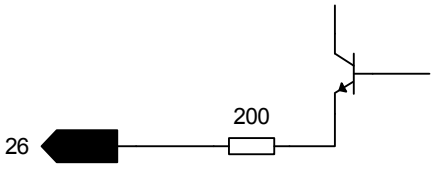
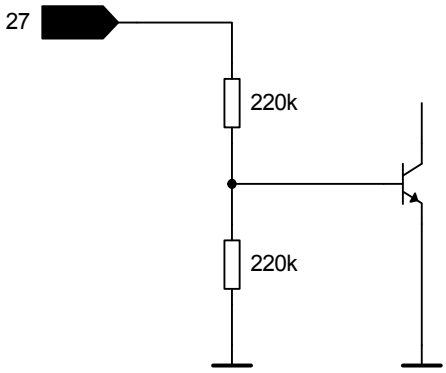
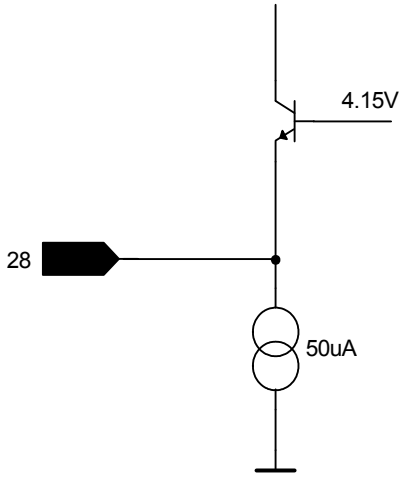
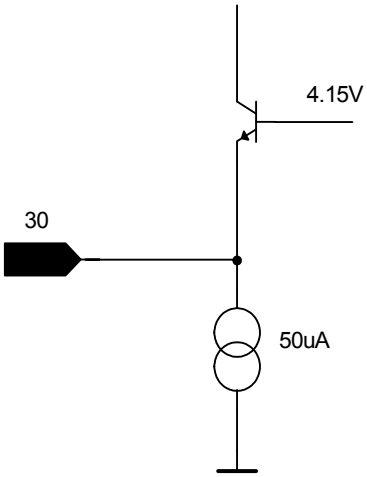
Pin No.	Symbol	Equivalent I/O-Schematic	Function
25	DATA		Data Output
26	PDO		Peak Detector Output
27	PDWN		Power Down Input
28	CRST2		External Crystal Connector 2
29	N.C.		Not connected

Table 2 Pin Definition and Function (cont'd)

Pin No.	Symbol	Equivalent I/O-Schematic	Function
30	CRST1		External Crystal Connector 1
31	VCC2		5 V Supply Analogue
32	GNDRF1		Internal GND Plane connected to RF-GND

2.3 Functional Block Diagram

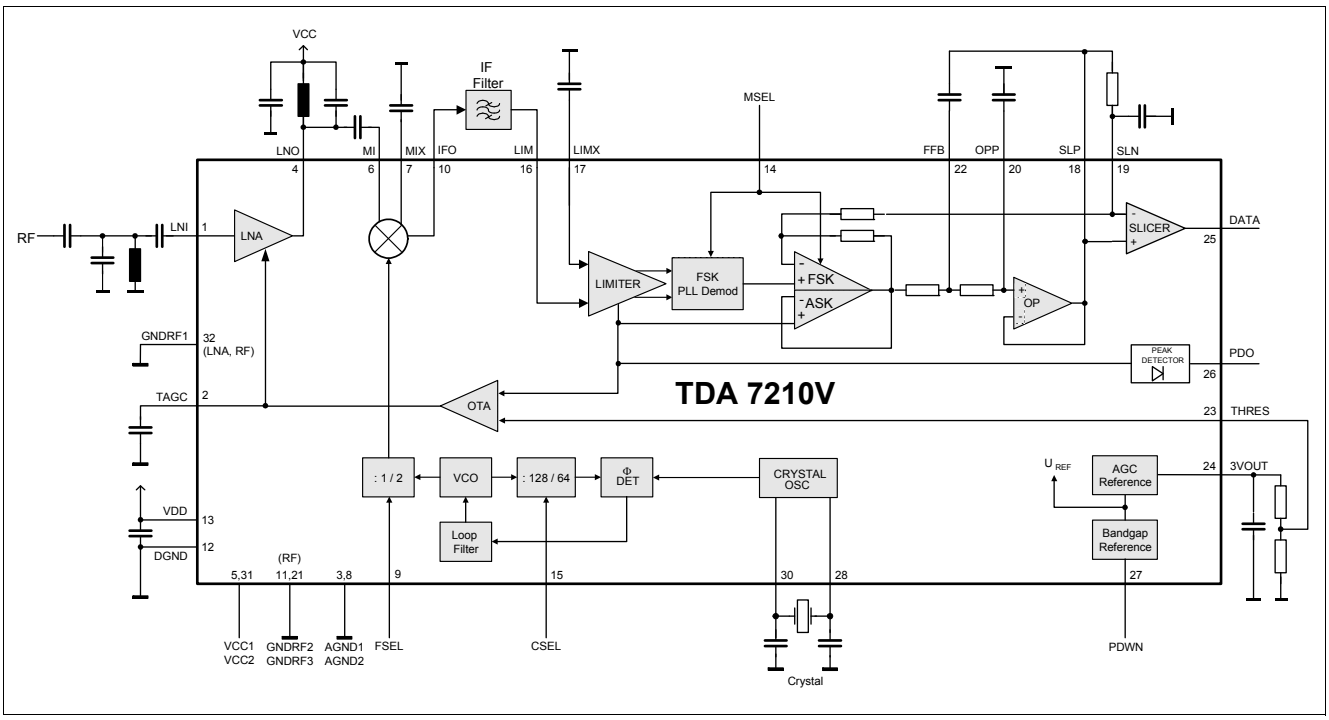


Figure 4 Main Block Diagram TDA7210V

2.4 Functional Blocks

2.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 20 to 27 dB (depending on the matching). The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output LNO (Pin 4) and the Mixer Inputs MI and MIX (Pins 6 and 7). The noise figure of the LNA is approximately 3 dB, the current consumption is 500 µA. The gain can be reduced by approximately 18 dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the THRES pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the 3VOUT pin (Pin 24) which provides a temperature stable 3 V output generated from the internal bandgap voltage and the THRES pin as described in **Chapter 3.1**. The time constant of the AGC action can be determined by connecting a capacitor to the TAGC pin (Pin 2) and should be chosen along with the appropriate threshold voltage according to the intended operating case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in **Chapter 3.1**.

2.4.2 Mixer

The Double Balanced Mixer downconverts the input frequency (RF) in the range of 400-440 MHz/810-870 MHz to the intermediate frequency (IF) at 10.7 MHz with a voltage gain of approximately 24 dB (depending on the matching) by utilising either high- or low-side injection of the local oscillator signal. In case the mixer is interfaced only single-ended, the unused mixer input has to be tied to ground via a capacitor. The mixer is followed by a low pass filter with a corner frequency of 20 MHz in order to suppress RF signals to appear at the IF output (IFO pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330 Ω to facilitate interfacing the pin directly to a standard 10.7 MHz ceramic filter without additional matching circuitry.

2.4.3 PLL Synthesizer

The Phase Locked Loop synthesiser consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including on-chip spiral inductors and varactor diodes. It's nominal centre frequency is 840 MHz, the operating range guaranteed over the temperature range specified is 820 to 860 MHz. Depending on whether high- or low-side injection of the local oscillator is used the receive frequency ranges are 810 to 840 MHz and 840 to 870 MHz or 400 to 420 MHz and 420 to 440 MHz (see also **Chapter 3.4**). No additional external components are necessary.
The oscillator signal is fed both to the synthesiser divider chain and to the downconverting mixer. In case of operation in the 400 to 440 MHz range, the signal is divided by two before it is fed to the mixer. This is controlled by the selection pin FSEL (Pin 9) as described in the following table. The overall division ratio of the divider chain can be selected to be either 128 or 64, depending on the frequency of the reference oscillator quartz (see below and **Chapter 3.4**). The loop filter is also realised fully on-chip.

Table 3 FSEL Pin Operating States

FSEL	RF Frequency
Open	400-440 MHz
Shorted to ground	810-870 MHz

2.4.4 Crystal Oscillator

The on-chip crystal oscillator circuitry allows for utilisation of quartzes both in the 6 and 13 MHz range as the overall division ratio of the PLL can be switched between 64 and 128 via the CSEL (Pin 15) pin according to the following table.

Table 4 CSEL Pin Operating States

CSEL	Crystal Frequency
Open	6.xx MHz
Shorted to ground	13.xx MHz

The calculation of the value of the necessary quartz load capacitance is shown in **Chapter 3.3**, the quartz frequency calculation is explained in **Chapter 3.4**.

2.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80 dB that has a bandpass-characteristic centred around 10.7 MHz. It has a typical input impedance of 330 Ω to allow for easy interfacing to a 10.7 MHz ceramic IF filter. The limiter circuit also acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in **Figure 6**. This signal is used to demodulate ASK-modulated receive signals in the subsequent baseband circuitry. The RSSI output is applied to the modulation format switch, to the Peak Detector input and to the AGC circuitry.

In order to demodulate ASK signals the MSEL pin has to be left open as described in the next chapter.

2.4.6 FSK Demodulator

To demodulate frequency shift keyed (FSK) signals a PLL circuit is used that is contained fully on chip. The Limiter output differential signal is fed to the linear phase detector as is the output of the 10.7 MHz center frequency VCO. The demodulator gain is typically 200 µV/kHz. The passive loop filter output that is comprised fully on chip is fed to both the VCO and the modulation format switch described in more detail below. This signal is representing the demodulated signal with high frequencies applied to the demodulator demodulated to logic ones and low frequencies demodulated to logic zeroes. Please note that due to this behaviour a sign inversion of the data occurs in case of high-side injection of the local oscillator at receive frequencies below 840 or 420 MHz, respectively.

The modulation format switch is actually a switchable amplifier with an AC gain of 11 that is controlled by the MSEL pin (Pin 14) as shown in the following table. This gain was chosen to facilitate detection in the subsequent circuits. The DC gain is 1 in order not to saturate the subsequent Data Filter wih the DC offset produced by the demodulator in case of large frequency offsets of the IF signal. The resulting frequency characteristic and details on the principle of operation of the switch are described in **Chapter 3.6**.

Table 5 MSEL Pin Operating States

MSEL	Modulation Format
Open	ASK
Shorted to ground	FSK

The demodulator circuit is switched off in case of reception of ASK signals.

2.4.7 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100 kHz used as a voltage follower and two 100 kΩ on-chip resistors. Along with two external capacitors a 2nd order Sallen-Key low pass filter is formed. The selection of the capacitor values is described in **Chapter 3.6**.

2.4.8 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of up to 100 kBaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for sbsequent circuits. The self-adjusting threshold on pin 19 its generated by RC-term or peak detector depending on the baseband coding scheme. The data slicer threshold generation alternatives are described in more detail in **Chapter 3.5**.

2.4.9 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. An external RC network is necessary. The input is connected to the output of the RSSI-output of the Limiter, the output is connected to the PDO pin (Pin 26). This output can be used as an indicator for the received signal strength to use in wake-up circuits and as a reference for the data slicer in ASK mode. Note that the RSSI level is also output in case of FSK mode.

2.4.10 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all subcircuits which is controlled by the PWDN pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50 nA.

Table 6 PDWN Pin Operating States

PDWN	Operating State
Open or tied to ground	Powerdown Mode
Tied to V_{CC}	Receiver On

3 Applications

3.1 Choice of LNA Threshold Voltage and Time Constant

In the following figure the internal circuitry of the LNA automatic gain control is shown.

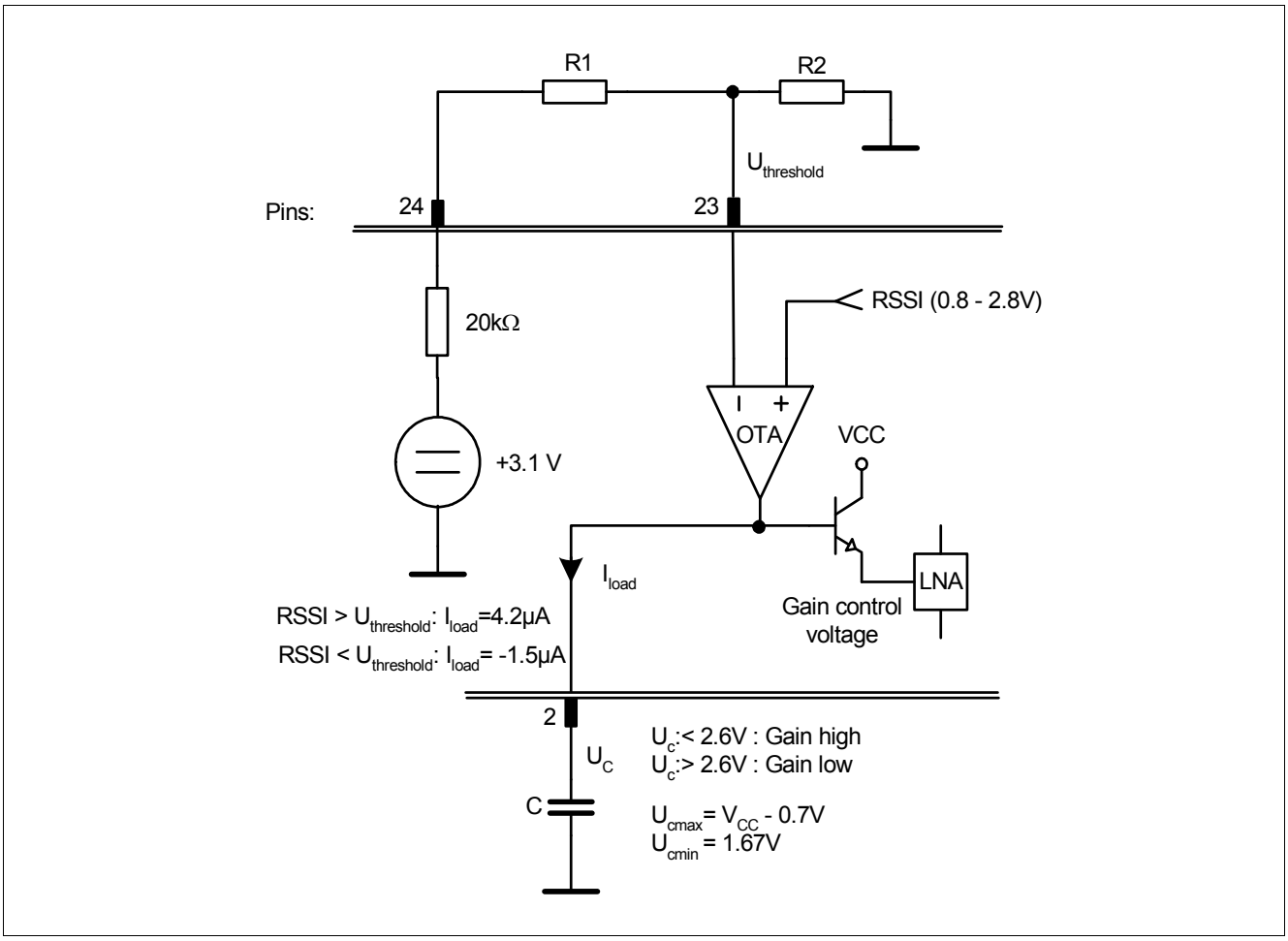


Figure 5 LNA Automatic Gain Control Circuitry

The LNA automatic gain control circuitry consists of an operational transimpedance amplifier that is used to compare the received signal strength signal (RSSI) generated by the Limiter with an externally provided threshold voltage Uthres. As shown in the following figure the threshold voltage can have any value between approximately 0.8 and 2.8 V to provide a switching point within the receive signal dynamic range.

This voltage Uthres is applied to the THRES pin (Pin 23) The threshold voltage can be generated by attaching a voltage divider between the 3VOUT pin (Pin 24) which provides a temperature stable 3 V output generated from the internal bandgap voltage and the THRES pin. If the RSSI level generated by the Limiter is higher than Uthres, the OTA generates a positive current Iload. This yields a voltage rise on the TAGC pin (Pin 2). Otherwise, the OTA generates a negative current. These currents do not have the same values in order to achieve a fast-attack and slow-release action of the AGC and are used to charge an external capacitor which finally generates the LNA gain control voltage.

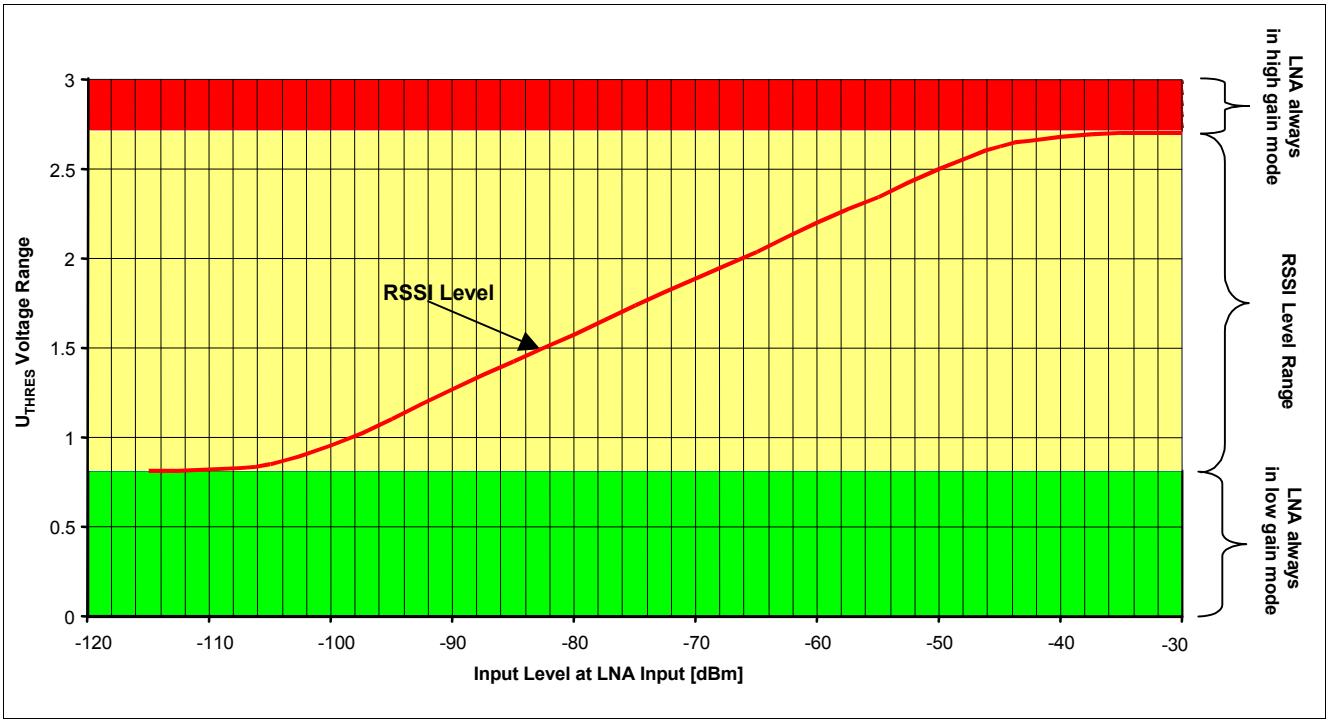


Figure 6 RSSI Level and Permissive AGC Threshold Levels

The switching point should be chosen according to the intended operating scenario. The determination of the optimum point is described in the accompanying Application Note, a threshold voltage level of 1.8 V is apparently a viable choice. It should be noted that the output of the 3VOUT pin is capable of driving up to 50 µA, but that the THRES pin input current is only in the region of 40 nA. As the current drawn out of the 3VOUT pin is directly related to the receiver power consumption, the power divider resistors should have high impedance values. The sum of R1 and R2 has to be 600 kΩ in order to yield 3 V at the 3VOUT pin. R1 can thus be chosen as 240 kΩ, R2 as 360 kΩ to yield an overall 3VOUT output current of 5 µA[1)] and a threshold voltage of 1.8 V.

Note: If the LNA gain shall be kept in either high or low gain mode this has to be accomplished by tying the THRES pin to a fixed voltage. In order to achieve always high gain mode operation, a voltage of at least 2.9 V or higher shall be applied to the THRES pin, such as a short to the 3VOUT pin. In order to achieve low gain mode operation a voltage lower than 0.7 V (depending on the matching and IF-filter) shall be applied to the THRES, such as a short to ground.

As stated above the capacitor connected to the TAGC pin is generating the gain control voltage of the LNA due to the charging and discharging currents of the OTA and thus is also responsible for the AGC time constant. As the charging and discharging currents are not equal two different time constants will result. The time constant corresponding to the charging process of the capacitor shall be chosen according to the data rate. According to measurements performed at Infineon the capacitor value should be higher than 47 nF.

1) Note the 20 kΩ resistor in series with the 3.1 V internal voltage source

3.2 Data Filter Design

Utilising the on-board voltage follower and the two 100 kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pins 18 (SLP) and 22 (FFB) and to pin 20 (OPP) as depicted in the following figure and described in the following formulas[1)].

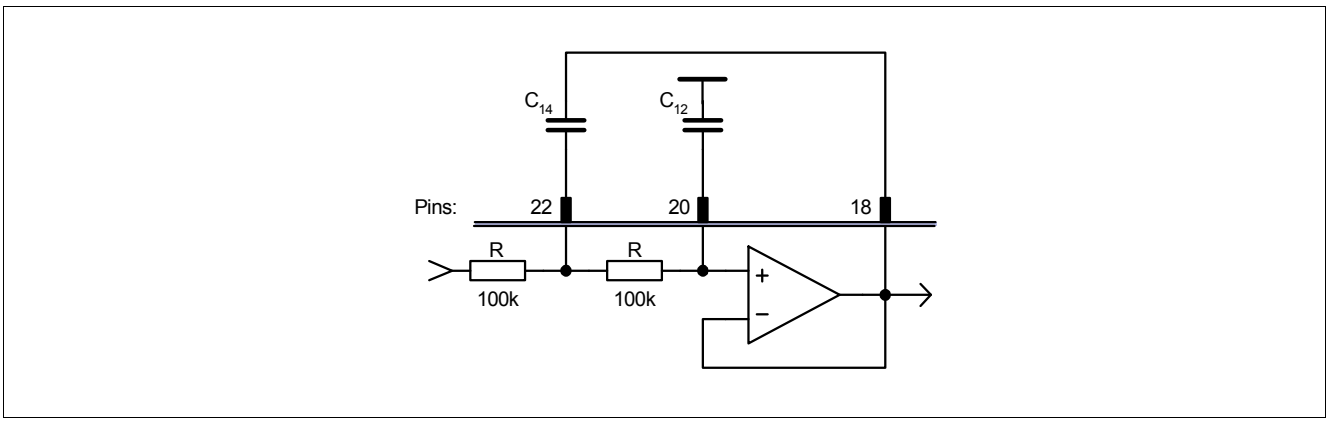


Figure 7 Data Filter Design

$$C12 = \frac{\sqrt{b}}{4QR\pi f_{3dB}} \tag{1}$$

$$C14 = \frac{2Q\sqrt{b}}{R2\pi f_{3dB}} \tag{2}$$

with

$$Q = \frac{\sqrt{b}}{a} \tag{3}$$

the quality factor of the poles, where in case of a Bessel filter a = 1.3617, b = 0.618

and thus Q = 0.577

and in case of a Butterworth filter a = 1.414, b = 1

and thus Q = 0.71

Example

Butterworth filter with f_{3dB} = 5 kHz and R = 100 kΩ:

C14 = 450 pF, C12 = 225 pF

1) Taken from Tietze/Schenk: Halbleiterschaltungstechnik, Springer Berlin, 1999.

3.3 Quartz Load Capacitance Calculation

The value of the capacitor necessary to achieve that the quartz oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in **Chapter 4.1.3** and by the quartz specifications given by the quartz manufacturer.

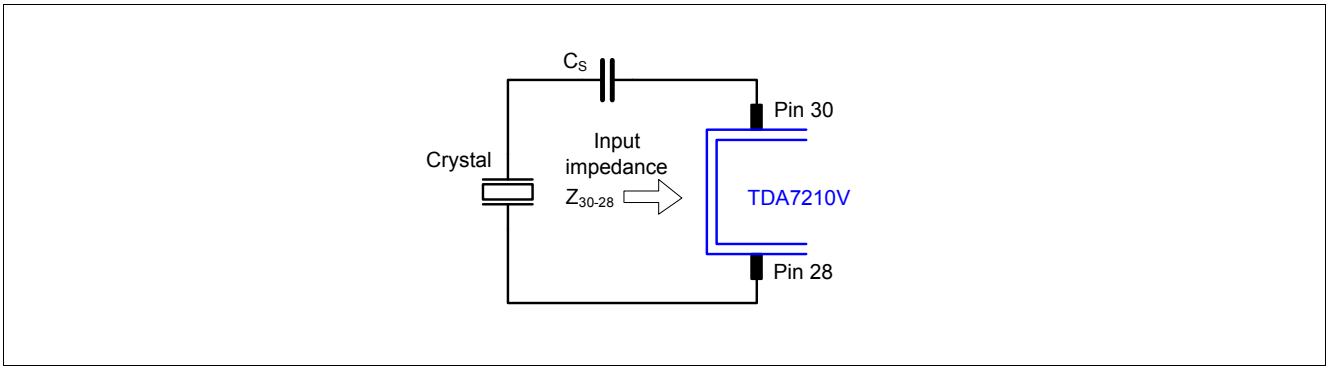


Figure 8 Determination of Series Capacitance Value for the Quartz Oscillator

Crystal specified with load capacitance

$$C_S = \frac{1}{\frac{1}{C_L} + 2\pi f X_L} \tag{4}$$

with CL the load capacitance (refer to the quartz crystal specification).

Examples

6.7 MHz: CL = 12 pF, XL=695 Ω, CS = 8.9 pF

13.4 MHz: CL = 12 pF, XL=1010 Ω, CS = 5.9 pF

These values may be obtained in high accuracy by putting two capacitors in series to the quartz, such as 22 pF and 15 pF in the 6.7 MHz case and 22 pF and 8.2 pF in the 13.4 MHz case.

But please note that the calculated value of CS includes the parasitic capacitors also.

3.4 Quartz Frequency Calculation

As described in **Chapter 2.4.3** the operating range of the on-chip VCO is 820 to 860 MHz with a nominal center frequency of 840 MHz. This signal is divided by 2 before applied to the mixer in case of operation at 434 MHz. This local oscillator signal can be used to downconvert the RF signals both with high- or low-side injection at the mixer. The resulting receive frequency ranges then extend between 810 and 870 MHz or between 400 and 440 MHz. Low-side injection of the local oscillator has to be used for receive frequencies between 840 and 870 MHz as well as high-side injection for receive frequencies below 840 MHz. Corresponding to that in the 400 MHz region low-side injection is applicable for receive frequencies above 420 MHz, high-side injection below this frequency. Therefore for operation both in the 868 and the 434 MHz ISM bands low-side injection of the local oscillator has to be used. Then the local oscillator frequency is calculated by subtracting the IF frequency (10.7 MHz) from the RF frequency (434 or 868 MHz). Please note that for low-side injection no sign-inversion occurs in case of reception and demodulation of FSK-modulated signals.

The overall division ratios in the PLL are 64 or 128 in case of operation at 868 MHz or 32 and 64 in case of operation at 434 MHz, depending on the crystal frequency used as shown below. The quartz frequency in case of low-side injection may be calculated by using the following formula:

$$f_{QU} = \frac{f_{RF} \pm 10.7}{r} \tag{5}$$

f_{RF} Receive frequency

f_{LO} Local oscillator (PLL) frequency (f_{RF} ± 10.7)

f_{QU} Quartz oscillator frequency

r Ratio of local oscillator (PLL) frequency and quartz, frequency as shown in the subsequent table.

Table 7 Dependence of PLL Overall Division Ratio on FSEL and CSEL

FSEL	CSEL	Ratio r = (fLO/fQU)
Open	Open	64
Open	GND	32
GND	Open	128
GND	GND	64

Example (low-side injection mode):

$$f_{QU} = (868.4MHz - 10.7MHz)/64 = 13.40156\,MHz \tag{6}$$

$$f_{QU} = (868.4MHz - 10.7MHz)/128 = 6.7008\,MHz \tag{7}$$

$$f_{QU} = (434.2\,MHz - 10.7MHz)/32 = 13.23437\,MHz \tag{8}$$

$$f_{QU} = (434.2\,MHz - 10.7MHz)/64 = 6.6172\,MHz \tag{9}$$

3.5 Data Slicer Threshold Generation

The threshold of the data slicer, especially for a coding scheme without DC-content, can be generated using an external R-C integrator as shown in Figure 9. The time constant TA of the R-C integrator has to be significantly larger than the longest period of no signal change TL within the data sequence. For the calculation of the time constant TA please see Application Note „TDA521x_ANV1.1“, chapter „4.11 Data Slicer“. In order to keep distortion low, the minimum value for R1 is 20 kΩ.

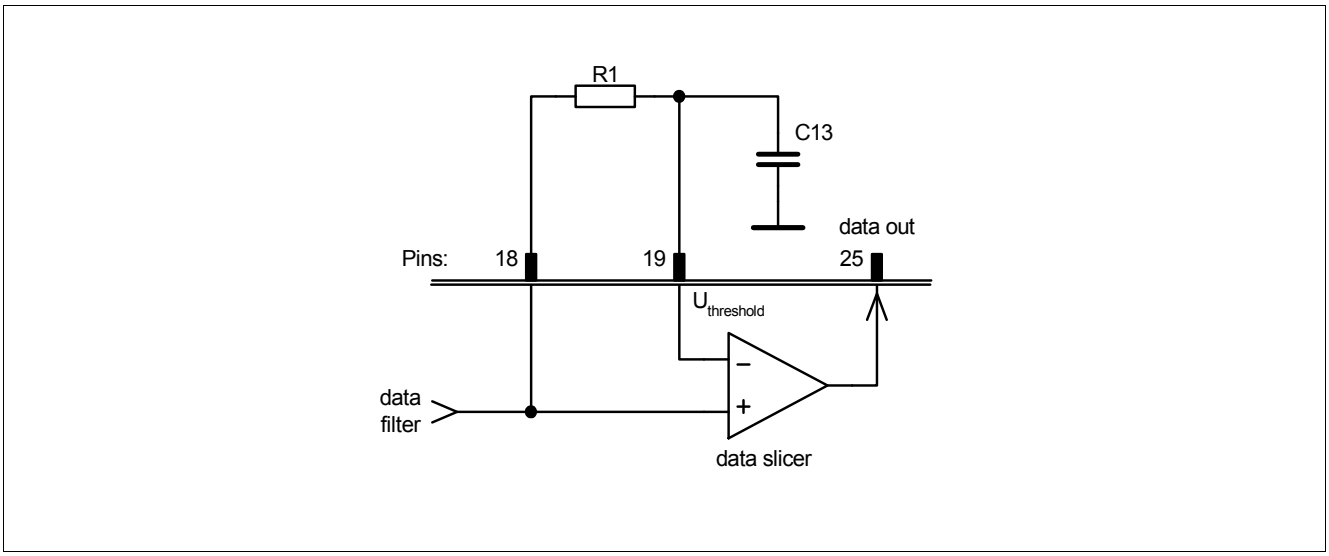


Figure 9 Data Slicer Threshold Generation with External R-C Integrator

In case of ASK operation another possibility for threshold generation is to use the peak detector in connection with two resistors and one capacitor as shown in the following figure. The component values are depending on the coding scheme and the protocol used.

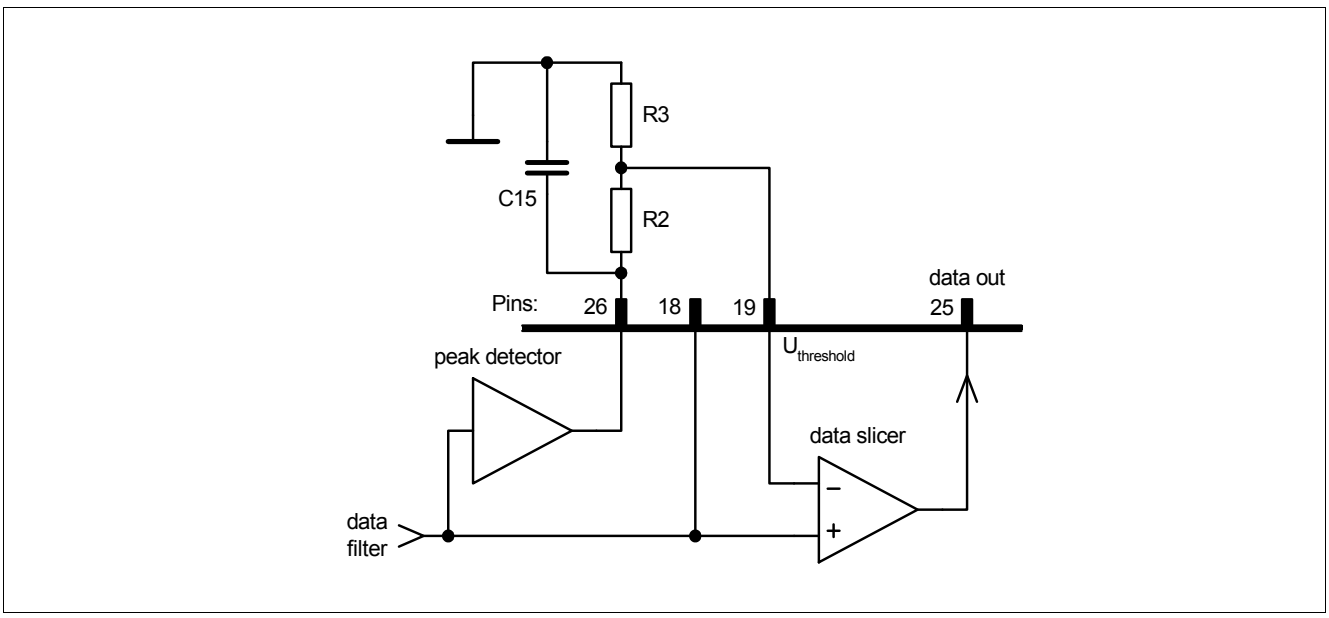


Figure 10 Data Slicer Threshold Generation Utilising the Peak Detector

3.6 ASK/FSK Switch Functional Description

The TDA7210V is containing an ASK/FSK switch which can be controlled via Pin 14 (MSEL). This switch is actually consisting of 2 operational amplifiers that are having a gain of 1 in case of the ASK amplifier and a gain of 11 in case of the FSK amplifier in order to achieve an appropriate demodulation gain characteristic. In order to compensate for the DC-offset generated especially in case of the FSK PLL demodulator there is a feedback connection between the threshold voltage of the bit slicer comparator (Pin 19) to the negative input of the FSK switch amplifier. This is shown in the following figure.

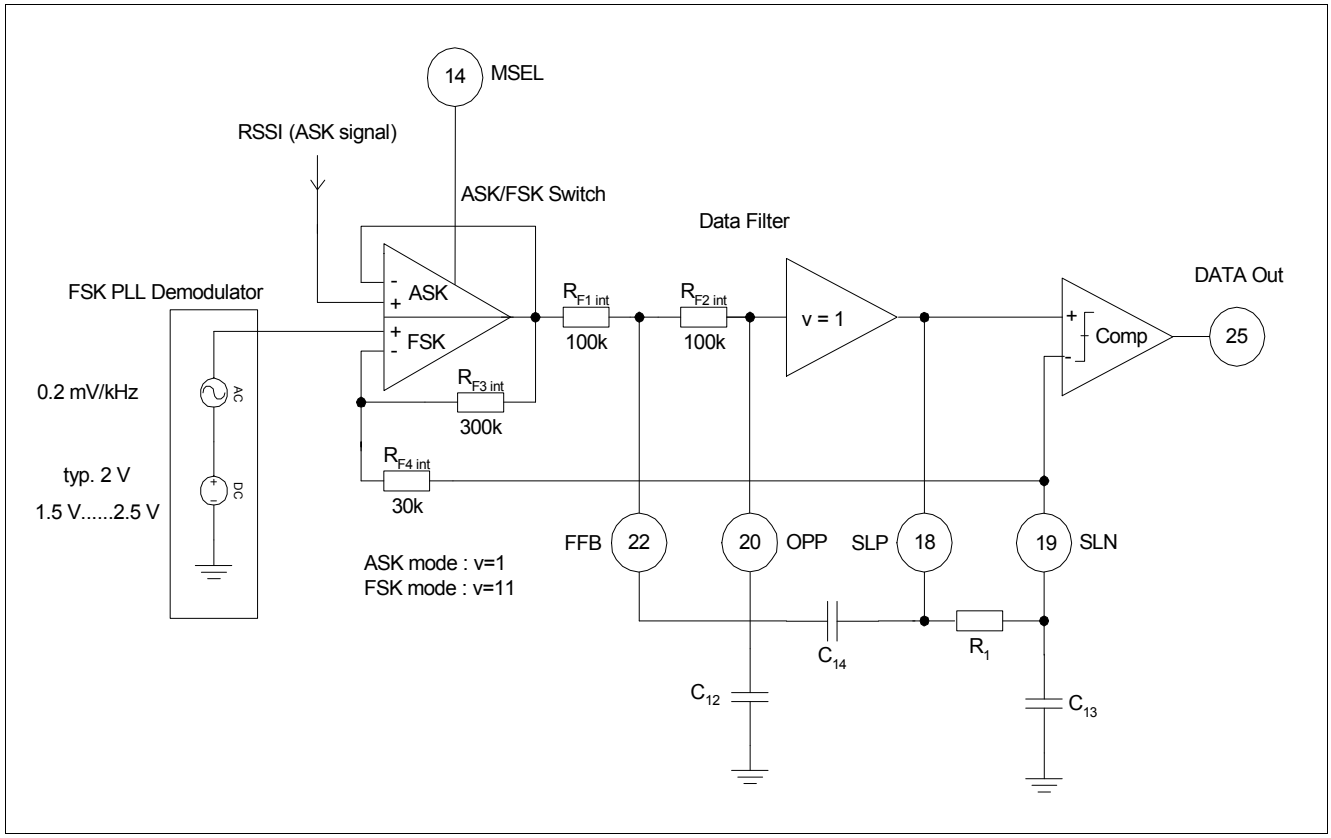


Figure 11 ASK/FSK Mode Datapath

3.6.1 FSK Mode

The FSK datapath has a bandpass characterisitc due to the feedback shown above (highpass) and the data filter (lowpass). The lower cutoff frequency f2 is determined by the external RC-combination. The upper cutoff frequency f3 is determined by the data filter bandwidth.

The demodulation gain of the FSK PLL demodulator is 200 µV/kHz. This gain is increased by the gain v of the FSK switch, which is 11. Therefore the resulting dynamic gain of this circuit is 2.2 mV/kHz within the bandpass. The gain for the DC content of FSK signal remains at 200 µV/kHz. The cutoff frequencies of the bandpass have to be chosen such that the spectrum of the data signal is influenced in an acceptable amount.

In case that the user data is containing long sequences of logical zeroes the effect of the drift-off of the bit slicer threshold voltage can be lowered if the offset voltage inherent at the negative input of the slicer comparator (Pin 19) is used. The comparator has no hysteresis built in.

This offset voltage is generated by the bias current of the negative input of the comparator (i.e. 20 nA) running over the external resistor R1. This voltage raises the voltage appearing at pin 19 (e.g. 1 mV with R1 = 100 kΩ). In order to obtain benefit of this asymmetrical offset for the demodulation of long zeros the lower of the two FSK frequencies should be chosen in the transmitter as the zero-symbol frequency.

In the following figure the shape of the above mentioned bandpass is shown.

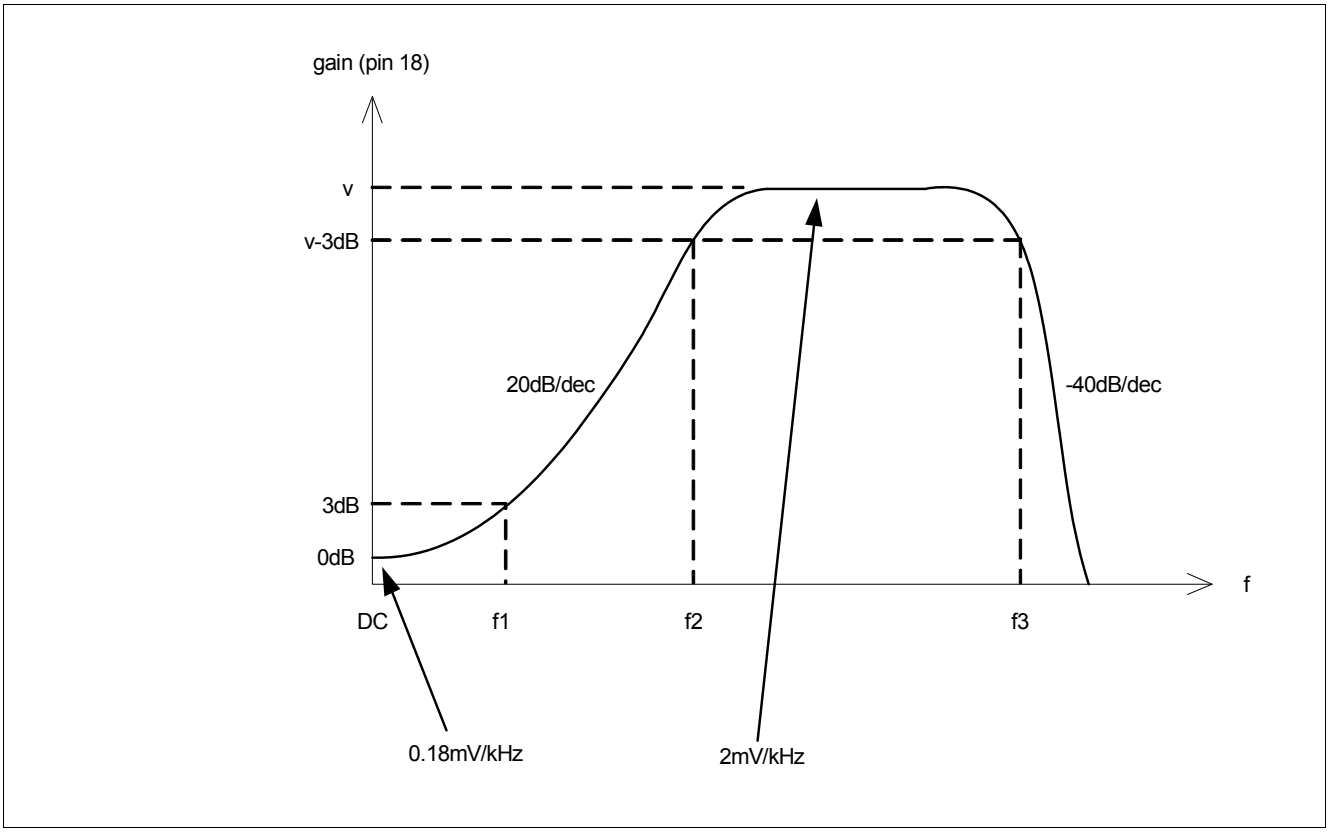


Figure 12 Frequency Characterstic in Case of FSK Mode

The cutoff frequencies are calculated with the following formulas:

$$f_1 = \frac{1}{2\pi \frac{R1 \cdot 330\,k\Omega}{R1 + 330\,k\Omega} \cdot C13} \tag{10}$$

$$f_2 = v \cdot f_1 = 11 \cdot f_1 \tag{11}$$

$$f_3 = f_{3dB} \tag{12}$$

f3 is the 3dB cutoff frequency of the data filter - see Section 3.2.

Example:
R1 = 100 kΩ, C13 = 47 nF
This leads to f1 = 44 Hz and f2 = 485 Hz

3.6.2 ASK Mode

In case the receiver is operated in ASK mode the datapath frequency charactersitic is dominated by the data filter alone, thus it is lowpass shaped.The cutoff frequency is determined by the external capacitors C12 and C14 and the internal 100k resistors as described in **Chapter 3.2**.

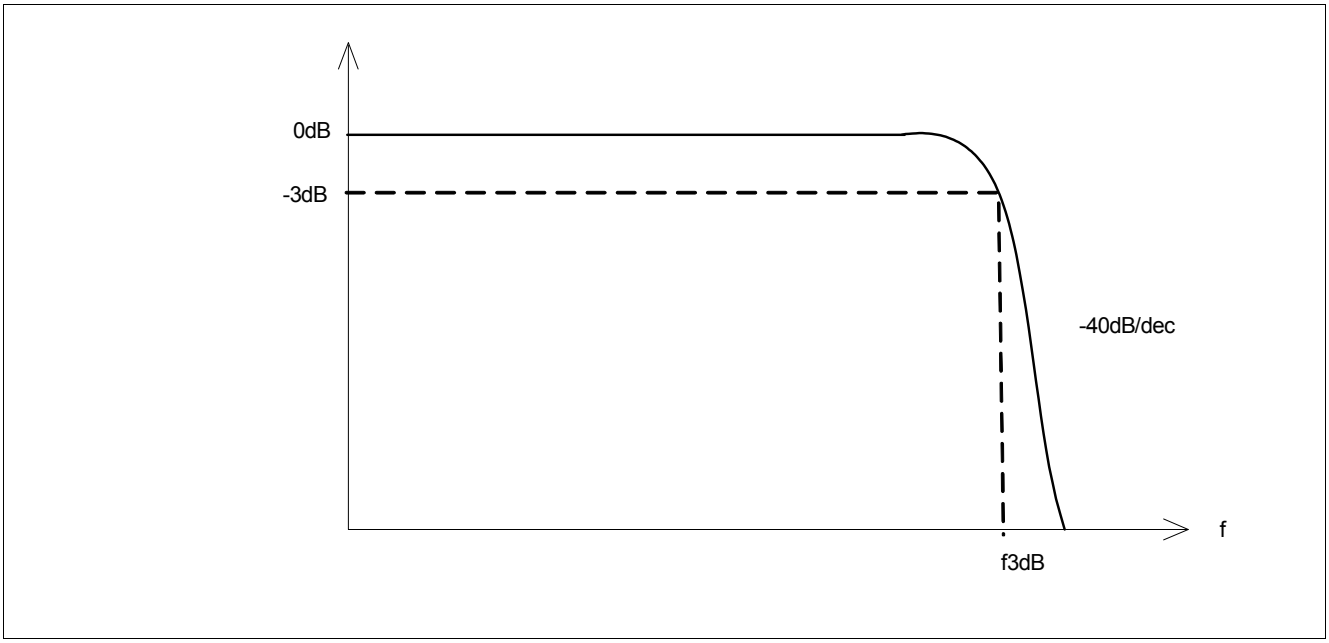


Figure 13 Frequency Charcteristic in Case of ASK Mode

3.7 Principle of the Precharge Circuit

In case the data slicer threshold shall be generated with an external RC network as described in **Chapter 3.5** it is necessary to use large values for the capacitor C13 attached to the SLN pin (pin 19) in order to achieve long time constants. This results also from the fact that the choice of the value for R1 connected between the SLP and SLN pins (pins 18 and 19) is limited by the 330 kΩ resistor appearing in parallel to R1 as can be seen in **Figure 11**. Apart from this a resistor value of 100 kΩ leads to a voltage offset of 1mV at the comparator input as described in **Chapter 3.6.1**. The resulting startup time constant t1 can be calculated with:

$$\tau_1 = \left(R1 \parallel 330\ k\Omega\right) \times C13 \tag{13}$$

In case R1 is chosen to be 100 kΩ and C13 is chosen as 47 nF this leads to

$$\tau_1 = \left(100k\Omega \parallel 330k\Omega\right) \times 47nF = 77k\Omega \times 47nF = 3.6ms \tag{14}$$

When the device is turned on this time constant dominates the time necessary for the device to be able to demodulate data properly. In the powerdown mode the capacitor is only discharged by leakage currents.

In order to reduce the turn-on time in the presence of large values of C13 a precharge circuit was included in the TDA7210V as shown in the following figure.

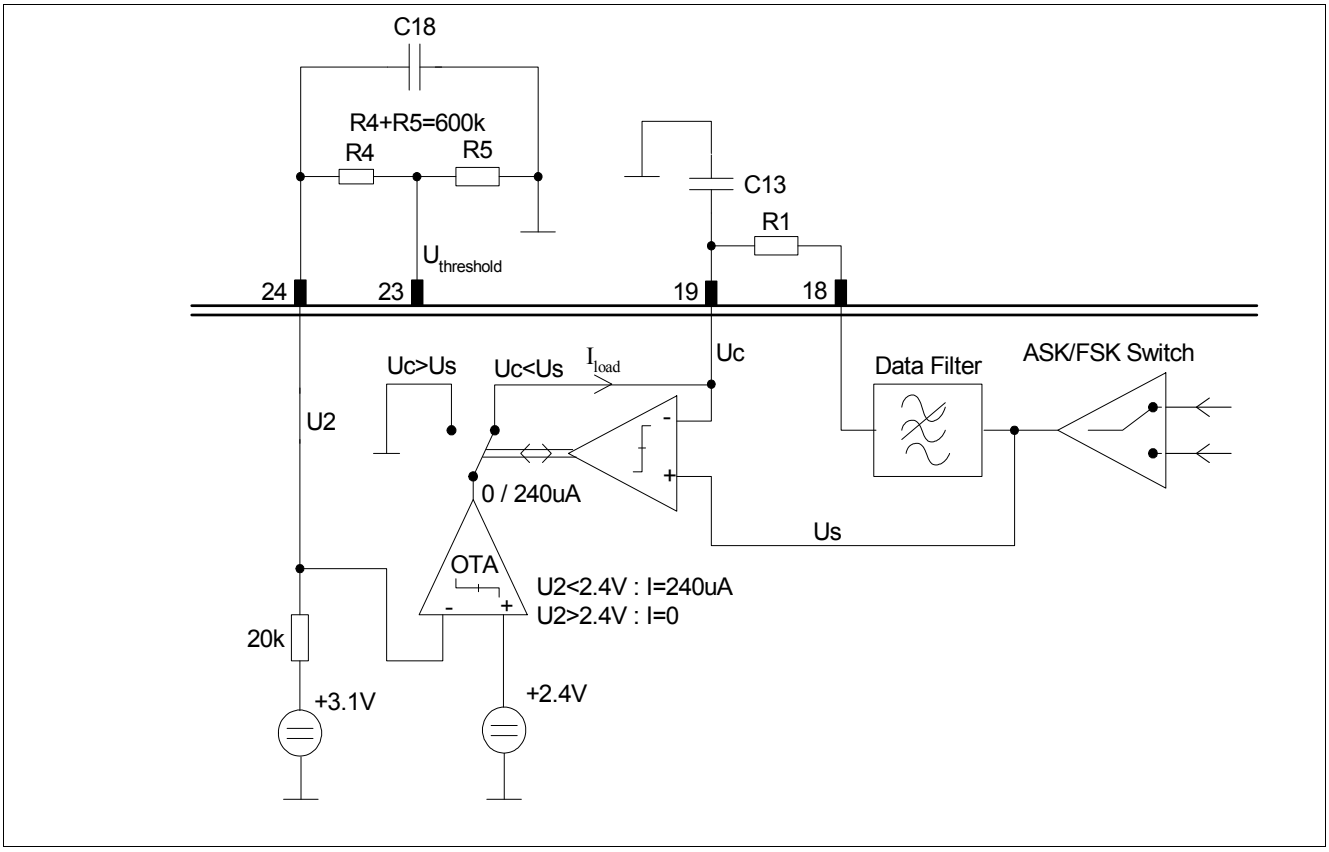


Figure 14 Principle of the Precharge Circuit

This circuit charges the capacitor C13 with an inrush current Iload of typically 220 µA for a duration of T2 until the voltage Uc appearing on the capacitor is equal to the voltage Us at the input of the data filter. This voltage is limited to 2.5 V. As soon as these voltages are equal or the duration T2 is exceeded the precharge circuit is disabled.

t2 is the time constant of the charging process of C18 which can be calculated as:

$$\tau_2 = 20k\Omega \times C18 \tag{15}$$

As the sum of R4 and R5 is sufficiently large and thus can be neglected. T2 can then be calculated according to the following formula:

$$T_l = \tau_2 \ln\left(\frac{1}{1-\frac{2.4V}{3V}}\right) \approx \tau_2 \times 1.6 \tag{16}$$

The voltage transient during the charging of C18 is shown in the following figure:

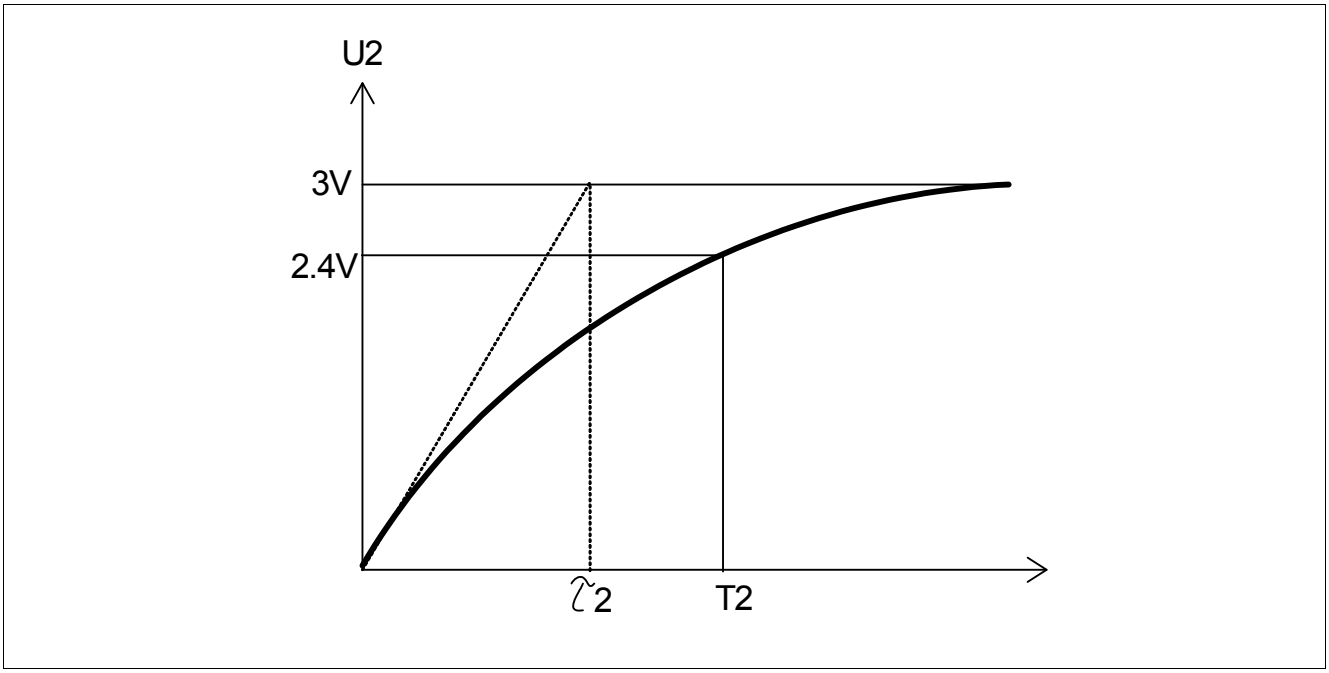


Figure 15 Voltage Appearing on C18 During Precharging Process

The voltage appearing on the capacitor C13 connected to pin 20 is shown in the following figure. It can be seen that due to the fact that it is charged by a constant current source it exhibits is a linear increase in voltage which is limited to USmax = 2.5 V which is also the approximate operating point of the data filter input. The time constant appearing in this case can be denoted as T3, which can be calculated with

$$T3 = \frac{U_{Smax} \cdot C13}{220\mu A} = \frac{2{,}5V}{220\mu A} \cdot C13 \tag{17}$$

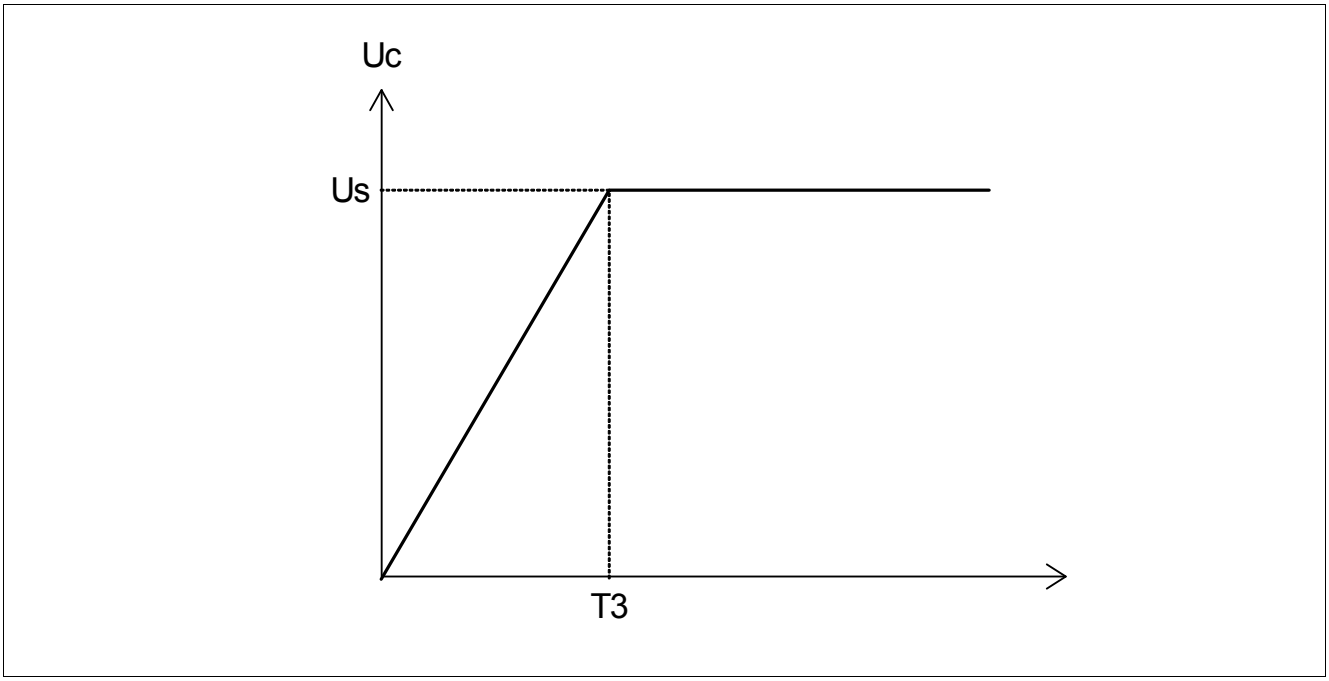


Figure 16 Voltage Transient on Capacitor C13 Attached to Pin 19

As an example the choice of C18 = 22 nF and C13 = 47 nF yields

t2 = 0.44 ms

T2 = 0.71 ms

T3 = 0.53 ms

This means that in this case the inrush current could flow for a duration of 0.64 ms but stops already after 0.49 ms when the USmax limit has been reached. T3 should always be chosen to be shorter than T2.

It has to be noted finally that during the turn-on duration T2 the overall device power consumption is increased by the 220 µA needed to charge C13.

The precharge circuit may be disabled if C18 is not equipped. This yields a T2 close to zero. Note that the sum of R4 and R5 has to be 600 kΩ in order to produce 3 V at the THRES pin as this voltage is internally used also as the reference for the FSK demodulator.

4 Electrical Characteristics

4.1 Electrical Data

4.1.1 Absolute Maximum Ratings

Attention: **TDA7210V is intended for use in general electronic equipment (AV equipment, telecommunication equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment) under a normal operation and use condition.**

Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 8 Absolute Maximum Ratings, Ambient temperature T_{AMB}=-40°C ... + 85°C

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply Voltage	V_{CC}	-0.3	–	5.5	V			1.1
Junction Temperature	T_j	-40	–	+125	°C			1.2
Storage Temperature	T_S	-40	–	+125	°C			1.3
Thermal Resistance	$R_{th\ JA}$	–	–	tbd.	K/W			1.4
ESD HBM integrity (all pins)	V_{ESD}	–	–	±2	kV	AEC Q100-002 EIA/JESD22-A114		1.5
ESD SDM integrity (all pins)	V_{ESD}	–	–	±500	V	AINSI/ESD5.3.2-2008		1.6
ESD SDM integrity (corner pins)	V_{ESD}	–	–	±750	V			1.7

4.1.2 Operating Range

Within the operational range the IC operates as explained in the circuit description. The AC/DC characteristic limits are not guaranteed. Currents flowing into the device are denoted as positive currents and v.v.

Supply voltage: V_{CC} = 4.5 V .. 5.5 V

Table 9 Operating Range, Ambient temperature T_{AMB}= -40°C ... + 85°C

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply Current	$I_{SF\ 868}$	4.1	–	7.7	mA	f_{RF} = 868 MHz, FSK Mode		2.1
	$I_{SF\ 434}$	3.9	–	7.5	mA	f_{RF} = 434 MHz, FSK Mode		2.2
	$I_{SA\ 868}$	3.4	–	7	mA	f_{RF} = 868 MHz, ASK Mode		2.3
	$I_{SA\ 434}$	3.2	–	6.8	mA	f_{RF} = 434 MHz, ASK Mode		2.4

Table 9 Operating Range, Ambient temperature T_{AMB}= -40°C ... + 85°C (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Receiver Input Level ASK,f_{RF}=434 MHz	RF_{in}	-116	–	-13	dBm	@ source imp. 50 Ω, BER 2E-3, average power level, Manchester enc. datarate 1 kBit, 280 kHz IF Bandwidth		2.5
Receiver Input Level FSK, frequ. dev. ± 50 kHz f_{RF}=434 MHz	RF_{in}	-113	–	-13	dBm		■	2.6
Receiver Input Level ASK, f_{RF}=868 MHz	RF_{in}	-112		-13		@ source impedance 50 Ω, BER 2E-3, average power level, Manchester encoded datarate 1 kBit, 280 kHz IF Bandwidth	■	2.7
Receiver Input Level FSK, frequ. dev. ± 50kHz f_{RF}=868 MHz	RF_{in}	-112		-13			■	2.8
LNI Input Frequency	f_{RF}	400/ 810	–	440/ 870	MHz			2.9
M/X Input Frequency	f_{MI}	400/ 810	–	440/ 870	MHz			2.10
3 dB IF Frequency Range ASK	$f_{IF\ -3dB}$	5	–	23	MHz		■	2.11
3 dB IF Frequency Range FSK	$f_{IF\ -3dB}$	10.4	–	11	MHz		■	2.12
Power Mode Standby	Standby	0	–	0.8	V			2.13
Power Mode On	ON	2.8	–	V_{CC}	V			2.14
Gain Control Voltage, LNA high gain state	V_{THRES}	2.8	–	V_{CC}-1	V			2.15
Gain Control Voltage, LNA low gain state	V_{THRES}	0	–	0.7	V			2.16

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.1.3 AC/DC Characteristics at T_{AMB} = 25°C

AC/DC characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production. Currents flowing into the device are denoted as positive currents and vice versa. The device performance parameters marked with ■ are not subject to production test. They were verified by design/characterization.

Table 10 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} = 4.5 ... 5.5 V

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply - Supply Current								
Supply Current Standby Mode	$I_{S\ PDWN}$	–	50	100	nA	Pin 27 (PDWN) open or tied to 0 V		3.1
Supply Current Device operating in 868 MHz range, FSK mode	$I_{SF\ 868}$	5.1	5.9	6.7	mA	Pin 9 (FSEL) tied to GND, Pin 14 (MSEL) tied to GND		3.2
Supply Current Device operating in 434 MHz range, FSK mode	$I_{SF\ 434}$	4.9	5.7	6.5	mA	Pin 9 (FSEL) open, Pin 14 (MSEL) tied to GND		3.3
Supply Current Device operating in 868 MHz range, ASK mode	$I_{SA\ 868}$	4.4	5.2	6	mA	Pin 9 (FSEL) tied to GND, Pin 14 (MSEL) open		3.4
Supply Current Device operating in 434 MHz range, ASK mode	$I_{SA\ 434}$	4.2	5	5.8	mA	Pin 9 (FSEL) open, Pin 14 (MSEL) open		3.5
LNA - Signal Input LNI (PIN 1), V_{THRES} > 2.8 V, high gain mode								
Average Power Level at BER = 2E-3 (Sensitivity) ASK f_{RF}=434 MHz	RF_{in}	–	-112	–	dBm	Manchester encoded datarate 4 kBit, 280 kHz IF Bandwidth	■	3.6
Average Power Level at BER = 2E-3 (Sensitivity) FSK f_{RF}=434 MHz	RF_{in}	–	-108	–	dBm	Manchester enc. datarate 4 kBit, 280 kHz IF Bandw.,± 50 kHz pk. dev.	■	3.7
Average Power Level at BER = 2E-3 (Sensitivity) ASK f_{RF}=868 MHz	RF_{in}	–	-108	–	dBm	Manchester encoded datarate 4 kBit, 280 kHz IF Bandwidth	■	3.8
Average Power Level at BER = 2E-3 (Sensitivity) FSK f_{RF}=868 MHz	RF_{in}	–	-107	–	dBm	Manchester enc. datarate 4 kBit, 280 kHz IF Bandw.,± 50 kHz pk. dev	■	3.9
Average Power Level at BER = 2E-3 (Sensitivity) ASK f_{RF}=434 MHz	RF_{in}	–	-115	–	dBm	Manchester encoded datarate 1 kBit, 280 kHz IF Bandwidth	■	3.10
Average Power Level at BER = 2E-3 (Sensitivity) FSK f_{RF}=434 MHz	RF_{in}	–	-112	–	dBm	Manchester enc. datarate 1 kBit, 280 kHz IF Bandw.,± 50 kHz pk. dev.	■	3.11
Average Power Level at BER = 2E-3 (Sensitivity) ASK f_{RF}=868 MHz	RF_{in}	–	-111	–	dBm	Manchester encoded datarate 1 kBit, 280 kHz IF Bandwidth	■	3.12

Table 10 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} = 4.5 ... 5.5 V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Average Power Level at BER = 2E-3 (Sensitivity) FSK f_{RF}=868 MHz	RF_{in}	–	-111	–	dBm	Manchester enc. datarate 1 kBit, 280 kHz IF Bandw.,± 50 kHz pk. dev.	■	3.13
Input impedance, f_{RF}=434 MHz	$S_{11\ LNA}$		0.890 / -36.3 deg				■	3.14
Input impedance, f_{RF}=868 MHz	$S_{11\ LNA}$		0.784 / -66.2 deg				■	3.15
Input level @ 1 dB C.P. f_{RF} = 434 MHz	$P1dB_{LNA}$	–	-16	–	dBm	Matched input	■	3.16
Input level @ 1 dB C.P. f_{RF} = 868 MHz	$P1dB_{LNA}$	–	-7	–	dBm	Matched input	■	3.17
Input 3rd order intercept point f_{RF}=434 MHz	$IIP3_{LNA}$	–	-21	–	dBm	Matched input	■	3.18
Input 3rd order intercept point f_{RF}=868 MHz	$IIP3_{LNA}$	–	-14	–	dBm	Matched input	■	3.19
LO signal feedthrough at antenna port	LO_{LNI}	–	-83	-73	dBm		■	3.20
LNA - Signal Output LNO (PIN 4), V_{THRES} > 2.8 V, high gain mode								
Gain f_{RF}=434 MHz	$S_{21\ LNA}$		1.497 / 137.0 deg				■	3.21
Gain f_{RF}=868 MHz	$S_{21\ LNA}$		1.298 / 103.7 deg				■	3.22
Output impedance, f_{RF}=434 MHz	$S_{22\ LNA}$		0.899 / -16.4 deg				■	3.23
Output impedance, f_{RF}=868 MHz	$S_{22\ LNA}$		0.885 / -25.7 deg				■	3.24
LNA- Signal Input LNI, V_{THRES} = GND, low gain mode								
Input impedance, f_{RF}=434 MHz	$S_{11\ LNA}$		0.896 / -37.1 deg				■	3.25
Input impedance, f_{RF}=868 MHz	$S_{11\ LNA}$		0.794 / -69.1 deg				■	3.26
Input level @ 1 dB C. P. f_{RF}=434 MHz	$P1dB_{LNA}$	–	-7	–	dBm	Matched input	■	3.27
Input level @ 1 dB C. P. f_{RF} = 868 MHz	$P1dB_{LNA}$	–	-3	–	dBm	Matched input	■	3.28

Table 10 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} = 4.5 ... 5.5 V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Input 3rd order intercept point f_{RF}=434 MHz	$IIP3_{LNA}$	–	-19	–	dBm	Matched input	■	3.29
Input 3rd order intercept point f_{RF}=868 MHz	$IIP3_{LNA}$	–	-13	–	dBm	Matched input	■	3.30
LNA - Signal Output LNO, V_{THRES} = GND, low gain mode								
Gain f_{RF}=434 MHz	$S_{21\ LNA}$		0.180 / 138.1 deg				■	3.31
Gain f_{RF}=868 MHz	$S_{21\ LNA}$		0.162 / 109.6 deg				■	3.32
Output impedance, f_{RF}=434 MHz	$S_{22\ LNA}$		0.904 / -16.0 deg				■	3.33
Output impedance, fRF=868 MHz	$S_{22\ LNA}$		0.888 / -26.4 deg				■	3.34
LNA - Antenna to IFO, V_{THRES} > 2.8 V, high gain mode								
Voltage Gain Antenna to IFO f_{RF}=434 MHz	$G_{Ant\text{-}IFO}$	–	51	–	dB			3.35
Voltage Gain Antenna to IFO f_{RF}=868 MHz	$G_{Ant\text{-}IFO}$	–	47	–	dB			3.36
LNA - Antenna to IFO, V_{THRES} = GND, low gain mode								
Voltage Gain Antenna to IFO f_{RF}=434 MHz	$G_{Ant\text{-}IFO}$	–	36	–	dB			3.37
Voltage Gain Antenna to IFO f_{RF}=868 MHz	$G_{Ant\text{-}IFO}$	–	28	–	dB			3.38
3VOUT - Signal 3VOUT (PIN 24)								
Output voltage	V_{3VOUT}	2.9	3.1	3.3	V	3VOUT Pin open		3.39
Current out	I_{3VOUT}	-3	-5	-10	µA	See **Chapter 3**.		3.40
AGC - Signal THRES (PIN 23)								
Input Voltage range	V_{THRES}	0	–	V_{CC}-1	V	See **Chapter 3**.		3.41
LNA low gain mode	V_{THRES}	0	–	–	V			3.42
LNA high gain mode	V_{THRES}	2.9	3.0	V_{CC}-1	V	Voltage must not be higher than V_{CC}-1 V		3.43
Current in	I_{THRES_in}	–	5	–	nA	µA	■	3.44
AGC - Signal TAGC (PIN 2)								
Current out LNA low gain state	I_{TAGC_out}	-3.6	-4.2	-5	µA	RSSI > V_{THRES}		3.45
Current in LNA high gain state	I_{TAGC_in}	1	1.5	2.2	µA	RSSI<V_{THRES}		3.46

Table 10 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} = 4.5 ... 5.5 V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
MIXER - Signal Input MI/MIX (PINS 6/7)								
Input impedance, f_{RF}=434 MHz	$S_{11\ MIX}$		0.936 / -15.2 deg				■	3.47
Input impedance, f_{RF}=868 MHz	$S_{11\ MIX}$		0.917 / -27.6 deg				■	3.48
Input 3rd order intercept point f_{RF}=434 MHz	$IIP3_{MIX}$	–	-42	–	dBm		■	3.49
Input 3rd order intercept point f_{RF}=868 MHz	$IIP3_{MIX}$	–	-42	–	dBm		■	3.50
MIXER - Signal Output IFO (PIN 10)								
Output impedance	Z_{IFO}	–	330	–	Ω		■	3.51
Conversion Voltage Gain $f_{RF=}$434 MHz	G_{MIX}	–	24	–	dB			3.52
Conversion Voltage Gain f_{RF}=868 MHz	G_{MIX}	–	31	–	dB			3.53
LIMITER - Signal Input LIM/X (PINS 16/17)								
Input Impedance	Z_{LIM}	264	330	396	Ω		■	3.54
RSSI dynamic range	DR_{RSSI}	60	–	80	dB		■	3.55
RSSI linearity	$LIN_{RSS}I$	–	±1	–	dB		■	3.56
Operating frequency (3 dB points)	f_{LIM}	5	10.7	23	MHz		■	3.57
LIMITER - DATA FILTER								
Useable bandwidth	$BW_{BB\ FILT}$	–	–	100	kHz		■	3.58
RSSI Level at Data Filter Output SLP, RFIN=-103 dBm	$RSSI_{low}$	–	1.39	–	V	LNA in high gain mode RF=434 MHz		3.59
RSSI Level at Data Filter Output SLP, RFIN=-30 dBm	$RSSI_{high}$	–	2.79	–	V	LNA in high gain mode RF=434 MHz		3.60
SLICER - Signal Output DATA (PIN 25)								
Maximum Datarate	DR_{max}	–	–	100	kB/s	NRZ, 20 pF capacitive loading	■	3.61
LOW output voltage	V_{SLIC_L}	0	–	0.1	V			3.62
HIGH output voltage	V_{SLIC_H}	V_{CC}-1.3	V_{CC}-1	V_{CC}-0.7	V	Output current = 200 µA		3.63
SLICER - Signal SLN (PIN 19)								
Precharge Current Out	I_{PCH_SLN}	-100	-220	-300	µA	See **Chapter 3**.		3.64
PEAK DETECTOR - Signal Output PDO (PIN 26)								

Table 10 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} = 4.5 ... 5.5 V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Load current	I_{load}	-500	–	–	µA	Static load current must not exceed -500 µA		3.65
Leakage current	$I_{leakage}$	0	200	1000	nA			3.66
CRYSTAL OSCILLATOR - Signals CRST1, CRST2, (PINS 30/28)								
Operating frequency	f_{CRSTL}	6	–	14	MHz	Fundamental mode, series resonance		3.67
Input Impedance @ ~6MHz	Z_{1-28}	–	-825 +j695	–	Ω		■	3.68
Input Impedance @ ~13MHz	Z_{1-28}	–	-600 +j1010	–	Ω		■	3.69
Serial Capacity @ ~6MHz	$C_{S\,6}$=C1	–	8.9	–	pF			3.70
Serial Capacity @ ~13MHz	C_{S13}=C1	–	5.9	–	pF			3.71
ASK/FSK SIGNAL SWITCH - Signal MSEL (PIN 14)								
ASK Mode	V_{MSEL}	1.4	–	4[1)]	V	Or open		3.72
FSK Mode	V_{MSEL}	0	–	0.2	V			3.73
FSK DEMODULATOR								
Demodulation Gain	G_{FMDEM}	–	200	–	µV/ kHz			3.74
Useable IF Bandwidth	BW_{IFPLL}	10.2	10.7	11.2	MHz			3.75
POWER DOWN MODE - Signal PDWN (PIN 27)								
Power Mode On	ON	2.8	–	V_{CC}	V			3.76
Power Mode Standby	Standby	0	–	0.8	V			3.77
Input bias current PDWN	I_{PDWN}	–	19	–	µA	Power On Mode		3.78
Start-up Time until valid signal is detected at IF	T_{SU}	–	<1	–	ms	Depends on the used crystal		3.79
VCO MULTIPLEXER - Signal FSEL (PIN 9)								
f_{RF} range 434 MHz	V_{FSEL}	1.4	–	4[1)]	V	Or open		3.80
f_{RF} range 868 MHz	V_{FSEL}	0	–	0.2	V			3.81
Output bias current FSEL	I_{FSEL}	-160	-200	-240	µA	FSEL tied to GND		3.82
PLL DIVIDER - Signal CSEL (PIN 15)								
f_{CRSTL} range 6.xxMHz	V_{CSEL}	1.4	–	4[1)]	V	or open		3.83
f_{CRSTL} range 13.xxMHz	V_{CSEL}	0	–	0.2	V			3.84
Input bias current CSEL	I_{CSEL}	-3	-5	-7	µA	CSEL tied to GND		3.85

1) Maximum voltage in Power-On state is 4 V, but in PDWN-state the maximum voltage is 2.8 V.

Attention: Test ■ means that the parameter is not subject to production test.
It was verified by design/characterization.

4.1.4 AC/DC Characteristics at T_{AMB} = -40 to 85°C

Currents flowing into the device are denoted as positive currents and vice versa.

Table 11 AC/DC Characteristics with T_{AMB}= -40°C ... + 85°C, V_{CC} = 4.5 ... 5.5 V

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply - Supply Current								
Supply Current Standby Mode	$I_{S\ PDWN}$	–	50	400	nA	Pin 27 (PDWN) open or tied to 0 V		4.1
Supply Current Device operating in 868 MHz range, FSK mode	$I_{SF\ 868}$	4.1	5.9	7.7	mA	Pin 9 (FSEL) tied to GND, Pin 14 (MSEL) tied to GND		4.2
Supply Current Device operating in 434 MHz range, FSK mode	$I_{SF\ 434}$	3.9	5.7	7.5	mA	Pin 9 (FSEL) open, Pin 14 (MSEL) tied to GND		4.3
Supply Current Device operating in 868 MHz range, ASK mode	$I_{SA\ 868}$	3.4	5.2	7	mA	Pin 9 (FSEL) tied to GND, Pin 14 (MSEL) open		4.4
Supply Current Device operating in 434 MHz range, ASK mode	$I_{SA\ 434}$	3.2	5	6.8	mA	Pin 9 (FSEL) open, Pin 14 (MSEL) open		4.5
3VOUT - Signal 3VOUT (PIN 24)								
Output voltage	V_{3VOUT}	2.9	3.1	3.3	V	3VOUT Pin open		4.6
Current out	I_{3VOUT}	-3	-5	-10	µA	See **Chapter 3**.		4.7
AGC - Signal THRES (PIN 23)								
Input Voltage range	V_{THRES}	0	–	V_{CC}-1	V	See **Chapter 3**.		4.8
LNA low gain mode	V_{THRES}	0	–	0.3	V			4.9
LNA high gain mode	V_{THRES}	2.9	3	3.3	V	Voltage must not be higher than VCC-1V		4.10
Current in	I_{THRES_in}	–	5	–	nA		■	4.11
AGC - Signal TAGC (PIN 2)								
Current out LNA low gain state	I_{TAGC_out}	-1	-4.2	-8	µA	RSSI > V_{THRES}		4.12
Current in LNA high gain state	I_{TAGC_in}	0.5	1.5	5	µA	RSSI<V_{THRES}		4.13
MIXER								
Conversion Voltage Gain f_{RF}=434 MHz	G_{MIX}	–	24	–	dB			4.14
Conversion Voltage Gain f_{RF}=868 MHz	G_{MIX}	–	32	–	dB			4.15

Table 11 AC/DC Characteristics with T_{AMB}= -40°C ... + 85°C, V_{CC} = 4.5 ... 5.5 V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
LIMITER - Signal Input LIM/X (PINS 16/17)								
RSSI dynamic range	DR_{RSSI}	60	–	80	dB			4.16
LIMITER - DATA FILTER								
RSSI Level at Data Filter Output SLP, RFIN=-103 dBm	$RSSI_{low}$	–	1.39	–	dB	LNA in high gain mode RF=434 MHz		4.17
RSSI Level at Data Filter Output SLP, RFIN=-30 dBm	$RSSI_{high}$	–	2.79	–	dB	LNA in high gain mode RF=434 MHz		4.18
SLICER - Signal Output DATA (PIN 25)								
Maximum Datarate	DR_{max}	–	–	100	kB/s	NRZ, 20 pF capacitive loading	■	4.19
LOW output voltage	V_{SLIC_L}	0	–	0.1	V			4.20
HIGH output voltage	V_{SLIC_H}	V_{CC}-1.5	V_{CC}-1	V_{CC}-0.5	V	Output current = 200 µA		4.21
SLICER - Signal SLN (PIN 19)								
Precharge Current Out	I_{PCH_SLN}	-100	-220	-300	µA	See **Chapter 3**.		4.22
PEAK DETECTOR - Signal Output PDO (PIN 26)								
Load current	I_{load}	-400	–	–	µA	Static load current must not exceed -500 µA		4.23
Leakage current	$I_{leakage}$	0	700	2000	nA			4.24
CRYSTAL OSCILLATOR - Signals CRST1, CRST2, (PINS 30/28)								
Operating frequency	f_{CRSTL}	6	–	14	MHz	Fundamental mode, series resonance		4.25
ASK/FSK SIGNAL SWITCH - Signal MSEL (PIN 14)								
ASK Mode	V_{MSEL}	1.4	–	4[1)]	V	Or open		4.26
FSK Mode	V_{MSEL}	0	–	0.2	V			4.27
FSK DEMODULATOR								
Demodulation Gain	G_{FMDEM}	–	200	–	µV/ kHz			4.28
Useable IF Bandwidth	BW_{IFPLL}	10.2	10.7	11.2	MHz			4.29
POWER DOWN MODE - Signal PDWN (PIN 27)								
Power Mode On	ON	2.8	–	V_{CC}	V			4.30
Power Mode Standby	Standby	0	–	0.8	V			4.31
Start-up Time until valid signal is detected at IF	T_{SU}	–	<1	–	ms	Depends on the used crystal		4.32
VCO MULTIPLEXER - Signal FSEL (PIN 9)								
f_{RF} range 434 MHz	V_{FSEL}	1.4	–	4[1)]	V	Or open		4.33
f_{RF} range 868 MHz	V_{FSEL}	0	–	0.2	V			4.34

Table 11 AC/DC Characteristics with T_{AMB}= -40°C ... + 85°C, V_{CC} = 4.5 ... 5.5 V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Output bias current FSEL	I_{FSEL}	-110	-200	-340	µA	FSEL tied to GND		4.35
PLL DIVIDER - Signal CSEL (PIN 15)								
f_{CRSTL} range 6.xxMHz	V_{CSEL}	1.4	–	4[1)]	V	Or open		4.36
f_{CRSTL} range 13.xxMHz	V_{CSEL}	0	–	0.2	V			4.37
Input bias current CSEL	I_{CSEL}	-3	-5	-7	µA	CSEL tied to GND		4.38

1) Maximum voltage in Power-On state is 4 V, but in PDWN-state the maximum voltage is 2.8 V.

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.2 Customer Test Circuit

The device performance parameters marked with ■ in **Table 9**, **Table 10**, and **Table 11** are not subject to production test. They were verified by design/characterization. The received signal is accessible on a 2-pole pin connector and can be used for simple remote-control applications. More information on the board is available on request.

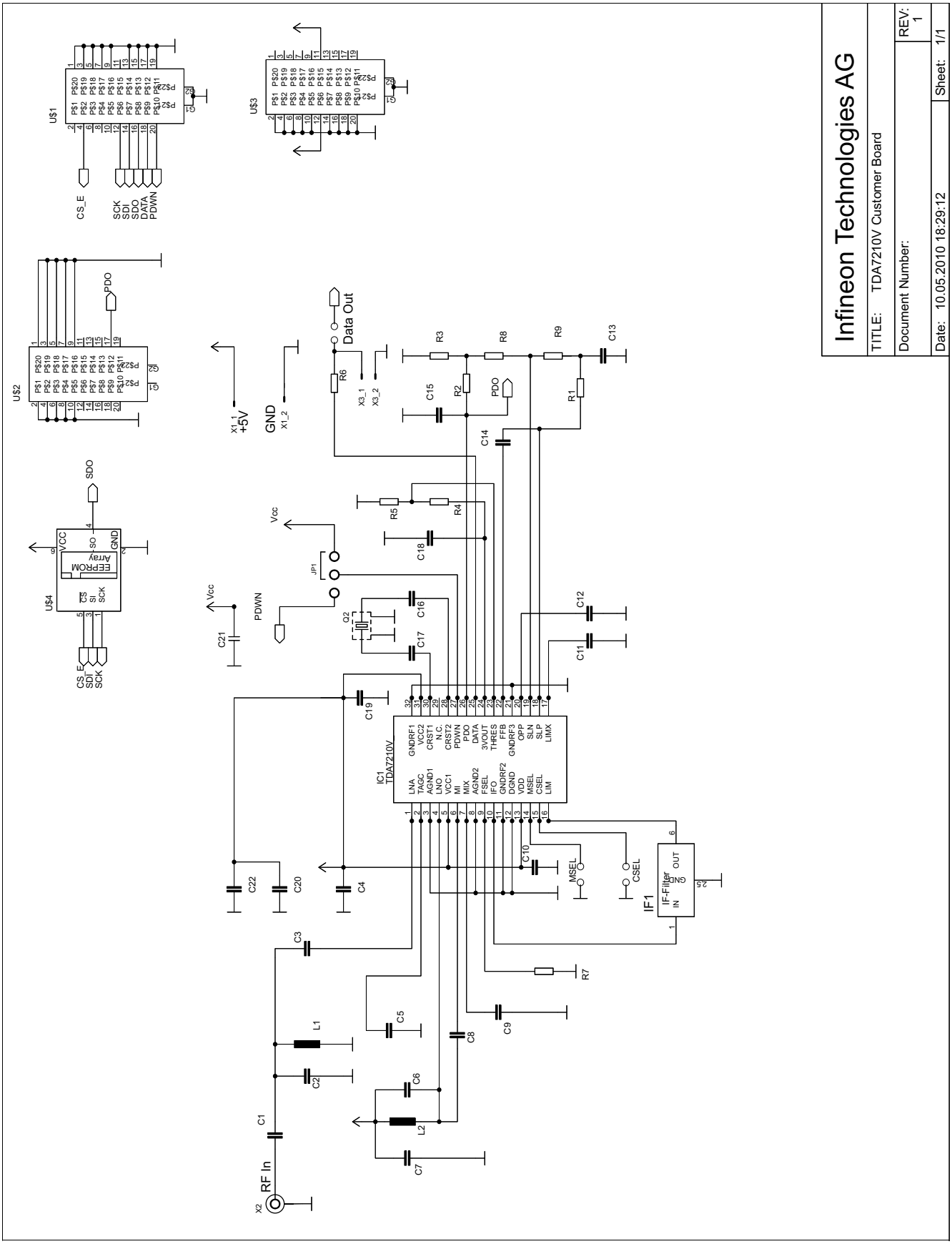


Figure 17 Schematic of the Customer Test Board TDA7210V

4.3 Customer Test Board Layout

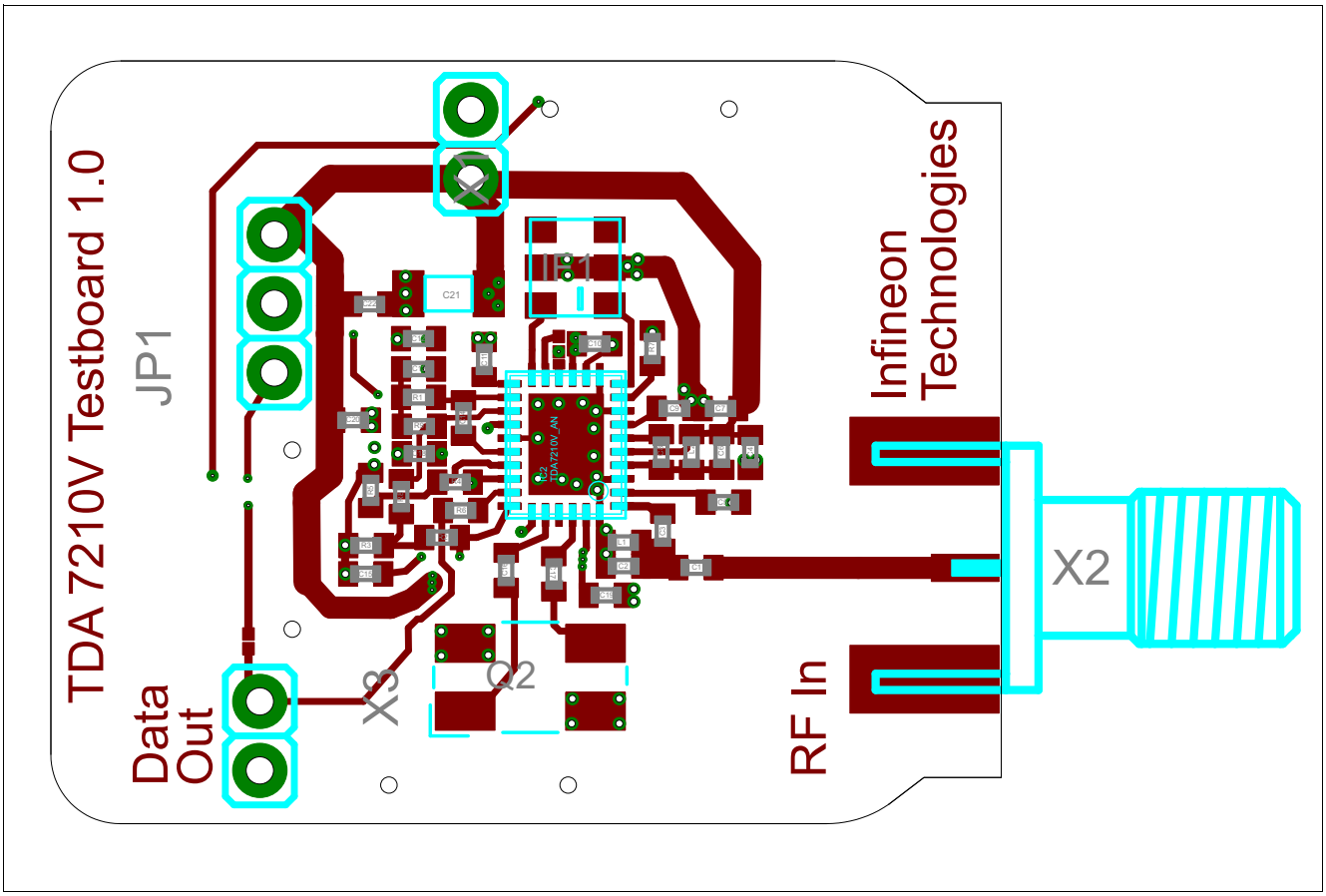


Figure 18 Top Layer of Customer Test Board TDA7210V

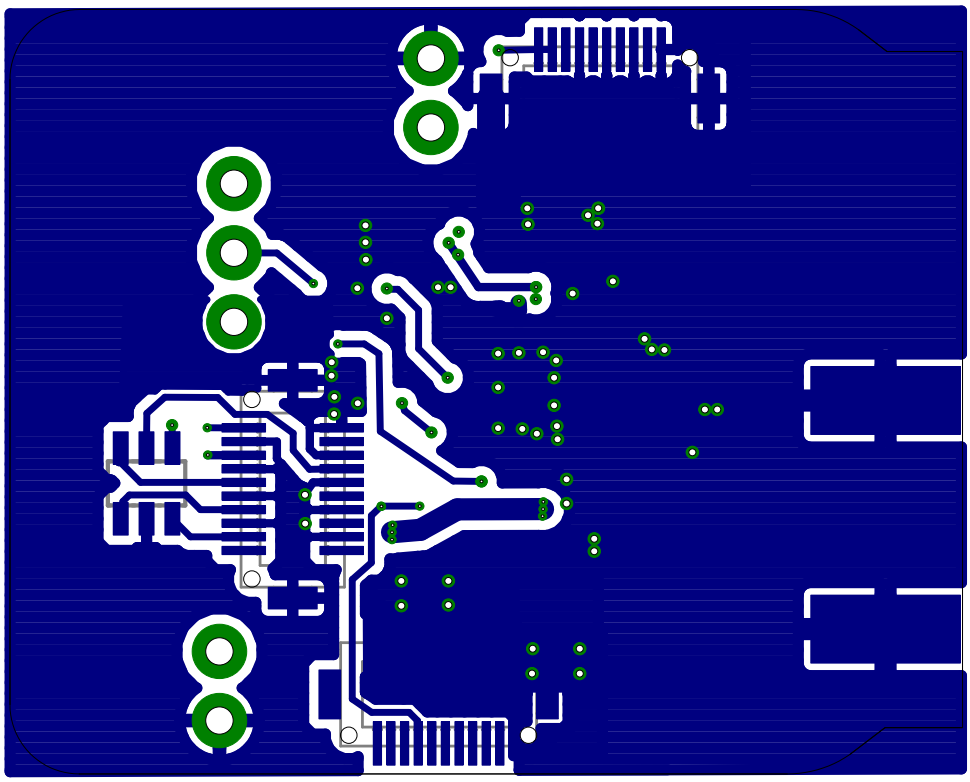


Figure 19 Bottom Layer of Customer Test Board TDA7210V

4.4 Bill of Materials

The following components are necessary for evaluation of the TDA7210V.

Table 12 Bill of Materials

Ref	Value	Specification
R1	100 kΩ	0402, ± 5%
R2	100 kΩ	0402, ± 5%
R3	820 kΩ	0402, ± 5%
R4	240 kΩ	0402, ± 5%
R5	360 kΩ	0402, ± 5%
R6	10 kΩ	0402, ± 5%
R7	434 MHz: - 868 MHz: 0 Ω	- 0402, ± 5%
R8	-	-
R9	0 Ω	0402, ± 5%
L1	434 MHz: 30 nH 868 MHz: 8.2 nH	Coilcraft SIMID 0402HP, ± 2% Coilcraft SIMID 0402HP, ± 2%
L2	434 MHz: 56 nH 868 MHz: 15 nH	Coilcraft SIMID 0402HP, ± 2% Coilcraft SIMID 0402HP, ± 2%
C1	434 MHz: 1.8 pF 868 MHz: 1.2 pF	0402, COG, ± 0.1 pF 0402, COG, ± 0.1 pF
C2	434 MHz: - 868 MHz: -	- 0402, COG, ± 0.1pF
C3	434 MHz: 18 pF 868 MHz: 10 pF	0402, COG, ± 0.1pF 0402, COG, ± 0.1pF
C4	100 pF	0402, COG, ± 5%
C5	47 nF	0402, COG, ± 5%
C6	434 MHz: - 868 MHz: -	- -
C7	100 pF	0402, X7R, ± 5%
C8	434 MHz: 100 pF 868 MHz: 270 pF	0402, COG, ± 1% 0402, COG, ± 1%
C9	100 pF	0402, COG, ± 5%
C10	10 nF	0402, X7R, ± 10%
C11	10 nF	0402, X7R, ± 10%
C12	220 pF	0402, COG, ± 5%
C13	47 nF	0402, X7R, ± 10%
C14	470 pF	0402, COG, ± 5%
C15	47 nF	0402, X7R, ± 5%
C16	8.2 pF	0402, COG, ± 0.1 pF
C17	22 pF	0402, COG, ± 1%
C18	22 nF	0402, X7R, ± 5%

Table 12 Bill of Materials (cont'd)

Ref	Value	Specification
C19	10 nF	0402, X7R, ± 5%
C20	47 nF	0402, X7R, ± 5%
C21	2.2 µF	0805, X7R, ± 10%
C22	47 nF	0402, X7R, ± 5%
Q1	(f_{RF} – 10.7 MHz)/32 or (f_{RF} – 10.7 MHz)/64	Tokoy Denpa TSS-6035B 434 MHz: 13.2343750 MHz, CL=12 pF, Spec.No. 120-16504 868 MHz: 13.4015625 MHz, CL=12 pF, Spec.No. 120-16505
Q2	IF-Filter 10,7MHz	Murata SFECF10M7FA00S0-R0
X1, X3	2-pole pin connector	2-pole pin connector, 2,54mm
X2	SMA-connector	RS: SMA Jack End Launch 1,07mm
JP1	3-pole pin connector	3-pole pin connector, 2,54mm
MSEL	solder bridge	closed solder bridge
CSEL	solder bridge	closed solder bridge
IC1	TDA7210V	Infineon

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