

OptiMOS® Power-Transistor

Features

- N-channel
- Enhancement mode
- Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- 175 °C operating temperature
- Avalanche rated
- dv/dt rated

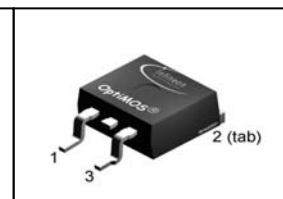
Product Summary

V_{DS}	30	V
$R_{DS(on),max}$	12.9	mΩ
I_D	42	A

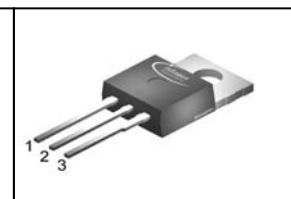
P-TO262-3-1



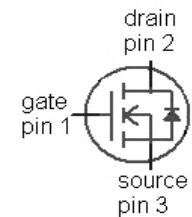
P-TO263-3-2



P-TO220-3-1



Type	Package	Ordering Code	Marking
SPP42N03S2L-13	P-TO220-3-1	Q67042-S4034	2N03L13
SPB42N03S2L-13	P-TO263-3-2	Q67042-S4035	2N03L13
SPI42N03S2L-13	P-TO262-3-1	Q67042-S4104	2N03L13



Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$	42	A
		$T_C=100\text{ °C}$	42	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}$	248	
Avalanche energy, single pulse	E_{AS}	$I_D=42\text{ A}$, $R_{GS}=25\text{ Ω}$	110	mJ
Repetitive avalanche energy	E_{AR}	limited by T_{jmax} ²⁾	8	mJ
Reverse diode dv/dt	dv/dt	$I_D=42\text{ A}$, $V_{DS}=24\text{ V}$, $di/dt=200\text{ A/μs}$, $T_{j,max}=175\text{ °C}$	6	kV/μs
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	83	W
Operating and storage temperature	T_J , T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	1.2	1.8	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=37\text{ }\mu\text{A}$	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance ⁴⁾	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=21\text{ A}$	-	14.9	19.9	m Ω
		$V_{GS}=4.5\text{ V}, I_D=21\text{ A},$ SMD version	-	14.5	19.6	
		$V_{GS}=10\text{ V}, I_D=21\text{ A}$	-	10.3	12.9	
		$V_{GS}=10\text{ V}, I_D=21\text{ A},$ SMD version	-	9.9	12.6	
Gate resistance	R_G		-	1	-	Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max},$ $I_D=42\text{ A}$	21	42	-	S

¹⁾ Current is limited by bondwire; with an $R_{thJC}=1.8\text{ K/W}$ the chip is able to carry 64 A at 25°C, for detailed information see app.-note ANPS071E at www.infineon.com/optimos.

²⁾ Defined by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

⁴⁾ Diagrams are related to straight lead versions.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	850	1130	pF
Output capacitance	C_{oss}		-	330	440	
Reverse transfer capacitance	C_{rss}		-	90	130	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=21\text{ A}, R_G=7.8\ \Omega$	-	6.5	9.8	ns
Rise time	t_r		-	12	18	
Turn-off delay time	$t_{d(off)}$		-	24	36	
Fall time	t_f		-	14.5	21.8	

Gate Charge Characteristics

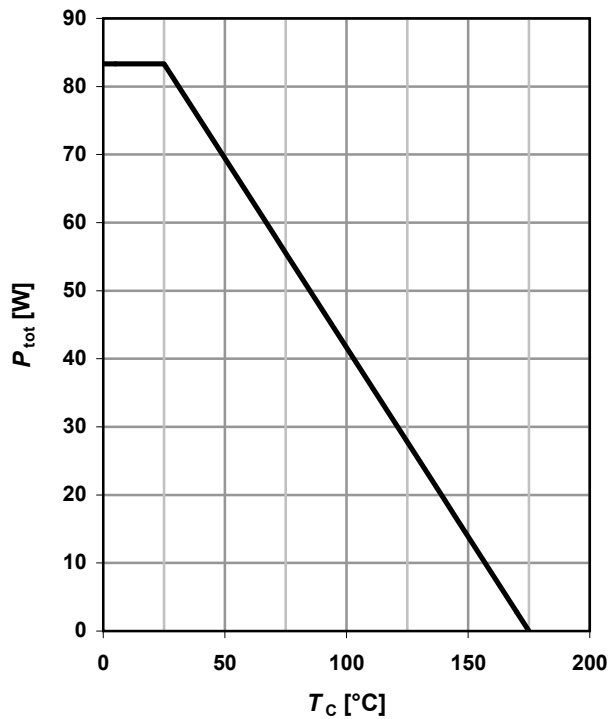
Gate to source charge	Q_{gs}	$V_{DD}=24\text{ V}, I_D=21\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	2.7	3.6	nC
Gate to drain charge	Q_{gd}		-	7.9	11.9	
Gate charge total	Q_g		-	22.9	30.5	
Gate plateau voltage	$V_{plateau}$		-	3.5	-	V

Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ °C}$	-	-	42	A
Diode pulse current	$I_{S,pulse}$		-	-	248	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=42\text{ A},$ $T_J=25\text{ °C}$	-	0.95	1.25	V
Reverse recovery time	t_{rr}	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	24	31	ns
Reverse recovery charge	Q_{rr}		-	18	23	

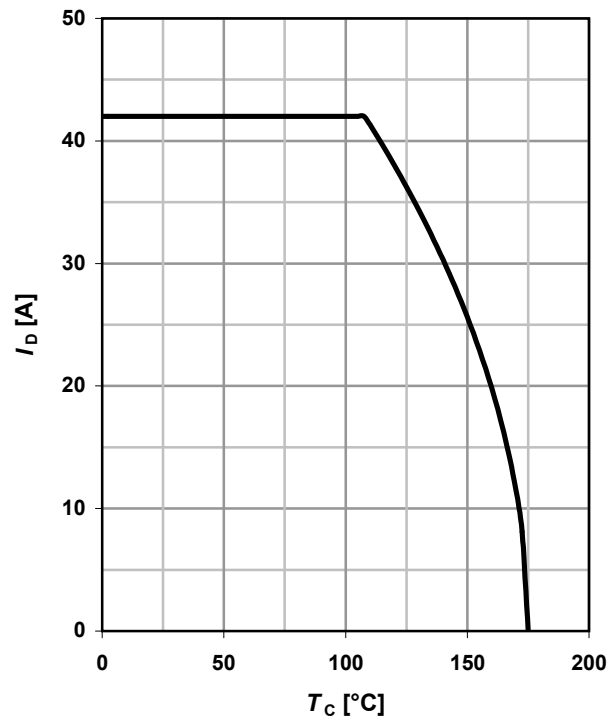
1 Power dissipation

$$P_{\text{tot}} = f(T_C)$$



2 Drain current

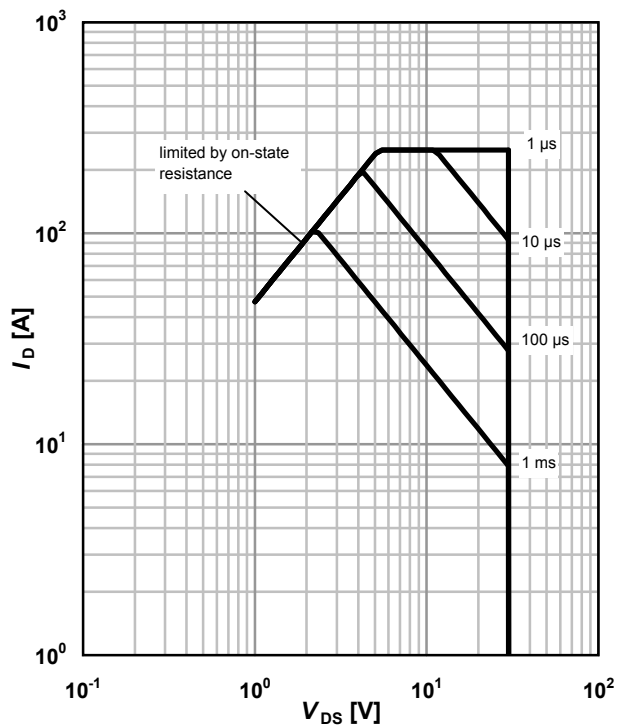
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

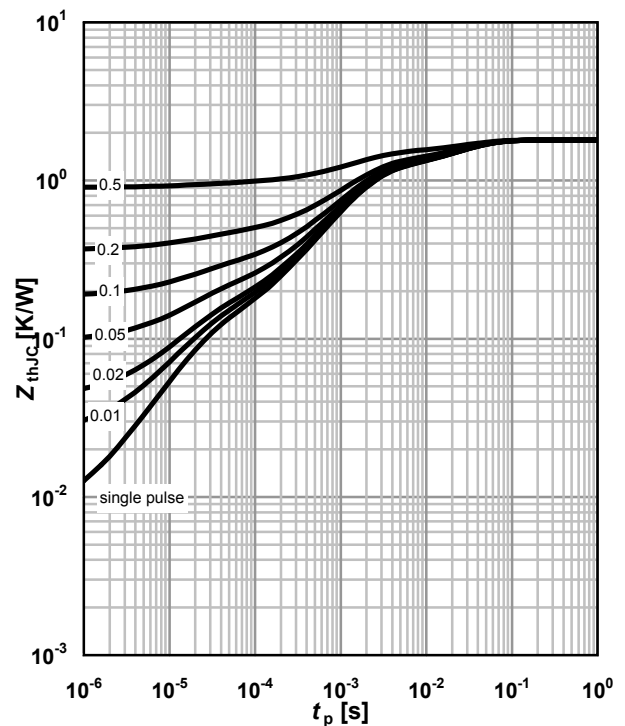
parameter: t_p



4 Max. transient thermal impedance

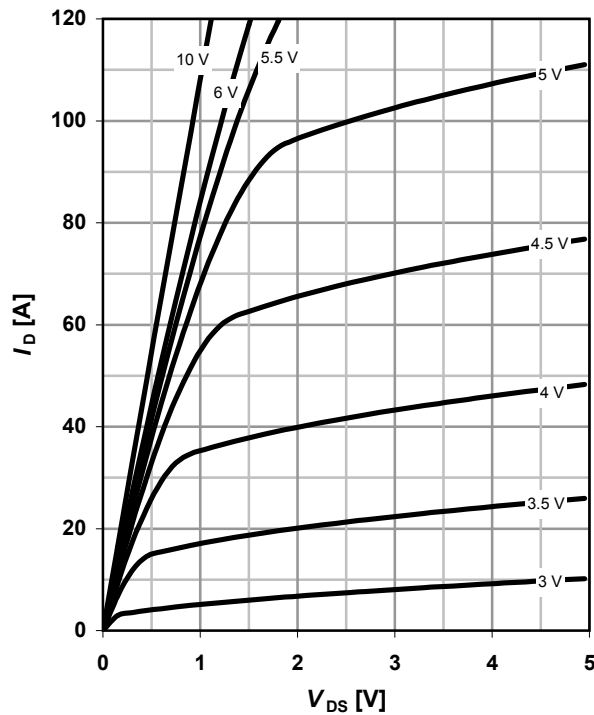
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p / T$



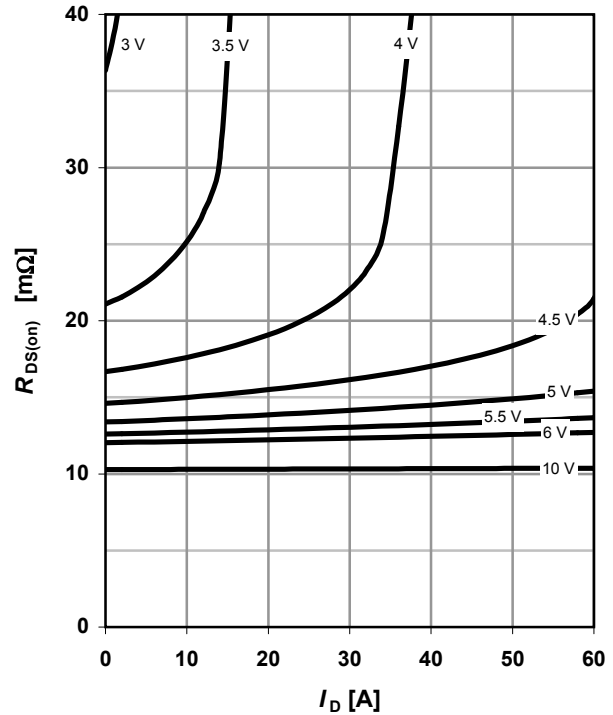
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


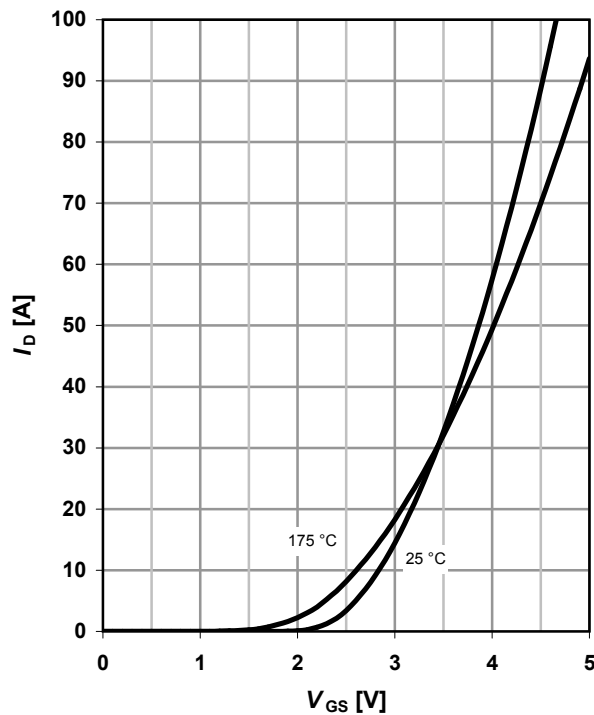
6 Typ. drain-source on resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

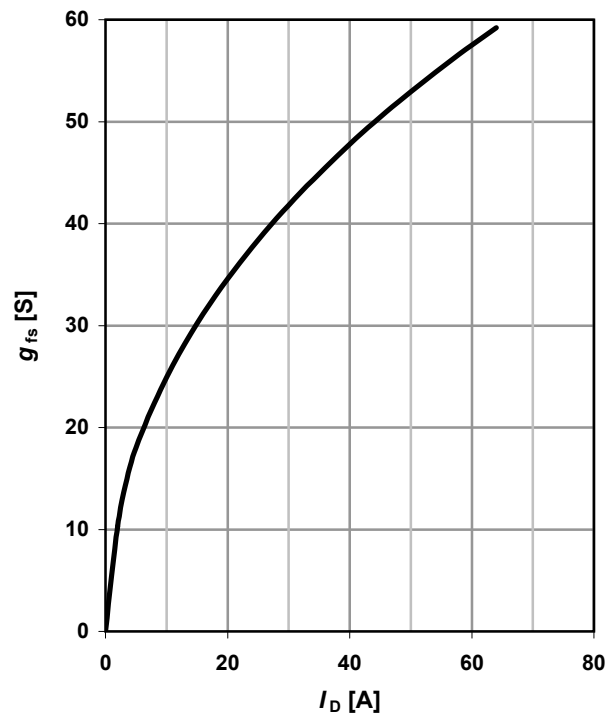
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

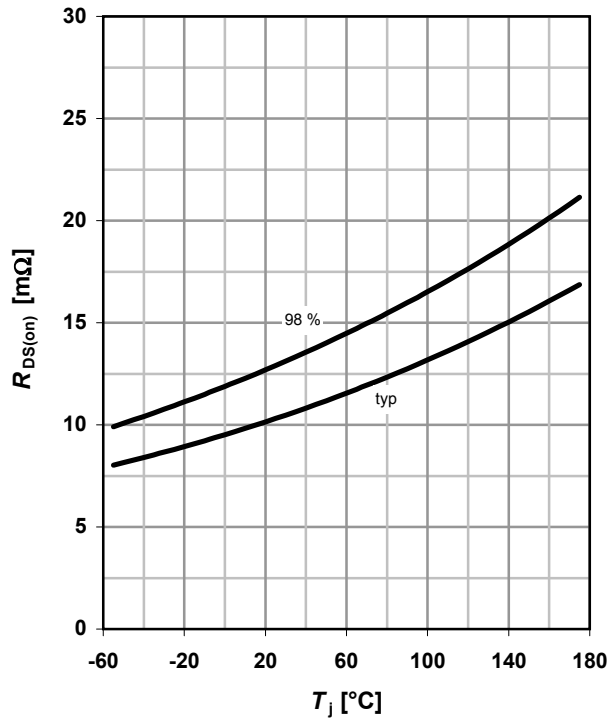
parameter: T_j


8 Typ. forward transconductance

 $g_{fs} = f(I_D); T_j = 25^\circ\text{C}$


9 Drain-source on-state resistance

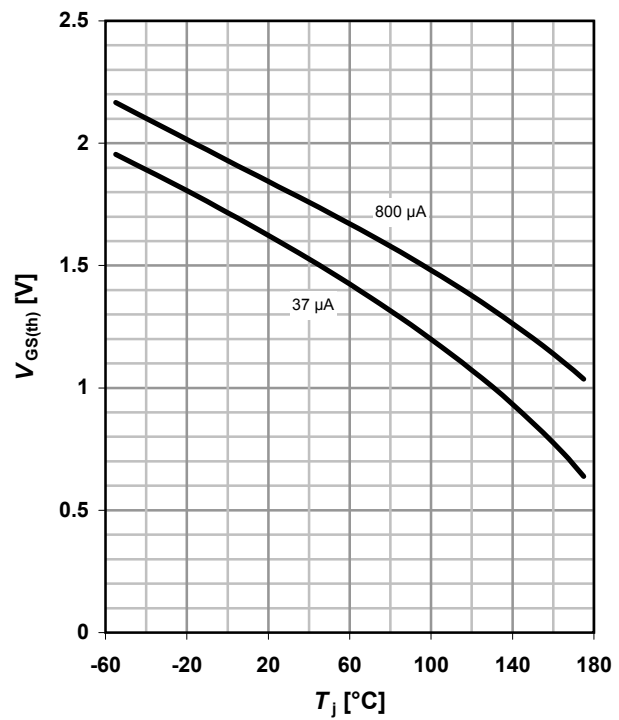
$$R_{DS(on)} = f(T_j); I_D = 21 \text{ A}; V_{GS} = 10 \text{ V}$$



10 Typ. gate threshold voltage

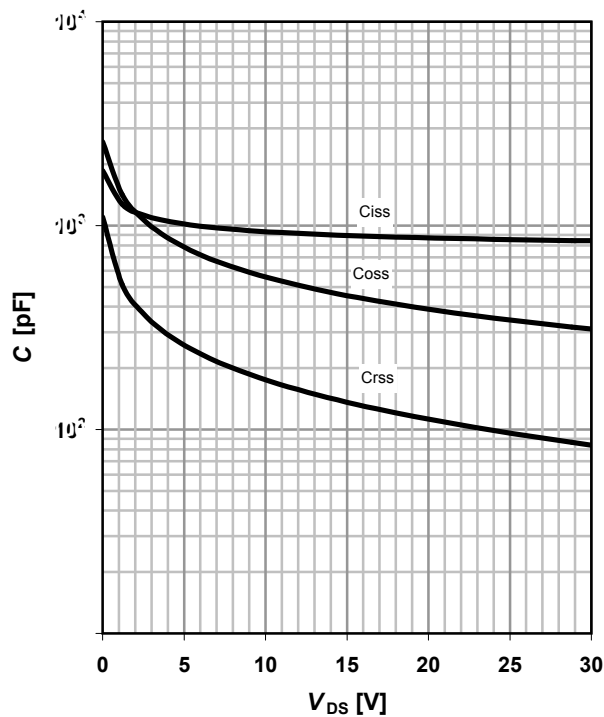
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



11 Typ. capacitances

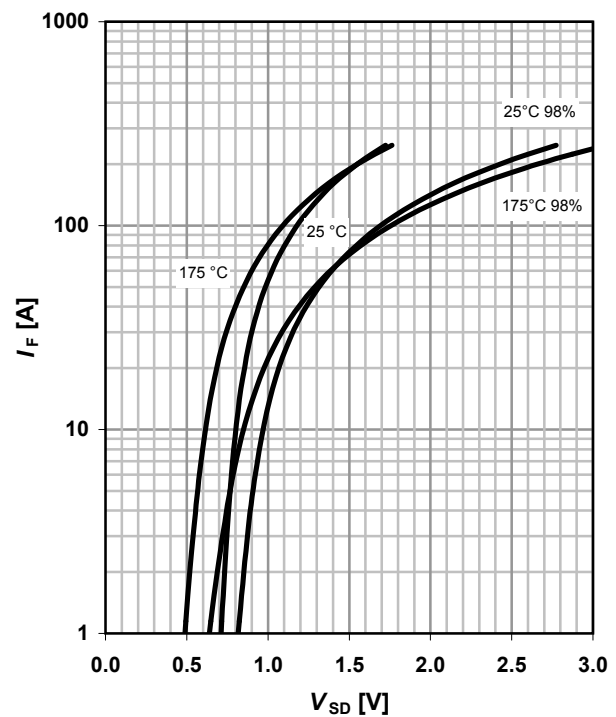
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

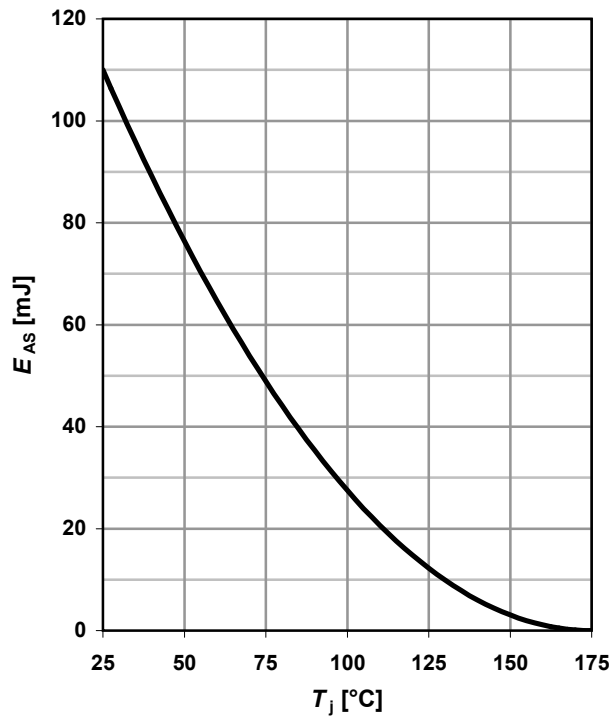
parameter: T_j



13 Avalanche characteristics

$$E_{AS}=f(T_j)$$

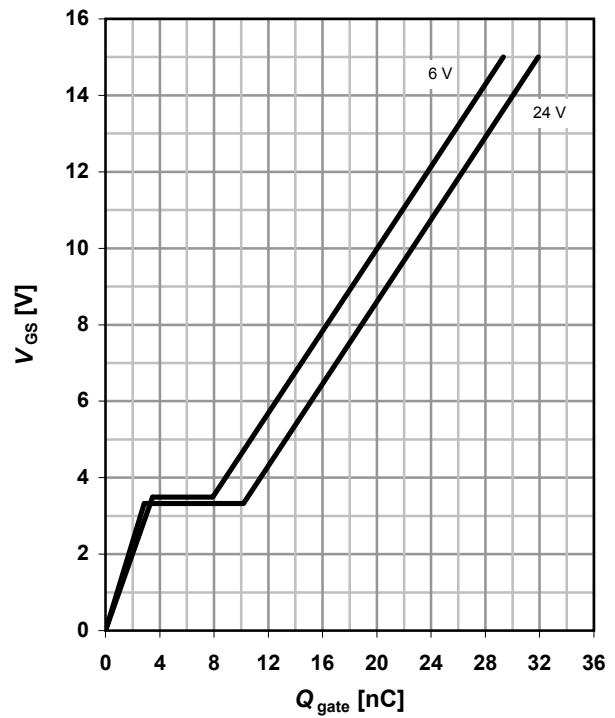
parameter: $I_D=42\text{A}$, $V_{DD}=25\text{V}$, $R_{GS}=25\Omega$



14 Typ. gate charge

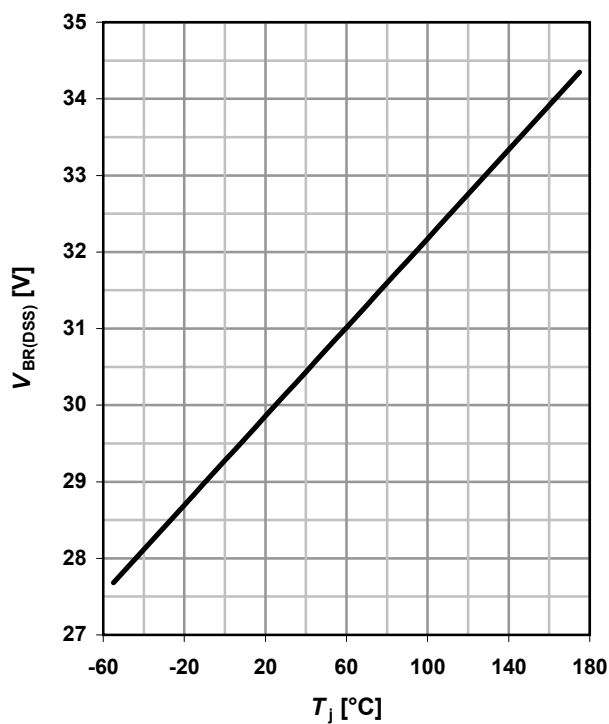
$$V_{GS}=f(Q_{\text{gate}}); I_D=21\text{ A pulsed}$$

parameter: V_{DD}

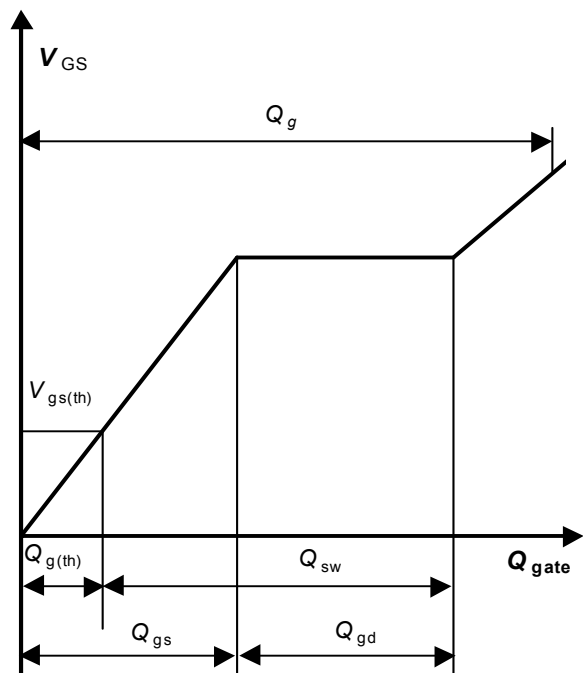


15 Drain-source breakdown voltage

$$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$$

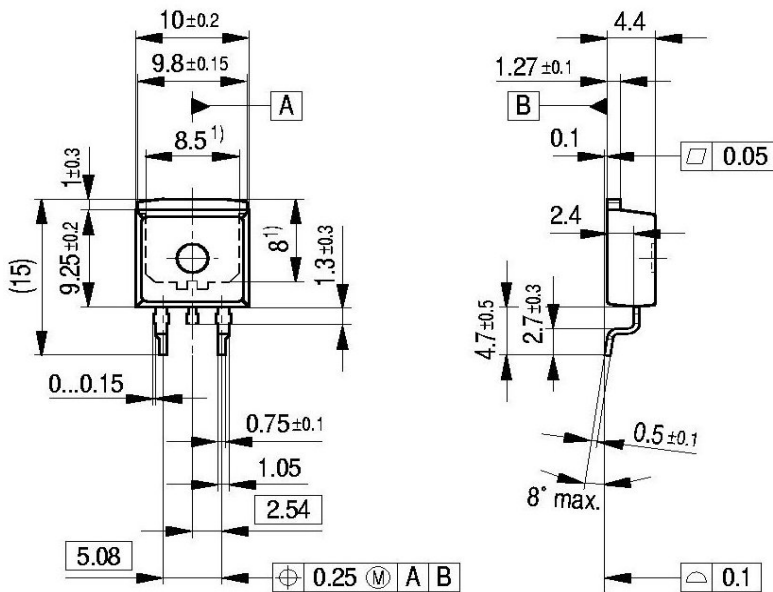


16 Gate charge waveforms



Package Outline

P-TO263-3-2: Outline

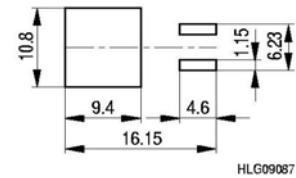


¹⁾ Typical

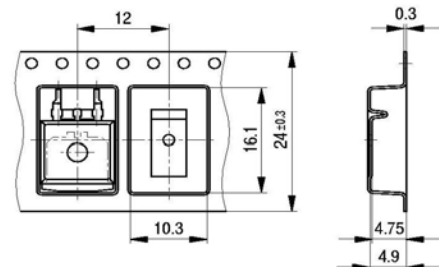
All metal surfaces tin plated, except area of cut.

GPT09085

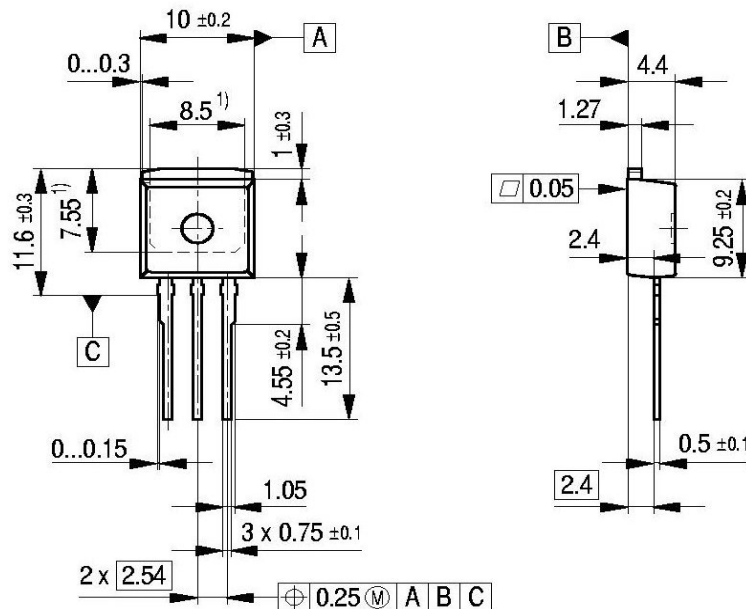
Footprint



Packaging



P-TO262-3-1: Outline



¹⁾ Typical

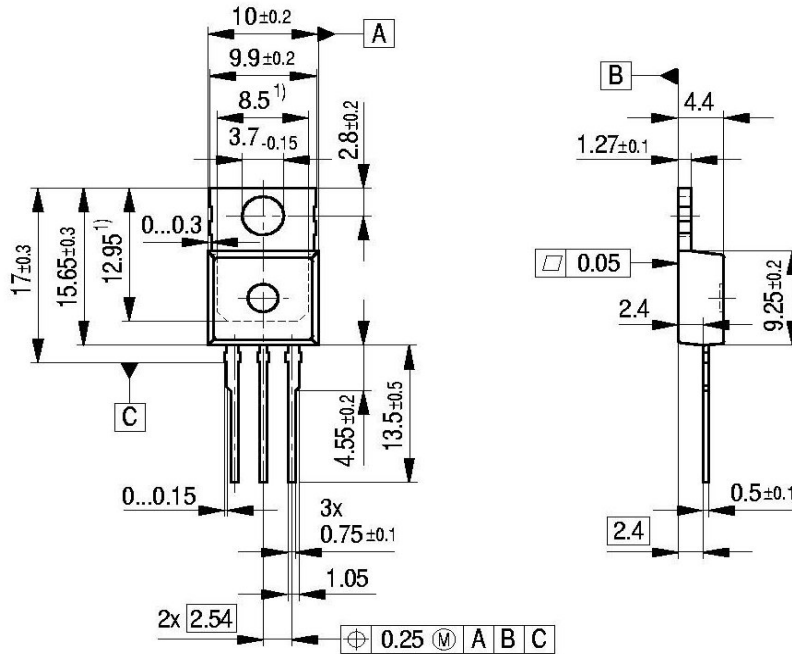
Metal surface min. X = 7.25, Y = 6.9

All metal surfaces tin plated, except area of cut.

Dimensions in mm

Package Outline

P-TO220-3-1: Outline

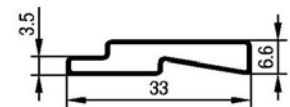


¹⁾ Typical

All metal surfaces tin plated, except area of cut.

Metal surface min. $x=7.25$, $y=12.3$

Packaging



Dimensions in mm

Published by
Infineon Technologies AG
Bereich Kommunikation
St.-Martin-Straße 53
D-81541 München
© Infineon Technologies AG 1999
All Rights Reserved.

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices, please contact your nearest Infineon Technologies office in Germany or our Infineon Technologies representatives worldwide (see address list).

Warnings

Due to technical requirements, components may contain dangerous substances.

For information on the types in question, please contact your nearest Infineon Technologies office.

Infineon Technologies' components may only be used in life-support devices or systems with the expressed written approval of Infineon Technologies if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Further information

Please note that the part number is BSPP42N03S2L-13, BSPB42N03S2L-13 and BSPI42N03S2L-13, for simplicity the device is referred to by the term SPP42N03S2L-13, SPB42N03S2L-13, SPI42N03S2L-13 throughout this documentation.