



BOURNS®

PROGRAMMABLE OVERVOLTAGE PROTECTOR QUAD FORWARD-CONDUCTING P-GATE THYRISTOR

TISP61089QB SLIC Overvoltage Protector

Quad Voltage-Programmable Protector

- Wide -20 V to -155 V Programming Range
- Low 5 mA max. Gate Triggering Current
- High 150 mA min. Holding Current
- Rated for ITU-T and YD/T-950 10/700 impulses
- Rated for Telcordia Intra-building impulses

10/700 Protection Voltage Specified

| Element | Protection Level 40 A, 5/310 |
|-----------------------------|---------------------------------|
| Diode | +12 |
| Crowbar $V_{GG} = -48$ V | -64 |

Description

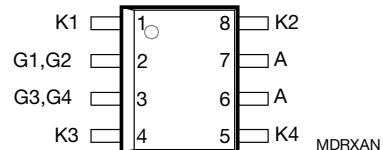
Bourns® TISP61089QB is a quad forward-conducting buffered p-gate overvoltage protector. It is designed to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. The TISP61089QB limits voltages that exceed the SLIC supply rail voltage. The TISP61089QB parameters are specified to allow equipment compliance with Telcordia GR-1089-CORE Intra-building, ITU-T K.20, K.21 and K.45 and YD/T-950.

The SLIC line driver section is typically powered from 0 V (ground) and a negative voltage in the region of -20 V to -155 V. The protector gate is connected to this negative supply. This references the protection (clipping) voltage to the negative supply voltage. As the protection voltage will then track the negative supply voltage the overvoltage stress on the SLIC is minimized.

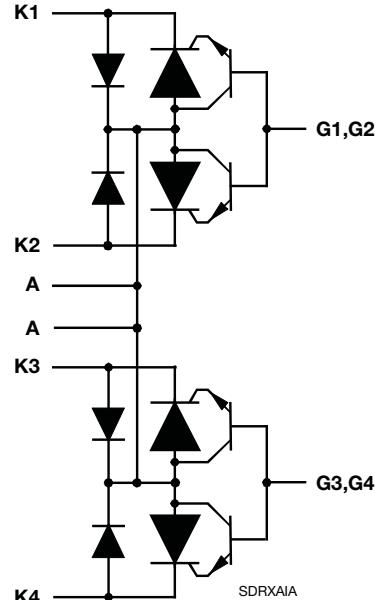
Positive overvoltages are clipped to ground by diode forward conduction. Negative overvoltages are initially clipped close to the SLIC negative supply rail value. If sufficient current is available from the overvoltage, then the protector will crowbar into a low voltage on-state condition. As the overvoltage subsides, the high holding current of the crowbar helps prevent d.c. latchup.

These monolithic protection devices are fabricated in ion-implanted planar vertical power structures for high reliability and are virtually transparent in normal operation. The TISP61089QB buffered gate design reduces the loading on the SLIC supply during overvoltages caused by power cross and induction. The TISP61089QB is available in an 8-pin plastic small-outline surface mount package.

D Package (Top View)



Device Symbol



How to Order

| Device | Package | Carrier | Order As | Marking Code | Standard Quantity |
|-------------|----------------------------|----------------------|-----------------|--------------|-------------------|
| TISP61089QB | 8 Pin Small Outline (D008) | Embossed Tape Reeled | TISP61089QBDR-S | 1089QB | 2500 |

*RoHS Directive 2002/95/EC Jan. 27, 2003 including annex and RoHS Recast 2011/65/EU June 8, 2011.

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Specifications are subject to change without notice.

Customers should verify actual device performance in their specific applications.

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Absolute Maximum Ratings, $T_J = 25^\circ\text{C}$ (Unless Otherwise Noted)

| Rating | Symbol | Value | Unit |
|--|-------------------|-----------------------|------------------|
| Repetitive peak off-state voltage, $I_G = 0$ | V_{DRM} | -170 | V |
| Repetitive peak gate-cathode voltage, $V_{KA} = 0$ | V_{GKRM} | -167 | V |
| Non-repetitive peak on-state pulse current (see Notes 1 and 2) 10/1000 μs (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4) 5/310 μs (ITU-T K.20/21/45, YD/T-950, open circuit voltage waveshape 10/700) 2/40 μs (IEC61000-4-5, 1.2/50 μs open circuit voltage, 2 ohm + 10 ohm, see Note 4) 2/10 μs (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4) | I_{TSP} | 30 40 85 120 | A |
| Non-repetitive peak on-state current, 60 Hz (see Notes 1, 2 and 3) 900 s | I_{TSM} | 0.5 | A |
| Non-repetitive peak gate current, 2/10 μs pulse, cathodes commoned (see Notes 1 and 2) | I_{GSM} | 40 | A |
| Junction temperature | T_J | -40 to +150 | $^\circ\text{C}$ |
| Storage temperature range | T_{stg} | -40 to +150 | $^\circ\text{C}$ |

NOTES: 1. Initially the protector must be in thermal equilibrium with $T_J = 25^\circ\text{C}$. The surge may be repeated after the device returns to its initial conditions.
 2. These non-repetitive rated currents are peak values for either polarity. The rated current values may be applied to any cathode-anode terminal pair. Additionally, all cathode-anode terminal pairs may have their rated current values applied simultaneously (in this case the anode terminal current will be four times the rated current value of an individual terminal pair).
 3. EIA/JESD51-2 environment and EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.
 4. Combination wave generator as specified in ITU-T K.20, K.21, K.44.

Recommended Operating Conditions

| | Min | Typ | Max | Unit |
|---------------------------------|-----|-----|-----|------|
| C_G Gate decoupling capacitor | | 100 | | nF |

Electrical Characteristics, $T_J = 25^\circ\text{C}$ (Unless Otherwise Noted)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|-----------------------|-----|-----|---------------|
| I_D Off-state current | $V_D = V_{\text{DRM}}, V_{\text{GK}} = 0$ | | | -5 | μA |
| $V_{(\text{BO})}$ Breakover voltage | 10/700 μs , $I_T = -40 \text{ A}$, $R_S = 55 \Omega$, $V_{\text{GG}} = -48 \text{ V}$, $C_G = 100 \text{ nF}$ | | | -64 | V |
| V_F Forward voltage | $I_F = 5 \text{ A}$, $t_w = 200 \mu\text{s}$ | | | 3 | V |
| V_{FRM} Peak forward recovery voltage | 10/700 μs , $I_F = 40 \text{ A}$, $R_S = 55 \Omega$, $V_{\text{GG}} = -48 \text{ V}$, $C_G = 100 \text{ nF}$ | | 12 | | V |
| I_H Holding current | $I_T = -1 \text{ A}$, $di/dt = 1 \text{ A/ms}$, $V_{\text{GG}} = -100 \text{ V}$ | -150 | | | mA |
| I_{GAS} Gate reverse current | $V_{\text{GG}} = V_{\text{GK}} = V_{\text{GKRM}}$, $V_{KA} = 0$ | | | -5 | μA |
| I_{GT} Gate trigger current | $I_T = 3 \text{ A}$, $t_{p(g)} \geq 20 \mu\text{s}$, $V_{\text{GG}} = -100 \text{ V}$ | | | 5 | mA |
| V_{GT} Gate trigger voltage | $I_T = 3 \text{ A}$, $t_{p(g)} \geq 20 \mu\text{s}$, $V_{\text{GG}} = -100 \text{ V}$ | | | 2.5 | V |
| C_{AK} Anode-cathode off-state capacitance | $f = 1 \text{ MHz}$, $V_d = 1 \text{ V}$ $I_G = 0$, (see Note 5) | $V_D = -3 \text{ V}$ | | 100 | pF |
| | | $V_D = -48 \text{ V}$ | | 50 | |

NOTE: 5. These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

Thermal Characteristics

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|-----------------|---|-----|-----|-----|------|
| $R_{\theta JA}$ | $P_{tot} = 0.8 \text{ W}, T_A = 25 \text{ }^{\circ}\text{C}$ 5 cm ² , FR4 PCB | | | 160 | °C/W |

Parameter Measurement Information

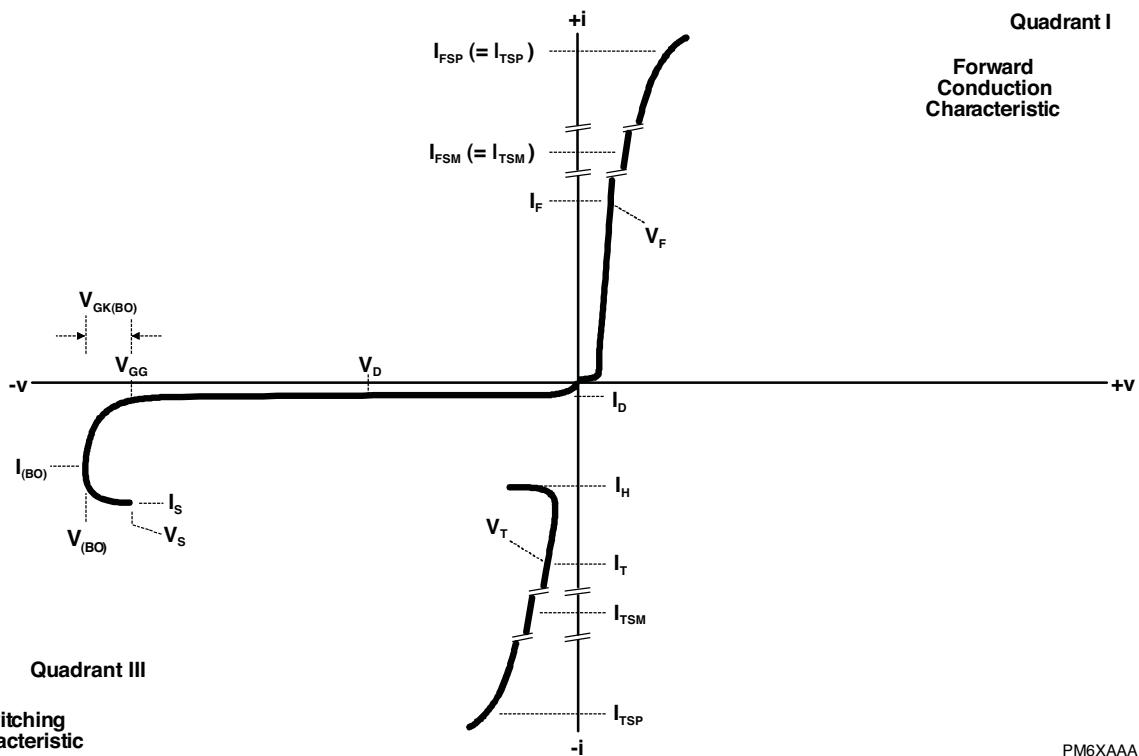


Figure 1. Voltage-Current Characteristic

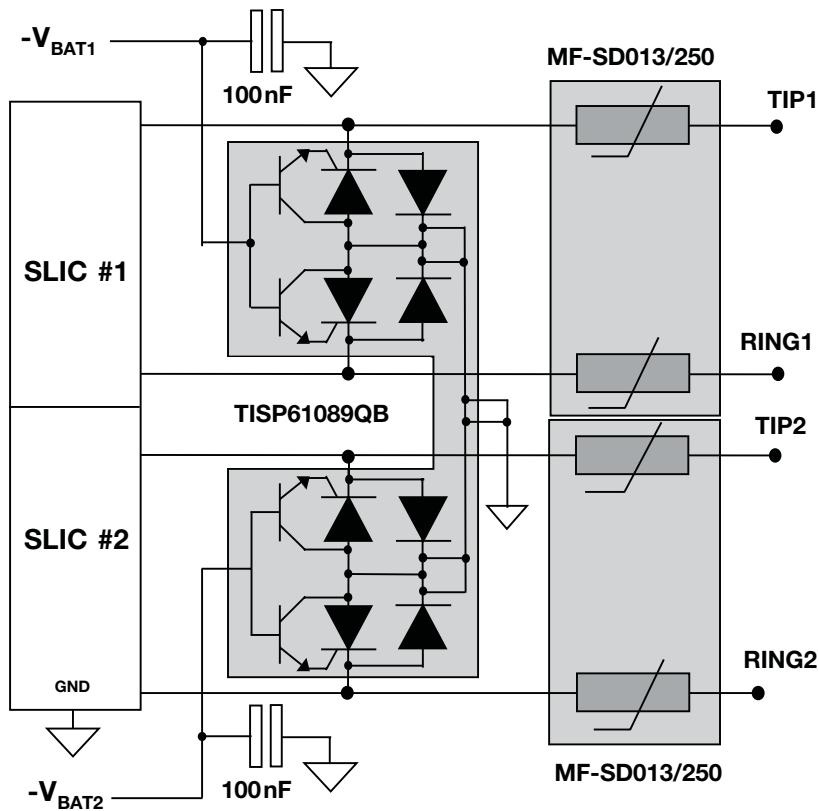
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Applications Information

Typical Applications Circuit

Figure 2 shows a typical TISP61089QB SLIC card protection circuit. The incoming line conductors, RING1/RING2 and TIP1/TIP2, connect to the relay matrix via the series overcurrent protection. Positive temperature coefficient (PTC) thermistors can be used for overcurrent protection. The resistance of the PTC thermistor will reduce the prospective current from the surge generator for the TISP61089QB.



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