

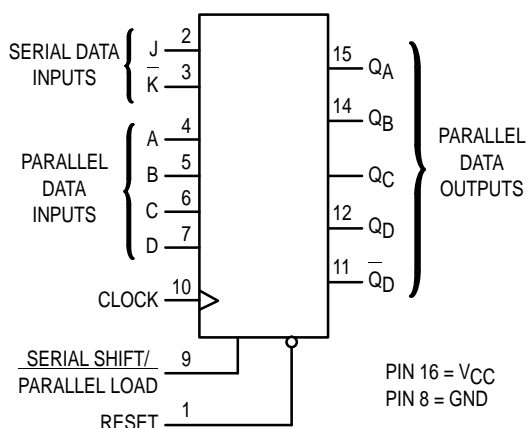
## 4-Bit Universal Shift Register High-Performance Silicon-Gate CMOS

The MC74HC195 is identical in pinout to the LS195. The device inputs are compatible with standard CMOS outputs, with pull up resistors, they are compatible with LSTTL outputs.

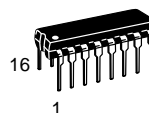
This static shift register features parallel load, serial load (shift right), hold, and reset modes of operation. These modes are tabulated in the Function Table, and further explanation can be found in the Pin Description section.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 150 FETs or 37.5 Equivalent Gates

**LOGIC DIAGRAM**



## MC74HC195



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08

### ORDERING INFORMATION

MC74HCXXXN Plastic

### PIN ASSIGNMENT

RESET	1	16	V <sub>CC</sub>
J	2	15	Q <sub>A</sub>
$\bar{K}$	3	14	Q <sub>B</sub>
A	4	13	Q <sub>C</sub>
B	5	12	Q <sub>D</sub>
C	6	11	$\bar{Q}_D$
D	7	10	CLOCK
GND	8	9	SERIAL SHIFT/ PARALLEL LOAD

**FUNCTION TABLE**

Inputs									Outputs					Operating Mode	
Reset	Shift/ Load	Clock	Serial		Parallel				Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	$\bar{Q}_D$		
L	X	X	X	X	X	X	X	X	L	L	L	L	H	Reset	
H	L	$\nearrow$	X	X	a	b	c	d	a	b	c	d	d	Parallel Load	
H	H	L	X	X	X	X	X	X	No Change					Hold	
H	H	$\nearrow$	L	H	X	X	X	X	Q <sub>A0</sub>	Q <sub>A0</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	$\bar{Q}_{Cn}$	Retain First Stage	Serial Shift
H	H	$\nearrow$	L	L	X	X	X	X	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	$\bar{Q}_{Cn}$	Reset First Stage	
H	H	$\nearrow$	H	H	X	X	X	X	$\bar{H}$	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	$\bar{Q}_{Cn}$	Set First Stage	
H	H	$\nearrow$	H	L	X	X	X	X	Q <sub>An</sub>	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	$\bar{Q}_{Cn}$	Toggle First Stage	

H = high level (steady state)

L = low level (steady state)

X = don't care

$\nearrow$  = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs

A, B, C, or D, respectively.

Q<sub>A0</sub> = the level of Q<sub>A</sub> before the indicated steady-state input conditions were established.

Q<sub>An</sub>, Q<sub>Bn</sub>, Q<sub>Cn</sub> = the level of Q<sub>A</sub>, Q<sub>B</sub>, or Q<sub>C</sub>, respectively, before the most recent  $\nearrow$  transition of the clock.



## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	− 1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	− 0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	± 20	mA
$I_{out}$	DC Output Current, per Pin	± 25	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	± 50	mA
$P_D$	Power Dissipation in Still Air Plastic DIP†	750	mW
$T_{stg}$	Storage Temperature	− 65 to + 150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\* Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: − 10 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	− 55	+ 125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ 0 1000 $V_{CC} = 4.5 \text{ V}$ 0 500 $V_{CC} = 6.0 \text{ V}$ 0 400		ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				− 55 to 25°C	≤ 85°C	≤ 125°C	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock to any Q or Q <sub>D</sub> (Figures 1 and 5)	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Reset to any Q or Q <sub>D</sub> (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

## NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		95	

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**TIMING REQUIREMENTS** (Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
$t_{su}$	Minimum Setup Time, A, B, C, D, J, or K to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
$t_{su}$	Minimum Setup Time, Serial Shift/Parallel Load to Clock (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
$t_h$	Minimum Hold Time, Clock to A, B, C, D, J, or K (Figure 3)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
$t_h$	Minimum Hold Time, Clock to Serial Shift/Parallel Load (Figure 4)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
$t_w$	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
$t_w$	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
$t_r$ , $t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

## PIN DESCRIPTION

## DATA INPUTS

**A, B, C, D (Pins 4, 5, 6, 7)**

Parallel data inputs.

## OUTPUTS

**Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, Q<sub>D</sub>,  $\overline{Q}_D$  (Pins 15, 14, 13, 12, 11)**

Parallel data outputs.

## CONTROL INPUTS

**Clock (Pin 10)**

Clock input. The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

**Serial Shift/Parallel Load (Pin 9)**

Shift or load control. A low level applied to this pin allows data to be loaded from the parallel inputs. Data is loaded with the positive transition of the Clock input. A high level allows data to be shifted in the manner dictated by the J and K control inputs.

**Reset (Pin 1)**

A low level applied to this pin resets all stages and forces all outputs low.

**J,  $\overline{K}$  (Pins 2, 3)**

Shift Control. With Serial Shift/Parallel Load high, J and  $\overline{K}$  control the mode of operation, as illustrated in the Function Table.

**J = L,  $\overline{K}$  = H**

With a positive transition of the Clock input, each bit is shifted to the right (in the direction Q<sub>A</sub> toward Q<sub>D</sub>) one stage and stage A maintains its previous state.

**J = H,  $\overline{K}$  = L**

With a positive transition of the Clock input, each bit is shifted right (in the direction of Q<sub>A</sub> toward Q<sub>D</sub>) one stage and the Q<sub>A</sub> output is inverted.

**J =  $\overline{K}$  = L**

With a positive transition of the Clock input, each bit is shifted right (in the direction Q<sub>A</sub> toward Q<sub>D</sub>) one stage and a low is loaded into stage A.

**J =  $\overline{K}$  = H**

With a positive transition of the Clock input, each bit is shifted right (in the direction Q<sub>A</sub> toward Q<sub>D</sub>) one stage and a high is loaded into stage A.

## SWITCHING WAVEFORMS

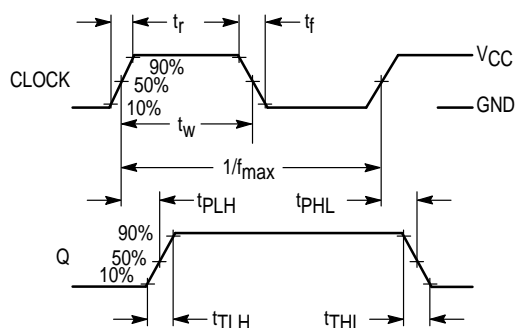


Figure 1.

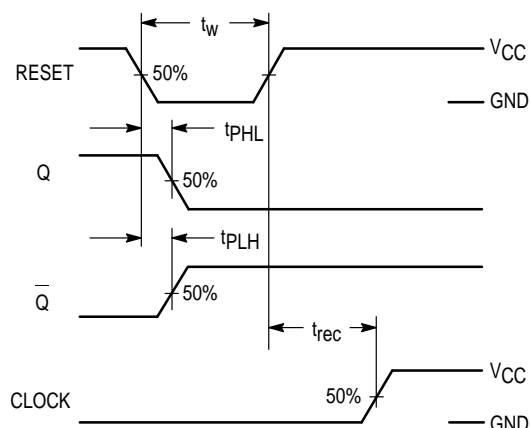


Figure 2.

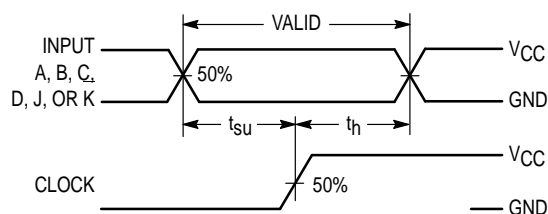


Figure 3.

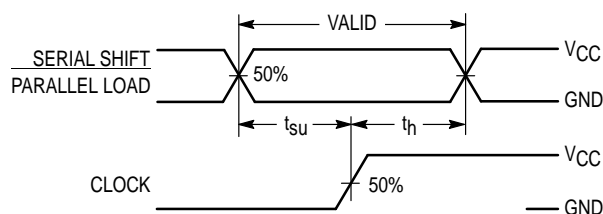
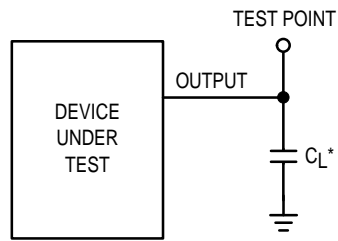
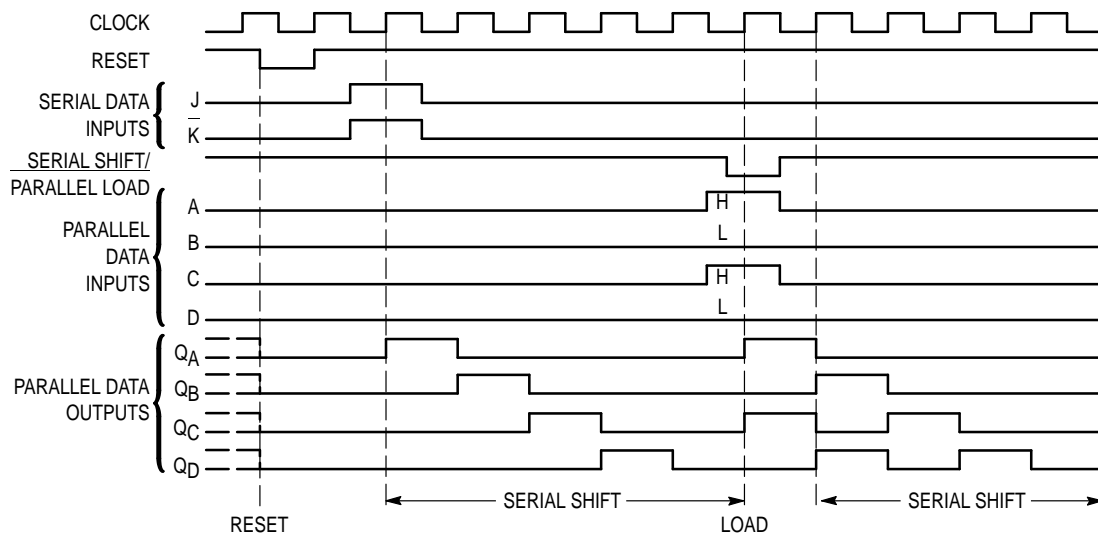


Figure 4.

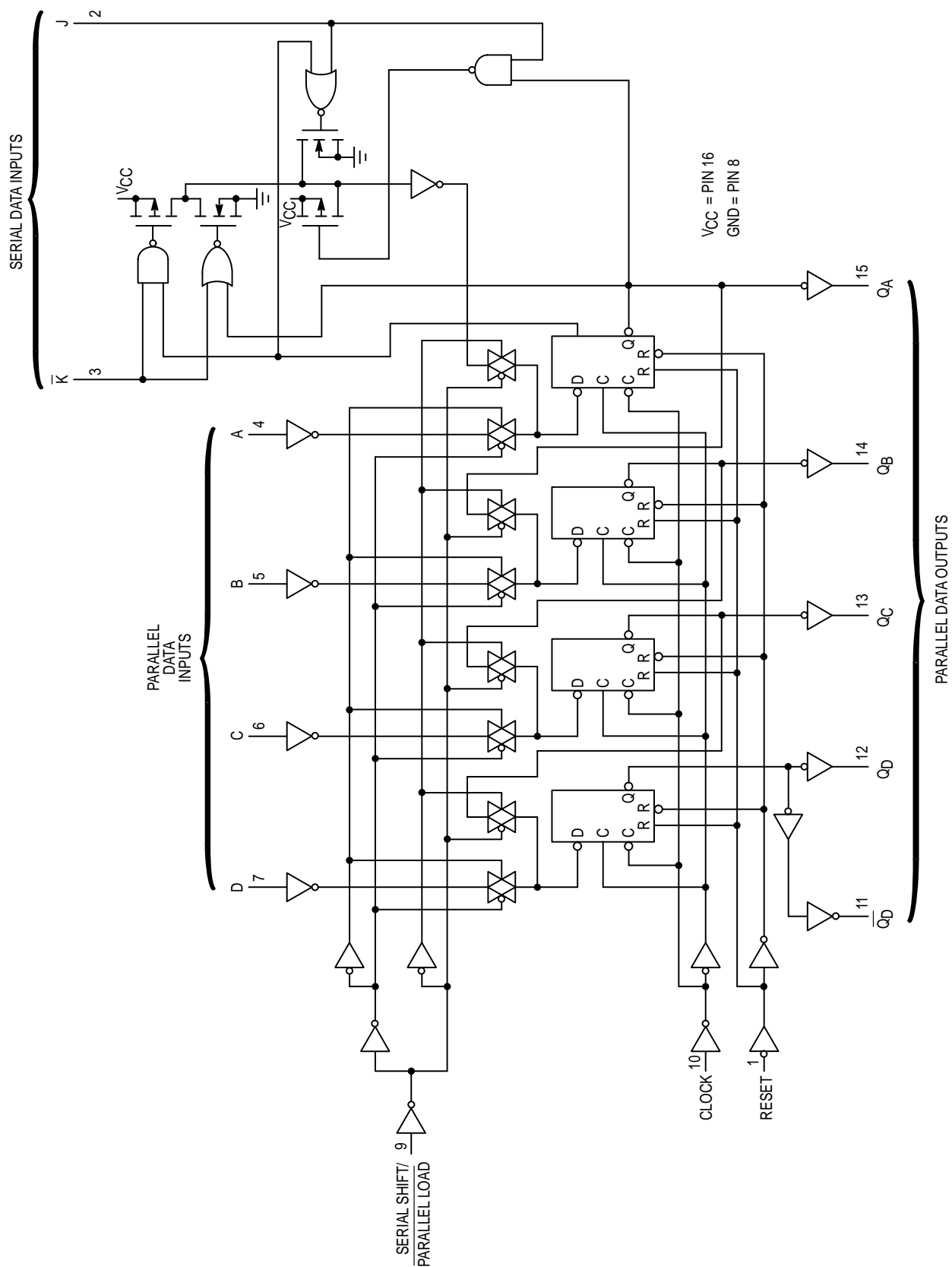
**TEST CIRCUIT**

\* Includes all probe and jig capacitance

**Figure 5.**

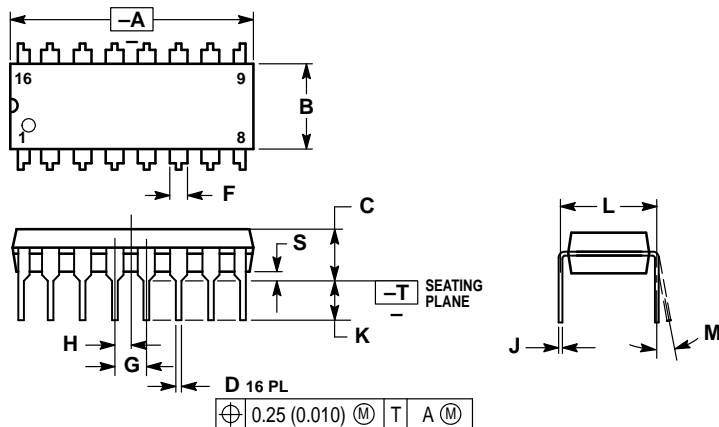
**TIMING DIAGRAM**

## EXPANDED LOGIC DIAGRAM



## OUTLINE DIMENSIONS


**N SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 648-08**  
**ISSUE R**



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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