

SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

- Internal Look-Ahead Circuitry for Fast Counting
- Carry Output for N-Bit Cascading
- Fully Synchronous Operation for Counting

description

This synchronous, presettable, 4-bit binary counter has internal carry look-ahead circuitry for use in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that normally are associated with asynchronous (ripple-clock) counters. However, counting spikes can occur on the ripple-carry (RCO) output. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of CLK.

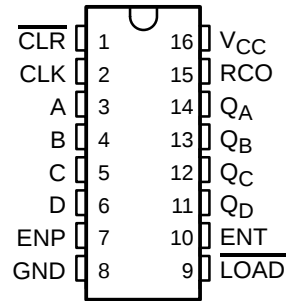
This counter is fully programmable. That is, it can be preset to any number between 0 and 15. Because presetting is synchronous, a low logic level at the load ($\overline{\text{LOAD}}$) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of ENP and ENT.

The clear function is synchronous, and a low logic level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs to low after the next low-to-high transition of the clock, regardless of the levels of ENP and ENT. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications, without additional gating. This function is implemented by the ENP and ENT inputs and an RCO output. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled, produces a high-logic-level pulse while the count is 15 (HHHH). The high-logic-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

The SN74F163A features a fully independent clock circuit. Changes at ENP, ENT, or $\overline{\text{LOAD}}$ that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the setup and hold times.

D, DB, OR N PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74F163AN	SN74F163AN
	SOIC – D	Tube	SN74F163AD	F163A
		Tape and reel	SN74F163ADR	
	SSOP – DB	Tape and reel	SN74F163ADBR	F163A

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

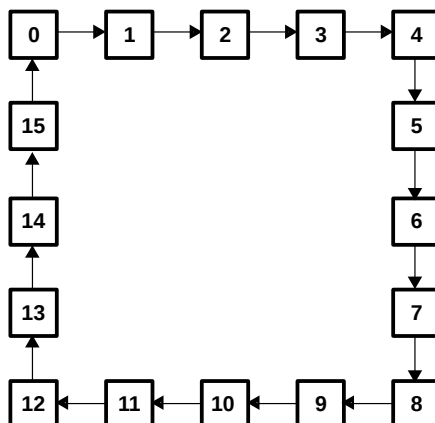
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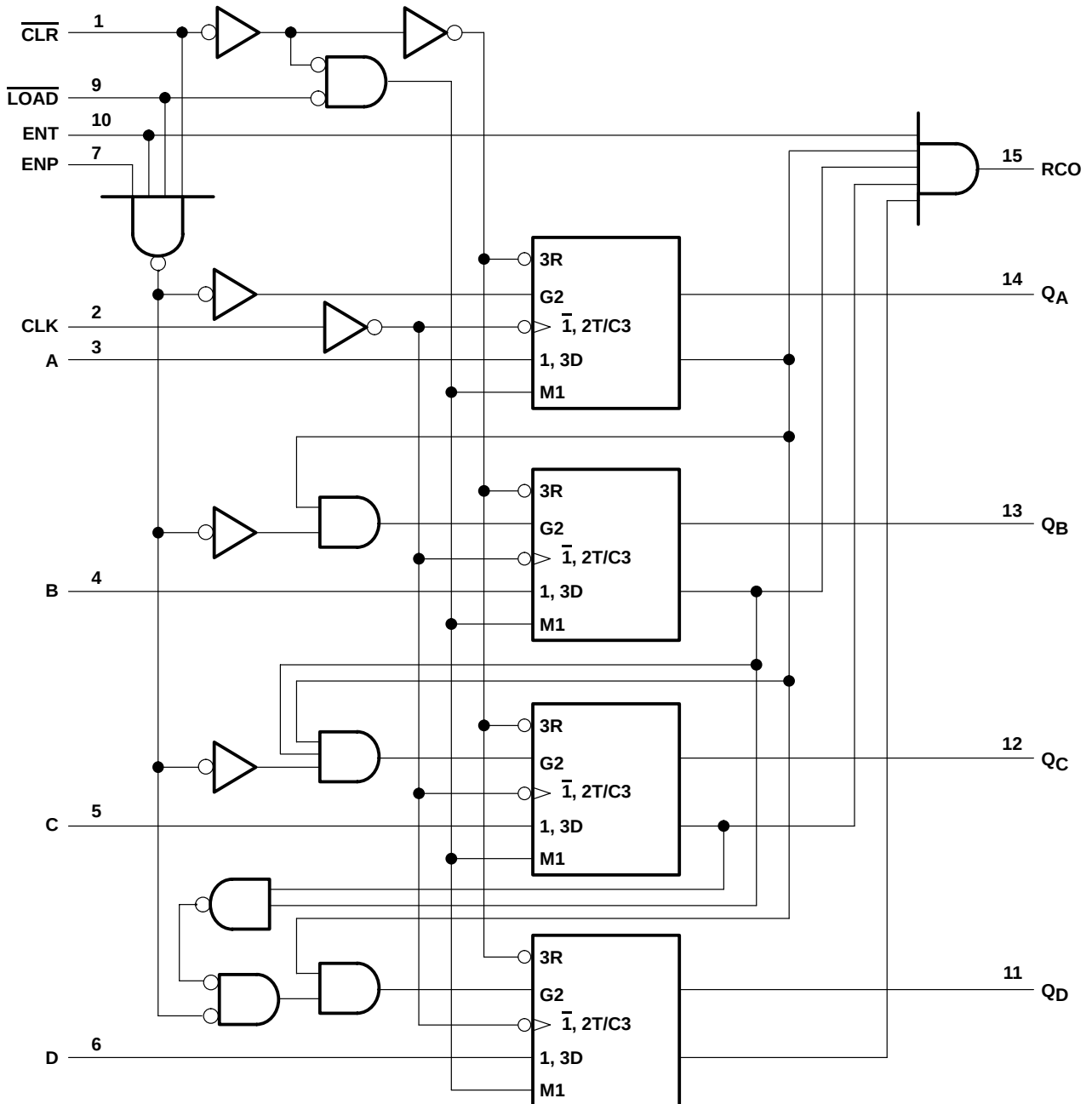
state diagram



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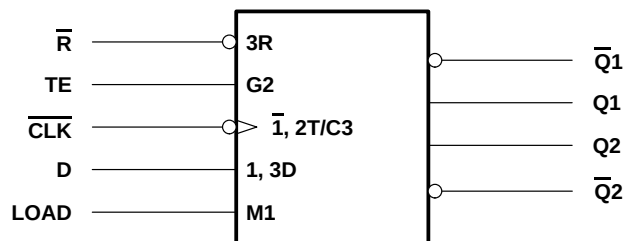
logic diagram (positive logic)



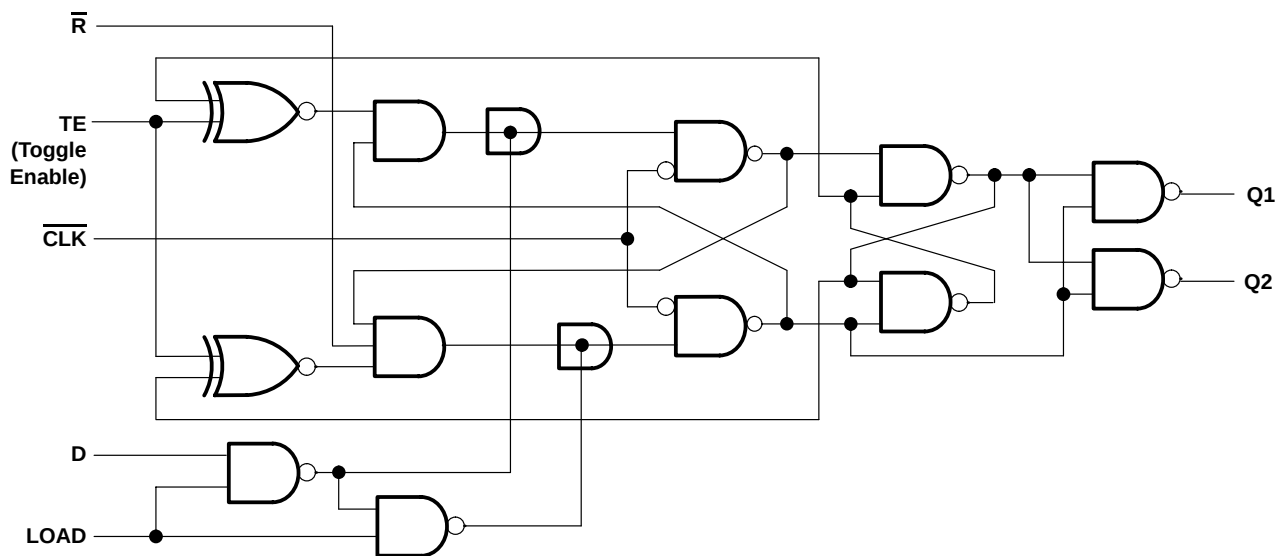
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logic symbol, each flip-flop



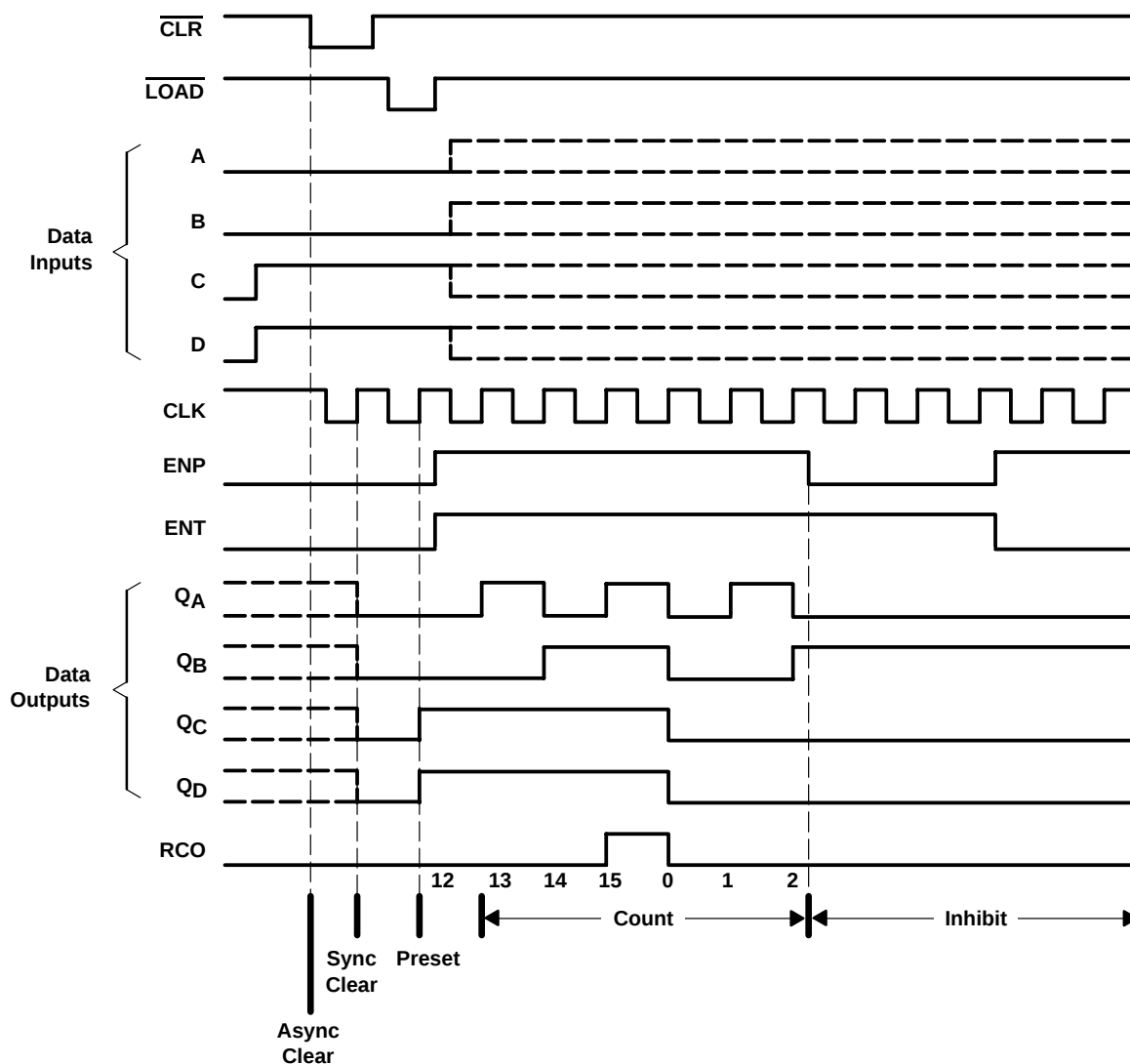
logic diagram, each flip-flop (positive logic)



typical clear, preset, count, and inhibit sequences

The following timing sequence is illustrated below:

1. Clear outputs to zero
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the high state	–0.5 V to V_{CC}
Current into any output in the low state	40 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
DB package	82°C/W
N package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{IK} Input clamp current			–18	mA
I_{OH} High-level output current			–1	mA
I_{OL} Low-level output current			20	mA
T_A Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -1$ mA	2.5	3.4		V
	$V_{CC} = 4.75$ V, $I_{OH} = -1$ mA	2.7			
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 20$ mA		0.3	0.5	V
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20	μA
I_{IL}	ENP, CLK, A, B, C, D			–0.6	mA
	ENT, LOAD			–1.2	
	CLR			–1.2	
$I_{OS}^{\S}$	$V_{CC} = 5.5$ V, $V_O = 0$	–60		–150	mA
I_{CC}	$V_{CC} = 5.5$ V		37	55	mA

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

^{\S} Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
				MIN	MAX			
f_{clock}	Clock frequency			0	100	0	90	MHz
t_w	Pulse duration	CLK high or low (loading)		5		5		ns
		CLK (counting)	High	4		4		
			Low	6		7		
t_{su}	Setup time	Data before CLK $\uparrow$		High or low	5	5		ns
		$\overline{\text{LOAD}}$ and $\overline{\text{CLR}}$ before CLK $\uparrow$	High	11	11.5			
			Low	8.5	9.5			
		ENP and ENT before CLK $\uparrow$	High	11	11.5			
			Low	5	5			
t_h	Hold time	Data after CLK $\uparrow$		High or low	2	2		ns
		LOAD and CLR after CLK $\uparrow$	High	2	2			
			Low	0	0			
		ENP and ENT after CLK $\uparrow$	High or low	0	0			

switching characteristics (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5\text{ V TO } 5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, $T_A = \text{MIN TO MAX}^\dagger$		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			100	120		90		MHz
t_{PLH}	CLK ($\overline{\text{LOAD}}$ high)	Any Q	2.7	5.1	7.5	2.7	8.5	ns
t_{PHL}			2.7	7.1	10	2.7	11	
t_{PLH}	CLK (LOAD low)	Any Q	3.2	5.6	8.5	3.2	9.5	ns
t_{PHL}			3.2	5.6	8.5	3.2	9.5	
t_{PLH}	CLK	RCO	4.2	9.6	14	4.2	15	ns
t_{PHL}			4.2	9.6	14	4.2	15	
t_{PLH}	ENT	RCO	1.7	4.1	7.5	1.7	8.5	ns
t_{PHL}			1.7	4.1	7.5	1.7	8.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 4: Load circuits and waveforms are shown in Figure 1.

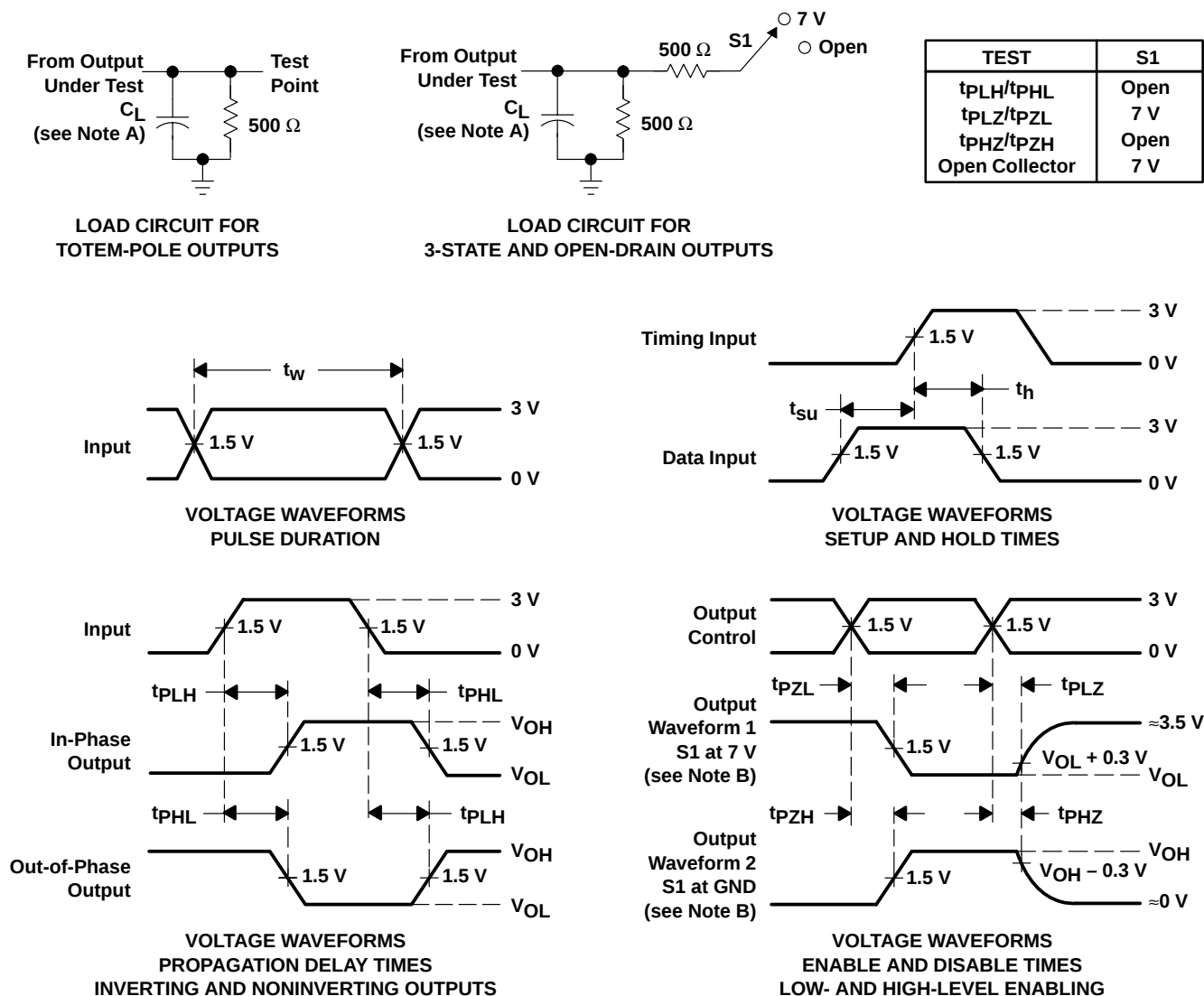


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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, duty cycle = 50%.
 - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74F163AD	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	0 to 70	F163A
SN74F163ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F163A
SN74F163ADR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F163A
SN74F163AN	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F163AN
SN74F163AN.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F163AN
SN74F163ANE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F163AN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F163ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F163ADR	SOIC	D	16	2500	340.5	336.1	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74F163AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74F163AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74F163AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74F163AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74F163ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74F163ANE4	N	PDIP	16	25	506	13.97	11230	4.32

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



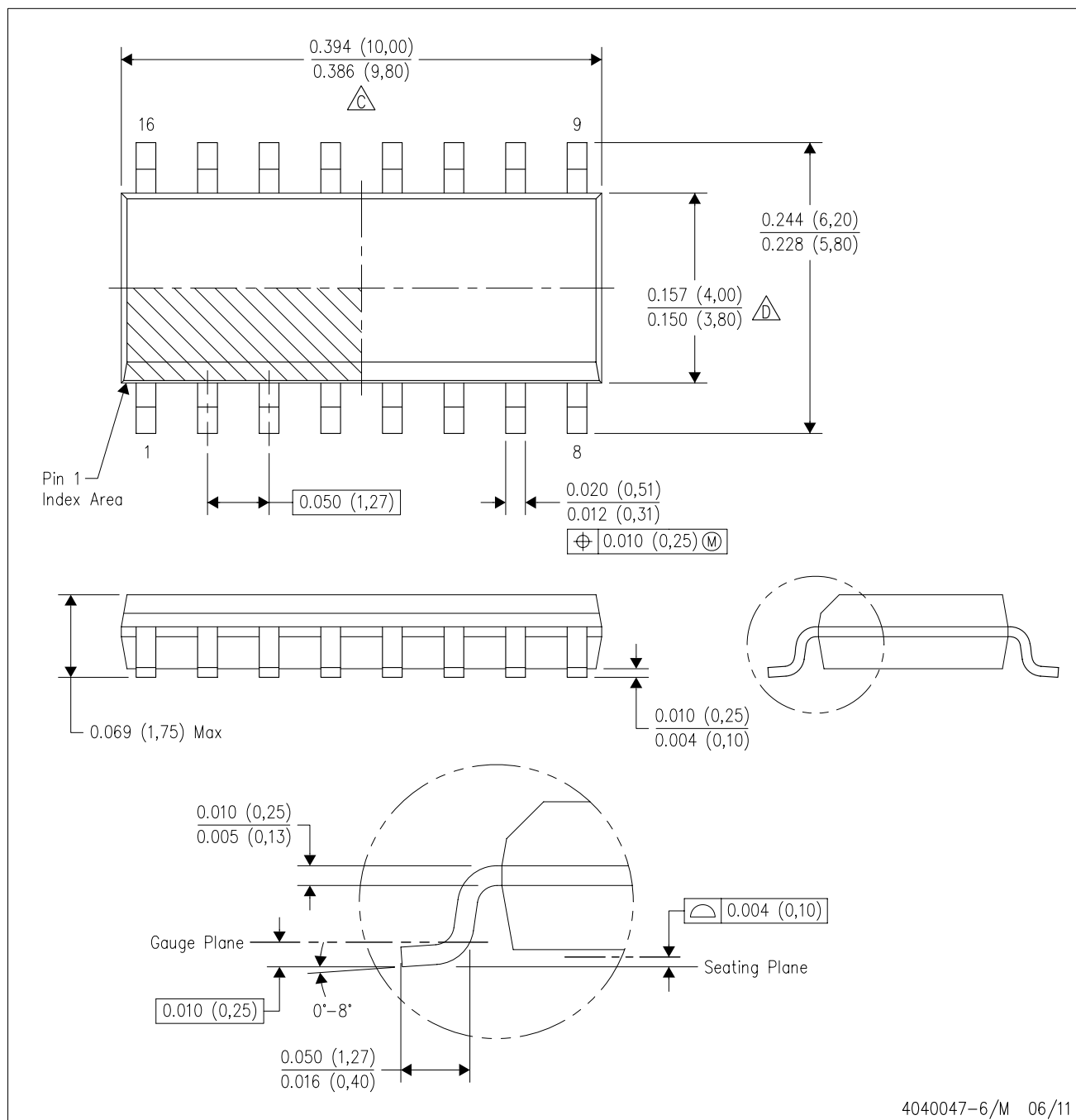
14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

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