

## POWER-DISTRIBUTION SWITCHES

### FEATURES

- 80-mΩ High-Side MOSFET Switch
- 500 mA Continuous Current per Channel
- Independent Thermal and Short-Circuit Protection With Overcurrent Logic Output
- Operating Range: 2.7-V to 5.5-V
- CMOS- and TTL-Compatible Enable Inputs
- 2.5-ms Typical Rise Time
- Undervoltage Lockout
- 10 µA Maximum Standby Supply Current
- Bidirectional Switch
- Available in 8-Pin and 16-Pin SOIC Packages
- Ambient Temperature Range, 0°C to 85°C
- ESD Protection

### DESCRIPTION

The TPS2080, TPS2081, and TPS2082 dual and the TPS2085, TPS2086 and TPS2087 quad power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered.

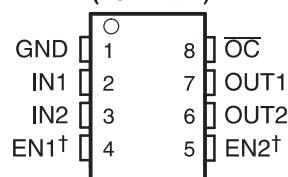
The TPS208x devices incorporate 80-mΩ N-channel MOSFET high-side power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by an independent logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS208x limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent (OCx) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present. The TPS208x devices are designed to current limit at 1.0-A load.

TPS2080, TPS2081, AND TPS2082

D PACKAGE

(TOP VIEW)

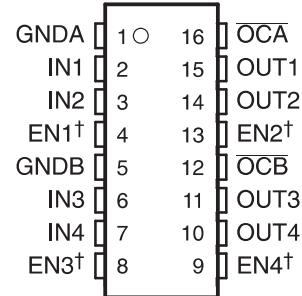


† See Available Options table

TPS2085, TPS2086 AND TPS2087

D PACKAGE

(TOP VIEW)



† See Available Options table

### GENERAL SWITCH CATALOG

33 mΩ, Single	80 mΩ, Single	80 mΩ, Dual	80 mΩ, Dual	80 mΩ, Triple	80 mΩ, Quad	80 mΩ, Quad
TPS201xA 0.2 A to 2 A	TPS2014 600 mA	TPS2042B 500 mA	TPS2080 500 mA	TPS2043B 500 mA	TPS2044B 500 mA	TPS2085 500 mA
TPS202x 0.2 A to 2 A	TPS2015 1 A	TPS2052B 500 mA	TPS2081 500 mA	TPS2053B 500 mA	TPS2054B 500 mA	TPS2086 500 mA
TPS203x 0.2 A to 2 A	TPS2041B 500 mA	TPS2046B 250 mA	TPS2082 500 mA	TPS2047B 250 mA	TPS2048B 250 mA	TPS2087 500 mA
	TPS2051B 500 mA	TPS2056 250 mA	TPS2083 250 mA	TPS2057A 250 mA	TPS2058 250 mA	TPS2095 250 mA
	TPS2045A 250 mA	TPS2062 1 A	TPS2084 250 mA	TPS2063 1 A		TPS2096 250 mA
	TPS2049 100 mA	TPS2056 250 mA	TPS2085 250 mA	TPS2064 1.5 A		TPS2097 250 mA
	TPS2055A 250 mA	TPS2062 1 A	TPS2086 250 mA			
	TPS2061 1 A	TPS2066 1 A	TPS2087 250 mA			
	TPS2065 1 A	TPS2060 1.5 A	TPS2088 250 mA			
	TPS2068 1.5 A	TPS2064 1.5 A	TPS2089 250 mA			
	TPS2069 1.5 A					



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

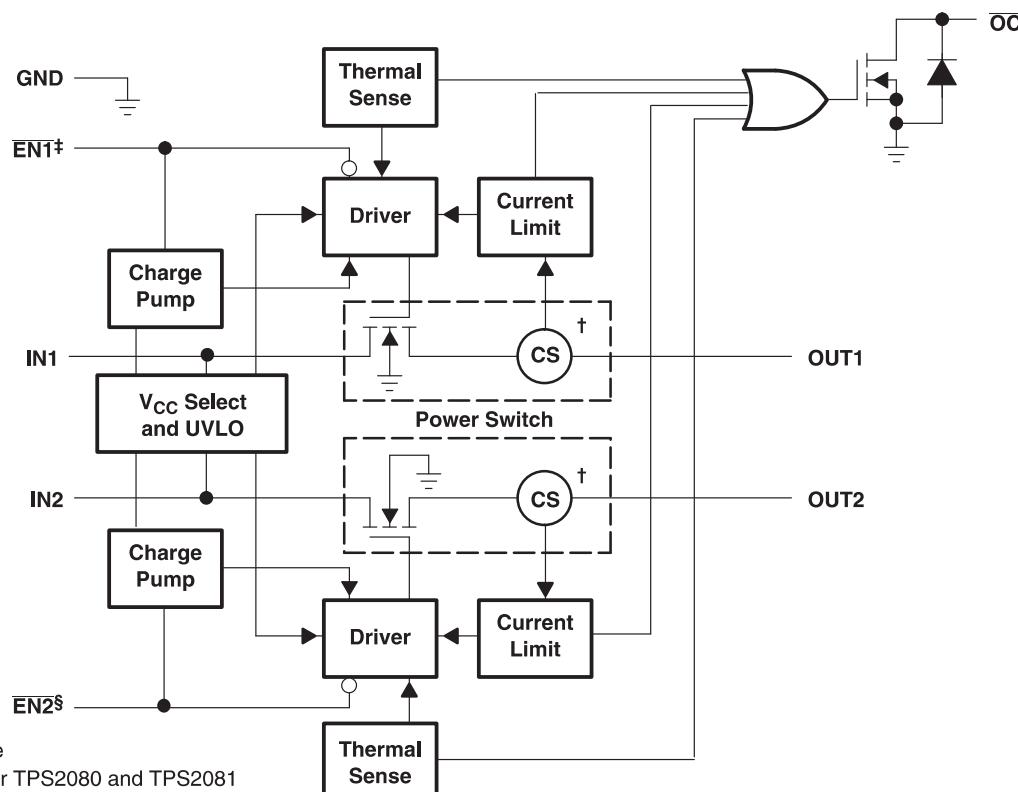
### AVAILABLE OPTIONS<sup>(1)</sup>

DUAL POWER DISTRIBUTION SWITCHES								
T <sub>A</sub>	ENABLE		RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES			
	EN1	EN2			SMALL OUTLINE (D) <sup>(2)</sup>			
0°C to 85°C	Active high	Active high	0.5	1.0	TPS2080D			
	Active high	Active low			TPS2081D			
	Active low	Active low			TPS2082D			
QUAD POWER DISTRIBUTION SWITCHES								
T <sub>A</sub>	ENABLE				TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES		
	EN1	EN2	EN3	DN4				
0°C to 85°C	Active high	Active high	Active high	Active high	0.5	1.0	TPS2085D	
	Active high	Active low	Active high	Active low			TPS2086D	
	Active low	Active low	Active low	Active low			TPS2087D	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2081DR).

**TPS2082 FUNCTIONAL BLOCK DIAGRAM**

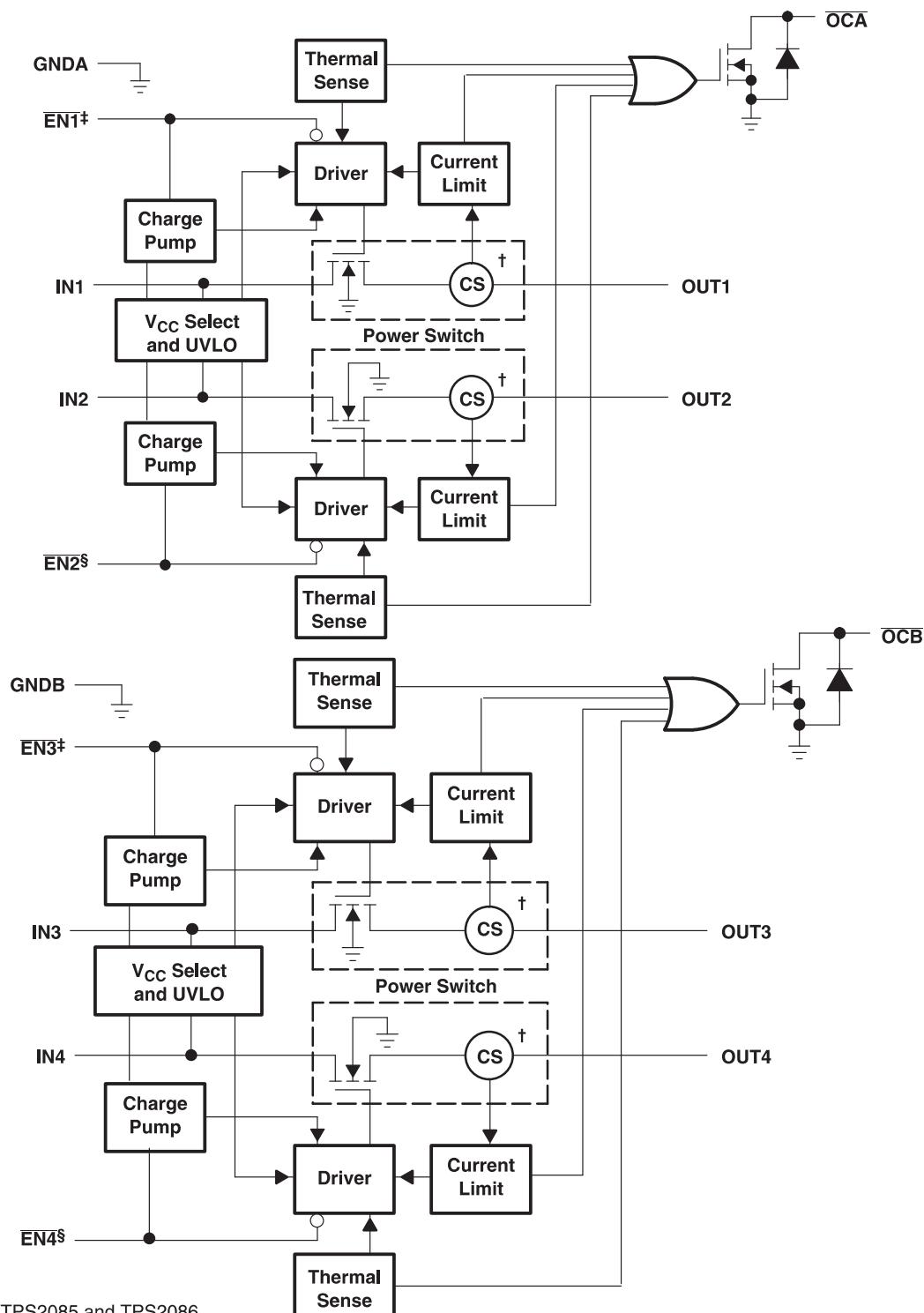


† Current sense

‡ Active high for TPS2080 and TPS2081

§ Active high for TPS2080

TPS2087 FUNCTIONAL BLOCK DIAGRAM



**TERMINAL FUNCTIONS**

DUAL POWER-DISTRIBUTION SWITCHES						
TERMINAL			I/O	DESCRIPTION		
NAME	NO.					
	TPS2080	TPS2081	TPS2082			
EN1			4	I	Enable input. Active low turns on power switch.	
EN2		5	5	I	Enable input. Active low turns on power switch.	
EN1	4	4		I	Enable input. Active high turns on power switch.	
EN2	5			I	Enable input. Active high turns on power switch.	
GND	1	1	1	I	Ground	
IN1	2	2	2	I	N-Channel MOSFET Drain	
IN2	3	3	3	I	N-Channel MOSFET Drain	
OC	8	8	8	O	Overcurrent. Open drain output active low	
OUT1	7	7	7	O	Power-switch output	
OUT2	6	6	6	O	Power-switch output	
QUAD POWER-DISTRIBUTION SWITCHES						
TERMINAL			I/O	DESCRIPTION		
NAME	NO.					
	TPS2085	TPS2086	TPS2087			
EN1			4	I	Enable input. Active low turns on power switch.	
EN2		13	13	I	Enable input. Active low turns on power switch.	
EN3			8	I	Enable input. Active low turns on power switch.	
EN4		9	9	I	Enable input. Active low turns on power switch.	
EN1	4	4		I	Enable input. Active high turns on power switch.	
EN2	13			I	Enable input. Active high turns on power switch.	
EN3	8	8		I	Enable input. Active high turns on power switch.	
EN4	9			I	Enable input. Active high turns on power switch.	
GNDA	1	1	1		Ground for IN1 and IN2 switch and circuitry	
GNDB	5	5	5		Ground for IN3 and IN4 switch and circuitry	
IN1	2	2	2	I	N-channel MOSFET drain	
IN2	3	3	3	I	N-channel MOSFET drain	
IN3	6	6	6	I	N-channel MOSFET drain	
IN4	7	7	7	I	N-channel MOSFET drain	
OCA	16	16	16	O	Overcurrent indicator for switch 1 and switch 2. Active-low open drain output.	
OCB	12	12	12	O	Overcurrent indicator for switch 3 and switch 4. Active low open drain output	
OUT1	15	15	15	O	Power-switch output	
OUT2	14	14	14	O	Power-switch output	
OUT3	11	11	11	O	Power-switch output	
OUT4	10	10	10	O	Power-switch output	

## DETAILED DESCRIPTION

### POWER SWITCH

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 mΩ ( $V_{I(IN)} = 5V$ ). Configured as a high-side switch, the power switch prevents current flow from OUTx to IN and IN to OUTx when disabled. The power switch supplies a minimum of 500 mA per switch.

### CHARGE PUMP

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7V and requires very little supply current.

### DRIVER

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

### ENABLE ( $\bar{EN}_x$ or $EN_x$ )

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10  $\mu A$  when a logic high is present on  $\bar{EN}_x$  or a logic low is present on  $EN_x$ . A logic low input on  $\bar{EN}_x$  or logic high on  $EN_x$  restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

### OVERCURRENT ( $\bar{OC}_x$ )

The  $\bar{OC}_x$  open drain output is asserted (active low) when an overcurrent or over temperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

### CURRENT SENSE

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

### THERMAL SENSE

The TPS208x implements a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks to determine which power switch is in an overcurrent condition and turns off that switch, thus isolating the fault without interrupting operation of the adjacent power switch. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The ( $OC_x$ ) open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

### UNDERVOLTAGE LOCKOUT

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		VALUE	UNIT	
$V_{I(IN)}$	Input voltage range <sup>(2)</sup>	-0.3 to 6	V	
$V_{O(OUTx)}$	Output voltage range <sup>(2)</sup>	-0.3 to $V_{I(IN)} + 0.3$	V	
$V_{I(ENx)}$ or $V_{I(ENx)}$	Input voltage range	-0.3 to 6	V	
$I_{O(OUTx)}$	Continuous output current	Internally Limited		
	Continuous total power dissipation	See Dissipation Rating Table		
$T_J$	Operating virtual junction temperature range	0 to 125	°C	
$T_{stg}$	Storage temperature range	-65 to 150	°C	
	Lead temperature soldering 1.6 mm (1/16 inch) from case for 10 seconds	260	°C	
ESD	Electrostatic discharge protection	Human body model	2	kV
		Machine model	200	V
		Charged device model (CDM)	750	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND.

## DISSIPATION RATINGS TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D-8	725 mW	5.8 mW/°C	464 mW	377 mW
D-16	1123 mW	9 mW/°C	719 mW	584 mW

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
$V_{I(IN)}$	Input voltage	2.7	5.5	V
$V_{I(ENx)}$ or $V_{I(ENx)}$	Input voltage	0	5.5	V
$I_O$	Continuous output current (per switch)	0	500	mA
$T_J$	Operating virtual junction temperature	0	125	°C

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range,  $V_{I(IN)} = 5.5$  V,  $I_O$  = rated current,  $V_{I(ENx)} = 0$  V,  $V_{I(ENx)} = V_{I(INx)}$  (unless otherwise noted)

SUPPLY CURRENT							
PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Supply current, low-level output	No Load on OUT	$V_{I(ENx)} = V_{I(IN)}$ , $V_{I(ENx)} = 0$ V	$T_J = 25^\circ\text{C}$	0.025	1	10	$\mu\text{A}$
Supply current, high-level output			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$				
Leakage current	OUT connected to ground	$V_{I(ENx)} = V_{I(IN)}$ , $V_{I(ENx)} = 0$ V	$T_J = 25^\circ\text{C}$	85	110	100	$\mu\text{A}$
Reverse leakage current			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$				

## ELECTRICAL CHARACTERISTICS (Continued)

over recommended operating junction temperature range,  $V_{I(IN)} = 5.5$  V,  $I_O$  = rated current,  $V_{I(ENx)} = 0$  V,  $V_{I(ENx)} = V_{I(INx)}$  (unless otherwise noted)

POWER SWITCH		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
PARAMETER						
$r_{DS(on)}$	Static drain-source on-state resistance	$V_{I(IN)} = 5$ V, $T_J = 25^\circ\text{C}$ , $I_O = 0.5$ A			80	100
		$V_{I(IN)} = 5$ V, $T_J = 85^\circ\text{C}$ , $I_O = 0.5$ A			90	120
		$V_{I(IN)} = 5$ V, $T_J = 125^\circ\text{C}$ , $I_O = 0.5$ A			100	135
		$V_{I(IN)} = 3.3$ V, $T_J = 25^\circ\text{C}$ , $I_O = 0.5$ A			90	125
		$V_{I(IN)} = 3.3$ V, $T_J = 85^\circ\text{C}$ , $I_O = 0.5$ A			110	145
		$V_{I(IN)} = 3.3$ V, $T_J = 125^\circ\text{C}$ , $I_O = 0.5$ A			120	165
$t_r$	Rise time, output	$V_{I(IN)} = 5.5$ V, $R_L = 10\Omega$ , $T_J = 125^\circ\text{C}$ , $C_L = 1\ \mu\text{F}$			2.5	ms
		$V_{I(IN)} = 2.7$ V, $R_L = 10\Omega$ , $T_J = 125^\circ\text{C}$ , $C_L = 1\ \mu\text{F}$			3	
$t_f$	Fall time, output	$V_{I(IN)} = 5.5$ V, $R_L = 10\Omega$ , $T_J = 125^\circ\text{C}$ , $C_L = 1\ \mu\text{F}$			4.4	ms
		$V_{I(IN)} = 2.7$ V, $R_L = 10\Omega$ , $T_J = 125^\circ\text{C}$ , $C_L = 1\ \mu\text{F}$			2.5	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

ENABLE INPUT $V_{I(ENx)}$ or $V_{I(ENx)}$		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PARAMETER						
$V_{IH}$	High-level input voltage	$2.7\text{ V} \leq V_{I(IN)} \leq 5.5\text{ V}$		2		V
$V_{IL}$	Low-level input voltage	$4.5\text{ V} \leq V_{I(IN)} \leq 5.5\text{ V}$			0.8	V
		$2.7\text{ V} \leq V_{I(IN)} \leq 4.5\text{ V}$			0.4	
$I_I$	Input current	$V_{I(ENx)} = 0$ V and $V_{I(ENx)} = V_{I(IN)}$ , or $V_{I(ENx)} = V_{I(IN)}$ and $V_{I(ENx)} = 0$ V		-0.5	0.5	$\mu\text{A}$
$t_{on}$	Turnon time	$C_L = 100\ \mu\text{F}$ , $R_L = 10\ \mu\text{F}$			20	ms
$t_{off}$	Turnon time	$C_L = 100\ \mu\text{F}$ , $R_L = 10\ \mu\text{F}$			40	ms

CURRENT LIMIT		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
PARAMETER						
$I_{OS}$	Short-circuit output current	$V_{I(IN)} = 5$ V, OUT connected to GND, Device enabled into short circuit	0.7	1	1.3	A

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

UNDERVOLTAGE LOCKOUT		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PARAMETER						
Low-level input voltage			2		2.5	V
Hysteresis		$T_J = 25^\circ\text{C}$			100	mV

OVERCURRENT $\overline{OCx}$		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PARAMETER						
Sink current <sup>(1)</sup>		$V_O = 5$ V			10	$\text{mA}$
Output low voltage		$I_O = 5\ \text{mA}$ , $V_{OL(\overline{OCx})}$			0.5	V
Off-state current <sup>(1)</sup>		$V_O = 5$ V, $V_O = 3.3$ V			1	$\mu\text{A}$

(1) Specified by design, not production tested.

## PARAMETER MEASUREMENT INFORMATION

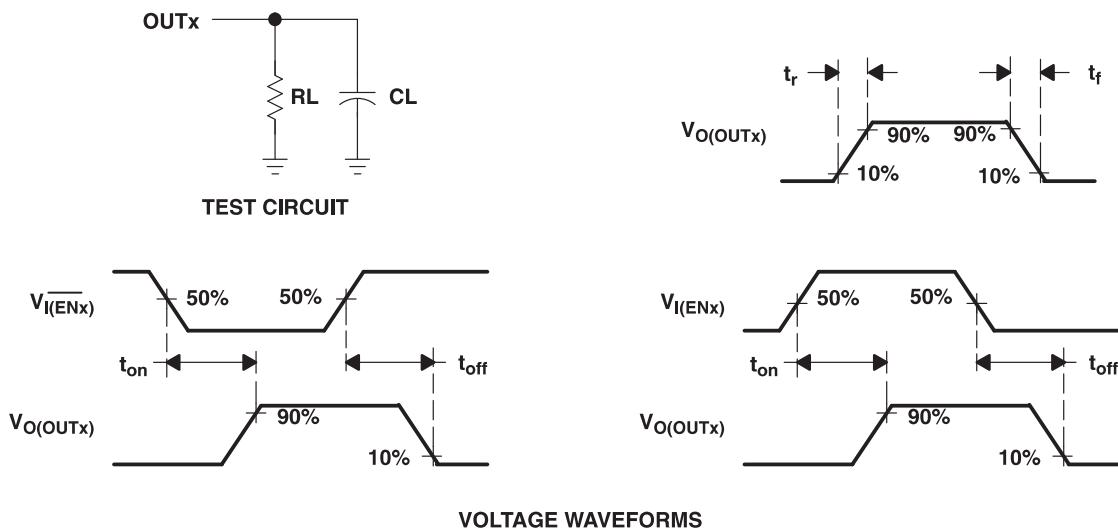
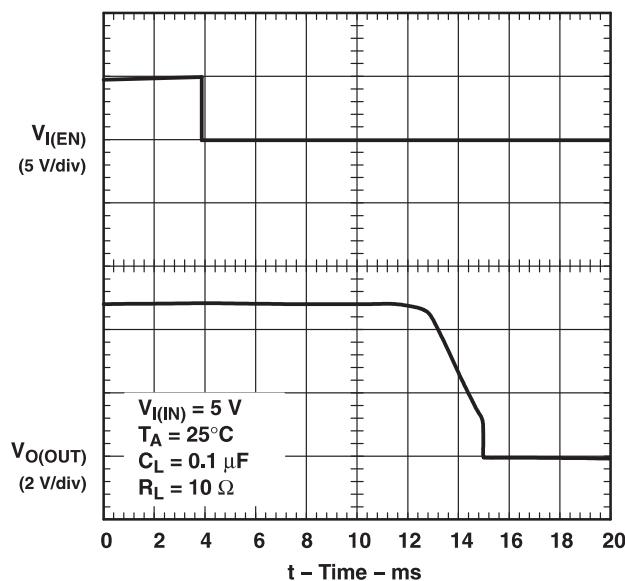
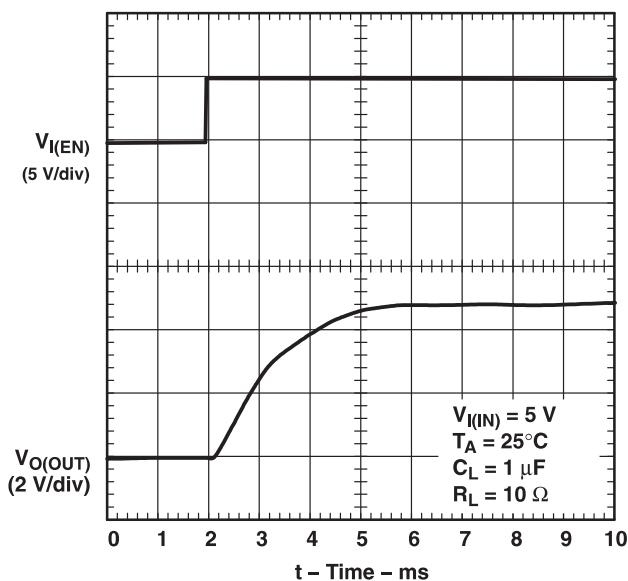
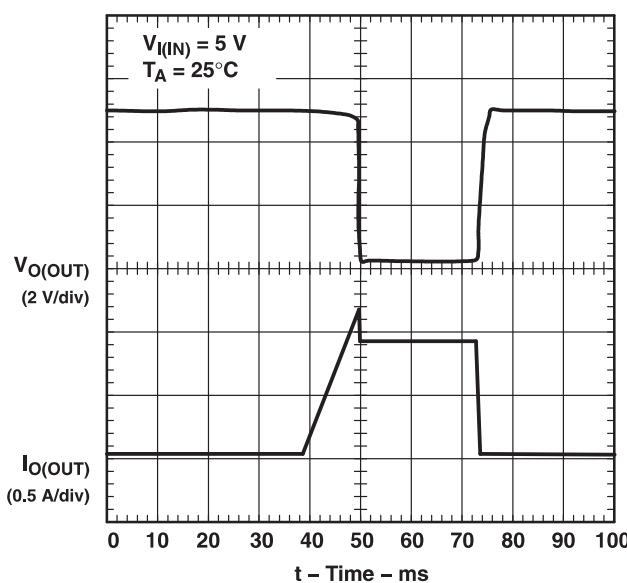
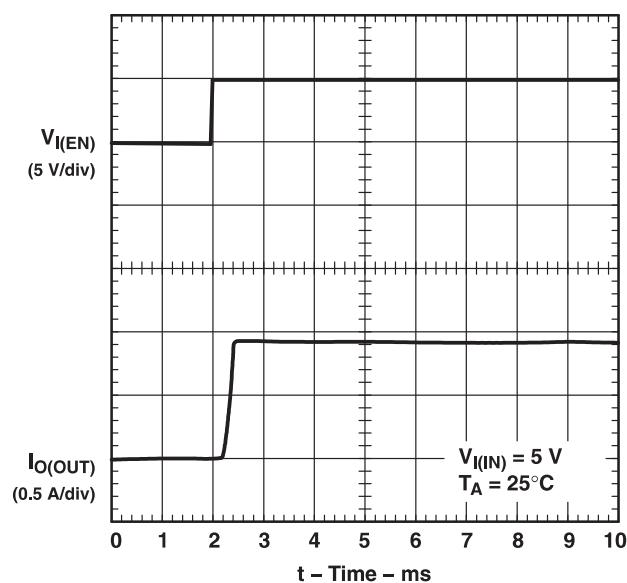
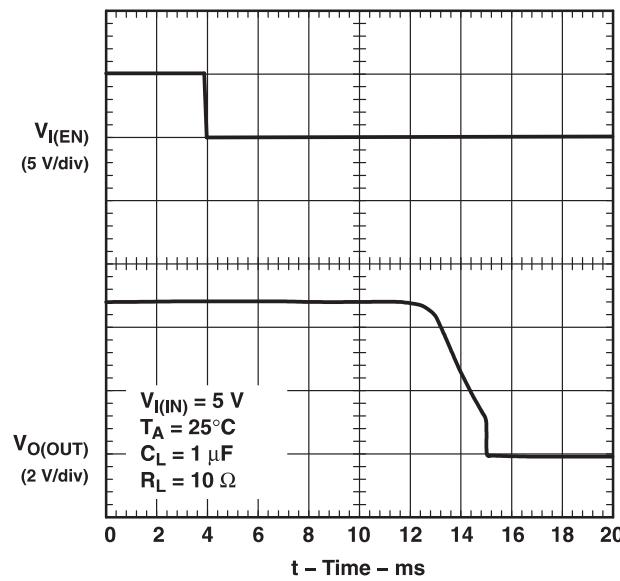
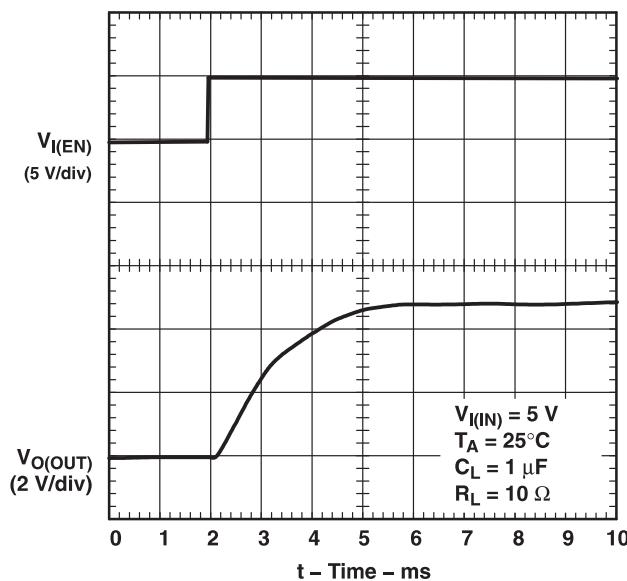


Figure 1. Test Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION (continued)



### PARAMETER MEASUREMENT INFORMATION (continued)

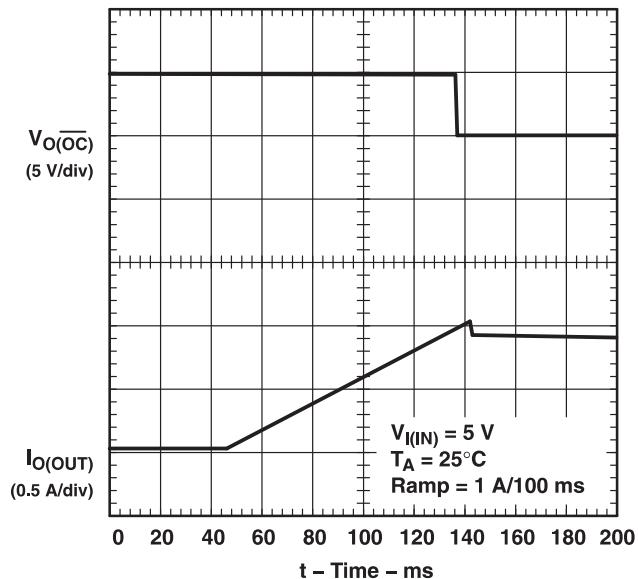


Figure 8. OC Response With Ramped Load on Enabled Device

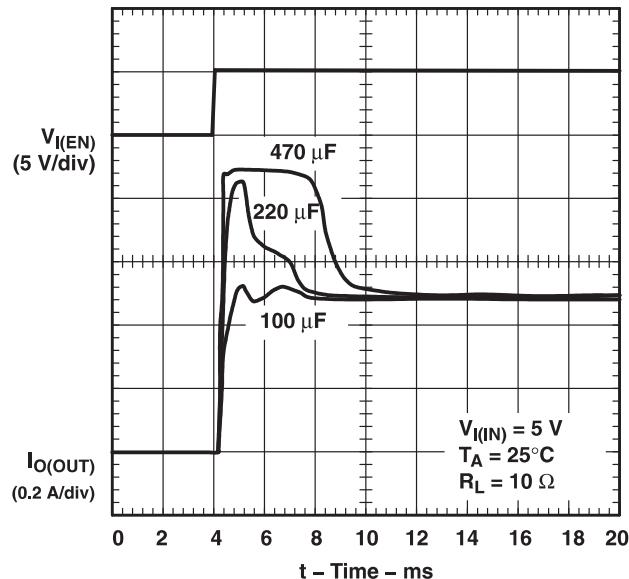


Figure 9. Inrush Current With 100- $\mu\text{F}$ , 220- $\mu\text{F}$  and 470- $\mu\text{F}$  Load Capacitance

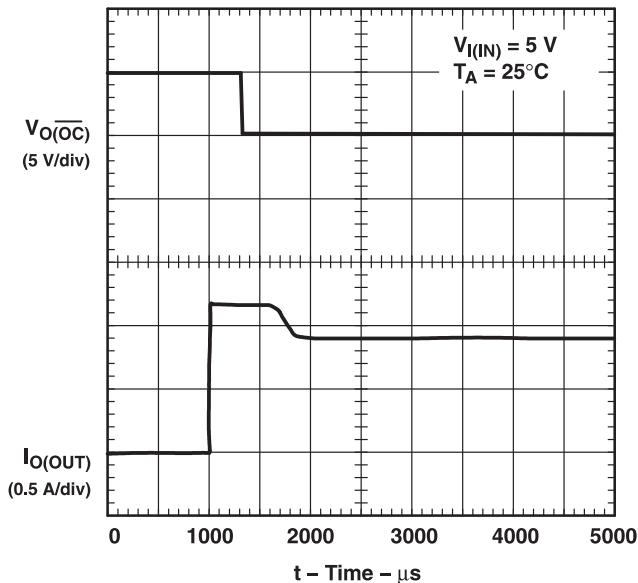


Figure 10. 4- $\Omega$  Load Connected to Enabled Device

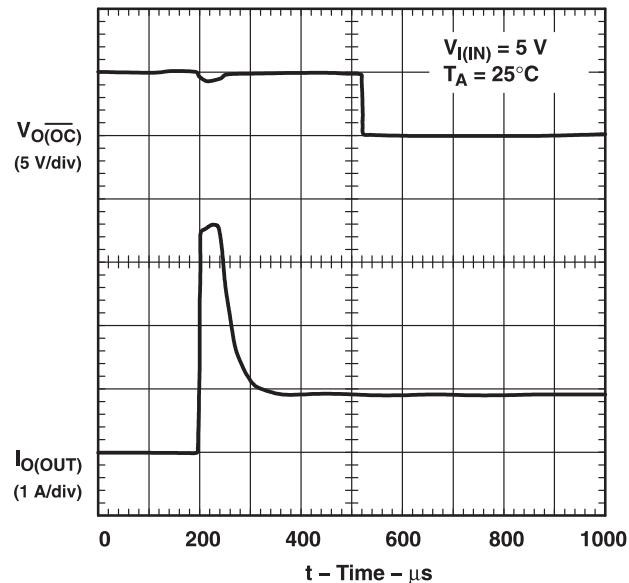


Figure 11. 1- $\Omega$  Load Connected to Enabled Device

## TYPICAL CHARACTERISTICS

TURNON DELAY TIME  
vs  
INPUT VOLTAGE

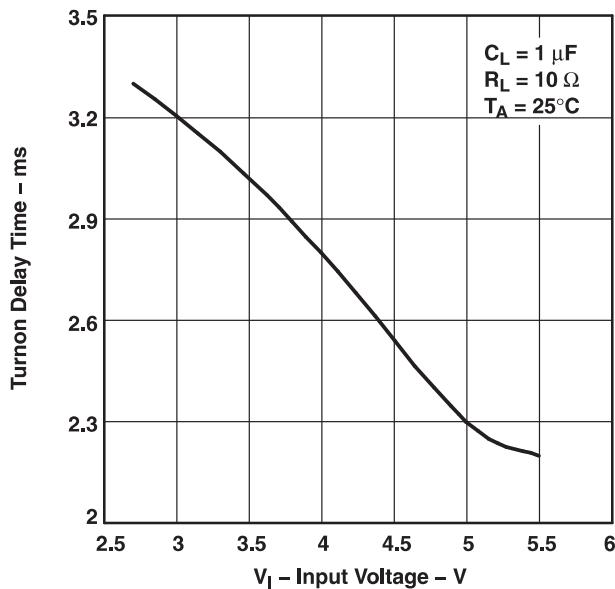


Figure 12.

TURNOFF DELAY TIME  
vs  
INPUT VOLTAGE

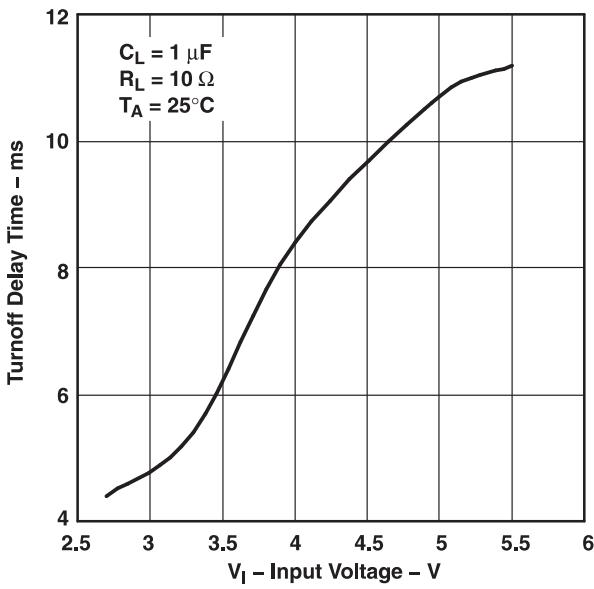


Figure 13.

RISE TIME  
vs  
INPUT VOLTAGE

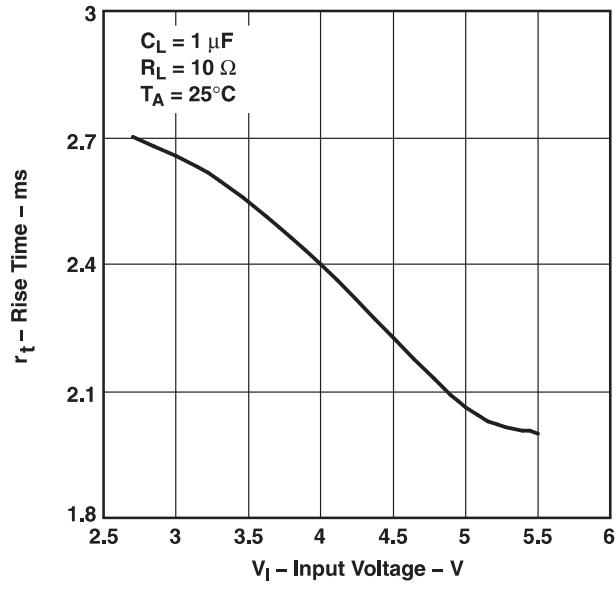


Figure 14.

FALL TIME  
vs  
INPUT VOLTAGE

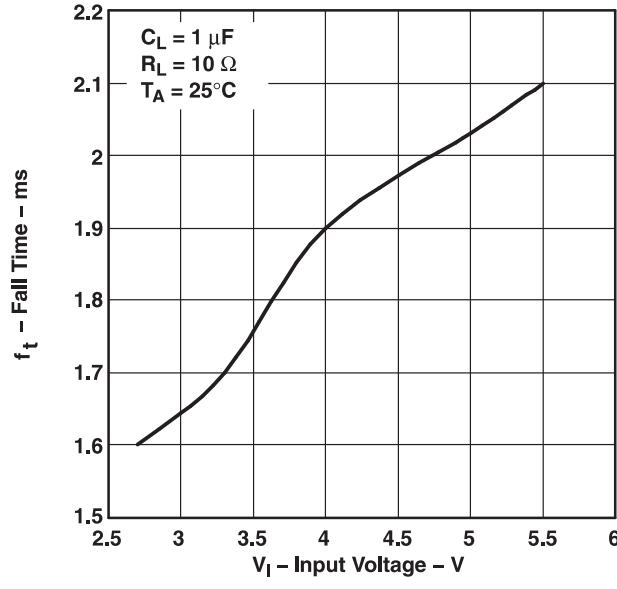


Figure 15.

**TYPICAL CHARACTERISTICS (continued)**

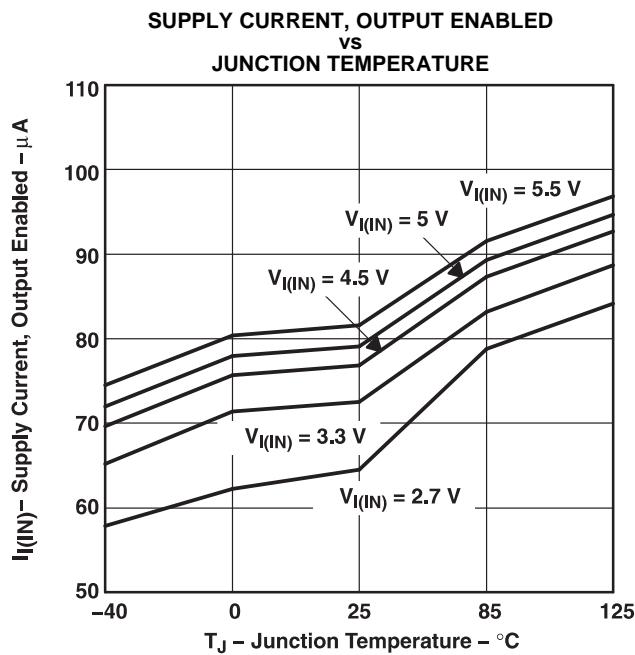


Figure 16.

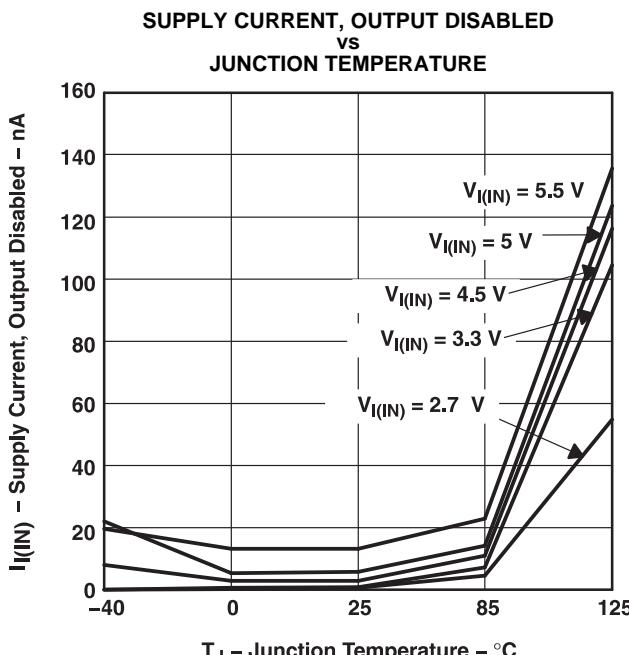


Figure 17.

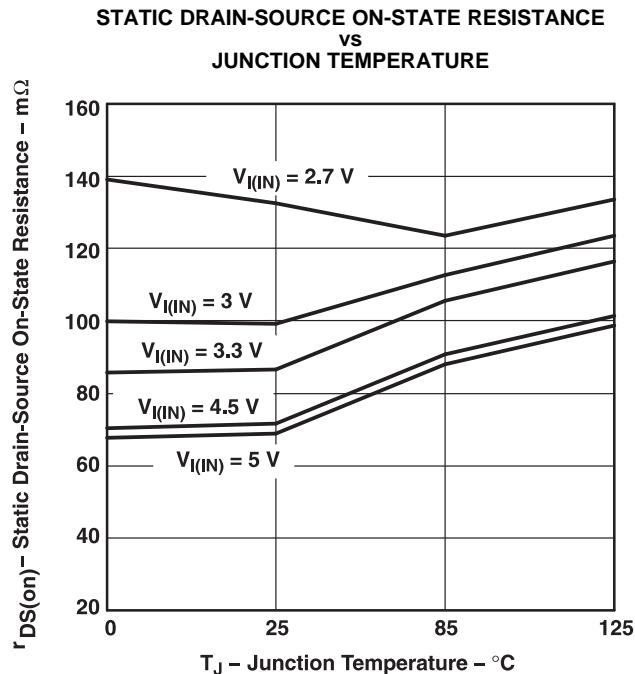


Figure 18.

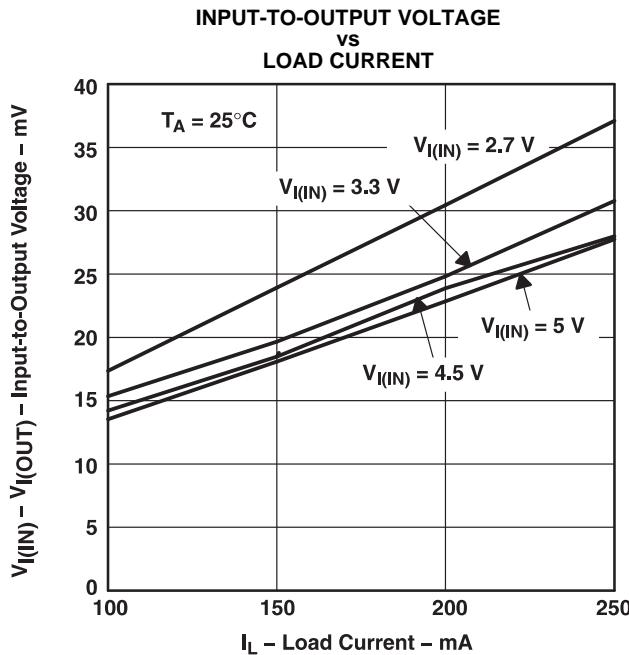


Figure 19.

TYPICAL CHARACTERISTICS (continued)

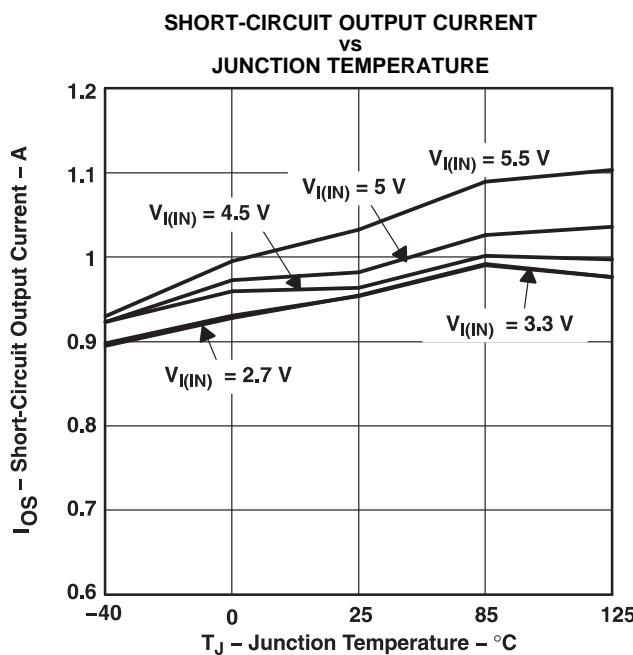


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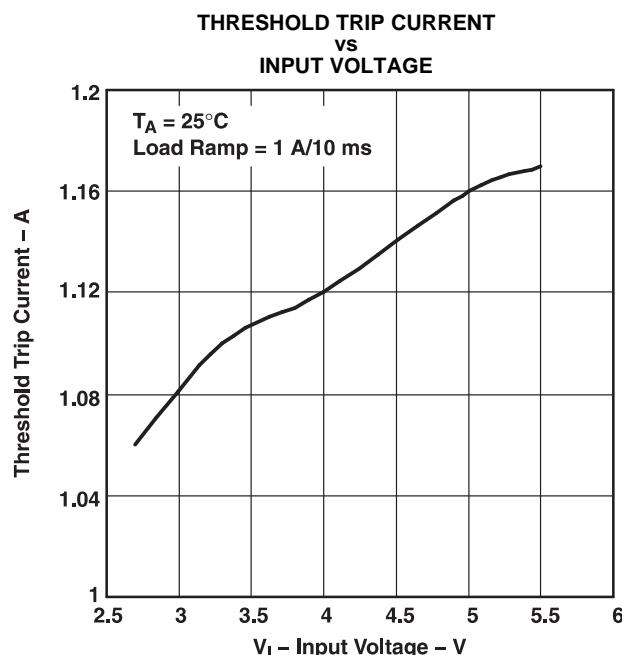


Figure 21.

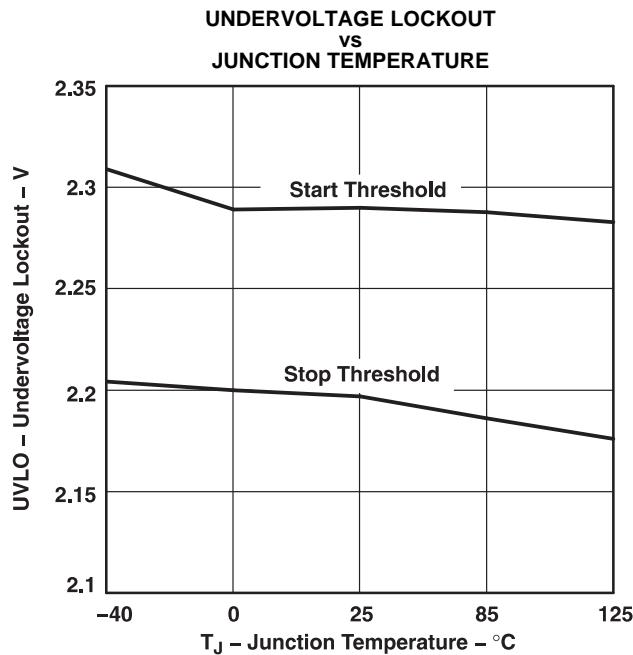


Figure 22.

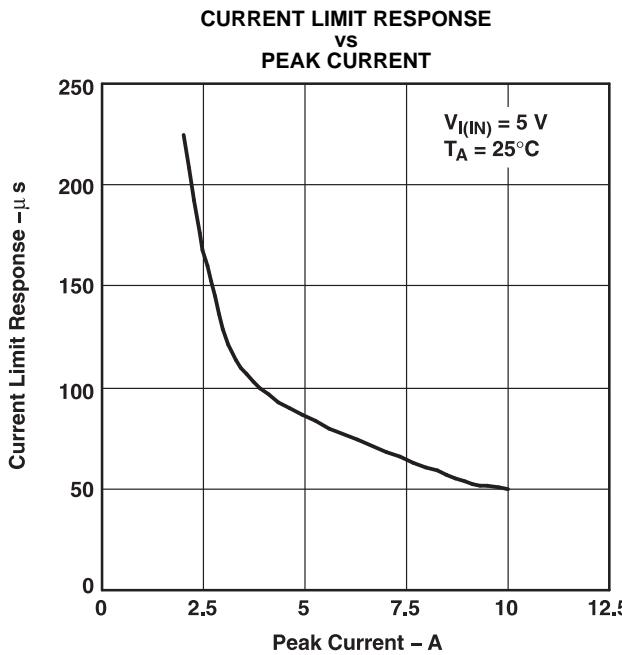


Figure 23.

## APPLICATION INFORMATION

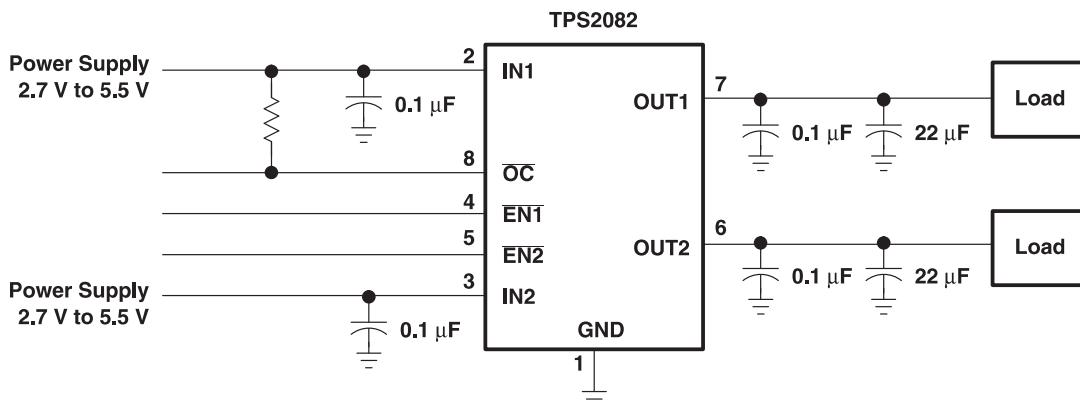


Figure 24. Typical Application

## POWER-SUPPLY CONSIDERATIONS

A 0.01- $\mu$ F to 0.1- $\mu$ F ceramic bypass capacitor between IN<sub>x</sub> and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01- $\mu$ F to 0.1- $\mu$ F ceramic capacitor improves the immunity of the device to short-circuit transients.

## OVERCURRENT

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before  $V_{I(IN)}$  has been applied (see [Figure 6](#)). The TPS208x senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, very high currents may flow for a short time before the current-limit circuit can react (see [Figure 10](#) and [Figure 11](#)). After the current-limit circuit has tripped (reached the overcurrent trip threshold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see [Figure 8](#)). The TPS208x is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

## OC RESPONSES

The OC open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. The TPS208x devices are designed to reduce false overcurrent reporting. An internal overcurrent transient filter eliminates the need to use external components to remove unwanted pulses. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

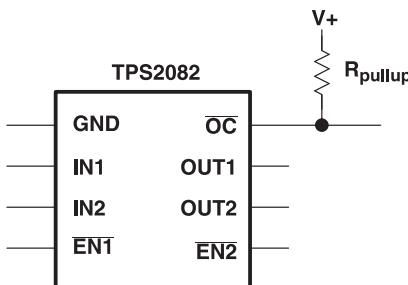


Figure 25. Typical Circuit for  $\overline{OC}$  Pin

## POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistance of these packages is high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the  $r_{DS(on)}$  of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read  $r_{DS(on)}$  from Figure 18. Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by the total number of switches being used, to get the total power dissipation coming from the N-channel MOSFETs.

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

$T_A$  = Ambient Temperature  $^{\circ}\text{C}$

$R_{\theta JA}$  = Thermal resistance SOIC =  $172^{\circ}\text{C/W}$  (for 8 pin),  $111^{\circ}\text{C/W}$  (for 16 pin)

$P_D$  = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

## THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS208x into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS208x implements a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature will rise. Once the die temperature rises to approximately  $140^{\circ}\text{C}$ , the internal thermal sense circuitry checks which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of  $140^{\circ}\text{C}$  and reach  $160^{\circ}\text{C}$ , both switches turn off. The  $\overline{OC}$  open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

## UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

## GENERIC HOT-PLUG APPLICATIONS (see Figure 26)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS208x, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS208x also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

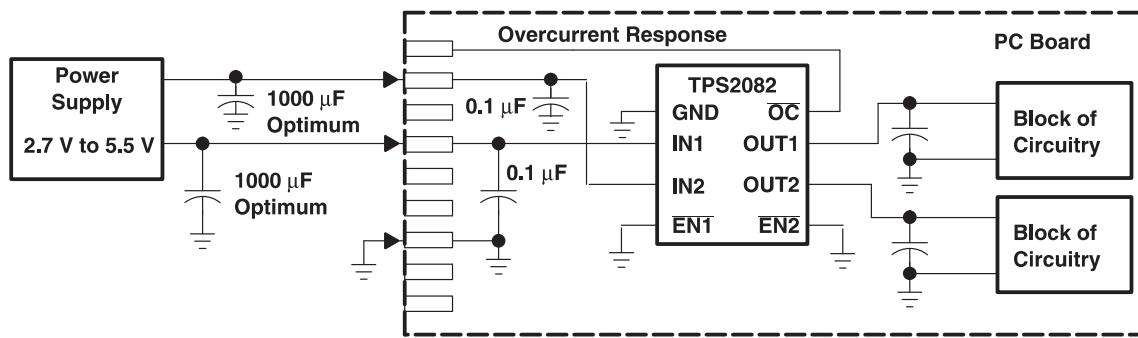


Figure 26. Typical Hot-Plug Implementation

By placing the TPS208x between the  $V_{CC}$  input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2080D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2080	<a href="#">Samples</a>
TPS2080DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2080	<a href="#">Samples</a>
TPS2080DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2080	<a href="#">Samples</a>
TPS2080DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2080	<a href="#">Samples</a>
TPS2081D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2081	<a href="#">Samples</a>
TPS2081DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2081	<a href="#">Samples</a>
TPS2082D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2082	<a href="#">Samples</a>
TPS2082DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2082	<a href="#">Samples</a>
TPS2082DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2082	<a href="#">Samples</a>
TPS2082DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2082	<a href="#">Samples</a>
TPS2085D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2085	<a href="#">Samples</a>
TPS2085DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2085	<a href="#">Samples</a>
TPS2085DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2085	<a href="#">Samples</a>
TPS2085DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2085	<a href="#">Samples</a>
TPS2086D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2086	<a href="#">Samples</a>
TPS2087D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2087	<a href="#">Samples</a>
TPS2087DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2087	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2087DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2087	<a href="#">Samples</a>
TPS2087DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2087	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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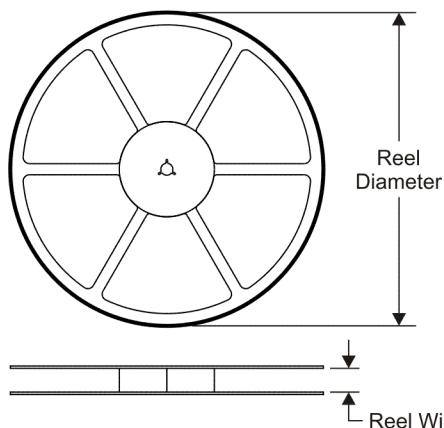
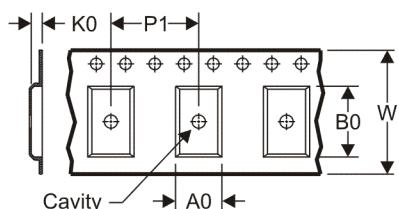


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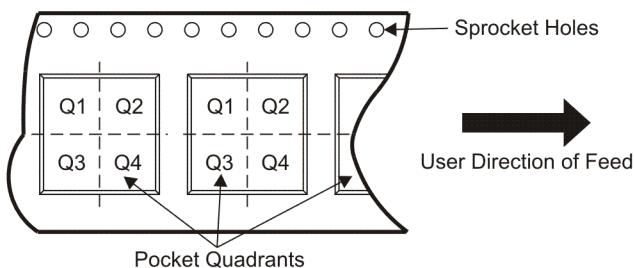
## PACKAGE OPTION ADDENDUM

10-Jun-2014

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2080DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2082DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2085DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TPS2087DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

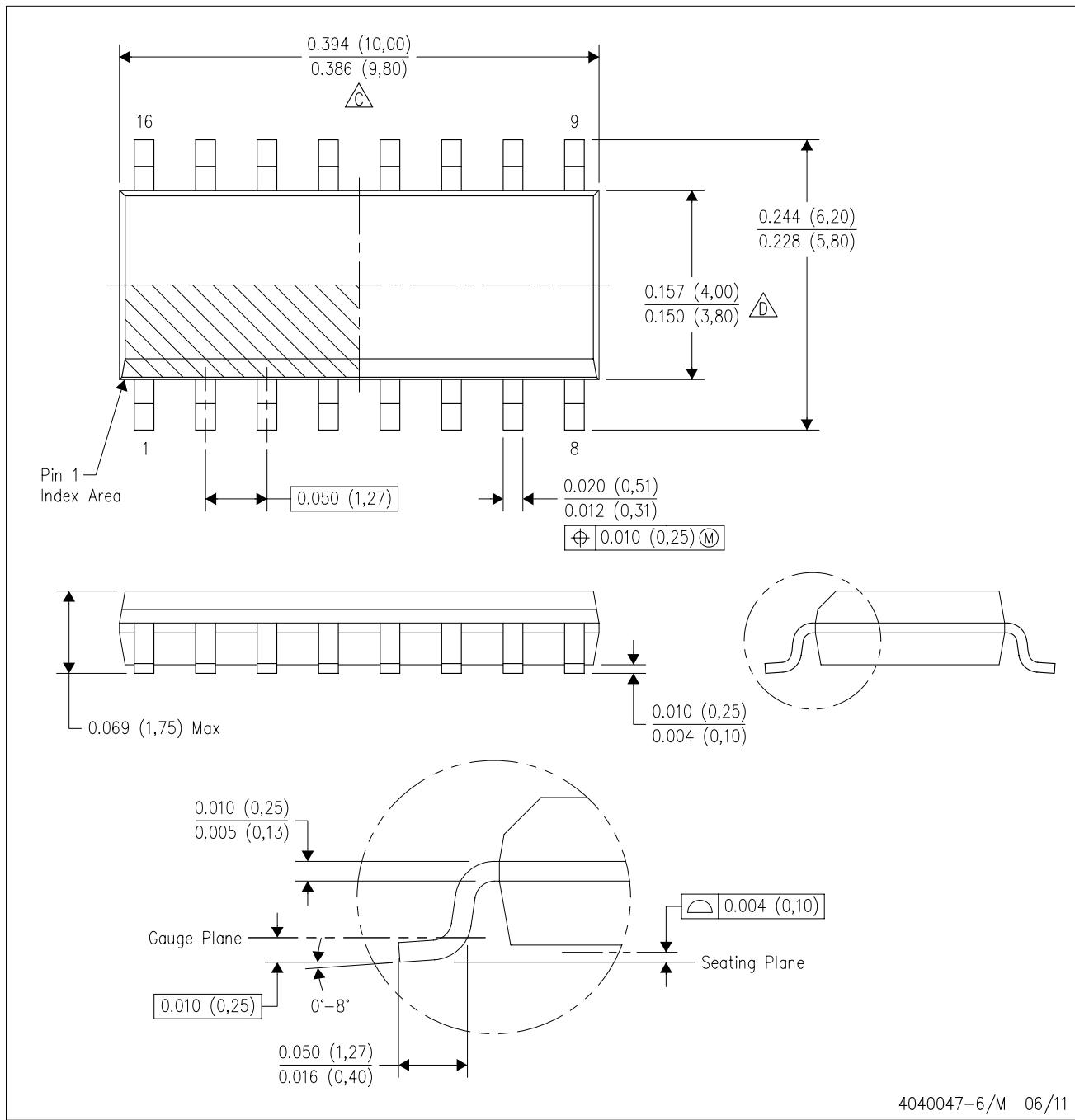
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2080DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2082DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2085DR	SOIC	D	16	2500	333.2	345.9	28.6
TPS2087DR	SOIC	D	16	2500	333.2	345.9	28.6

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

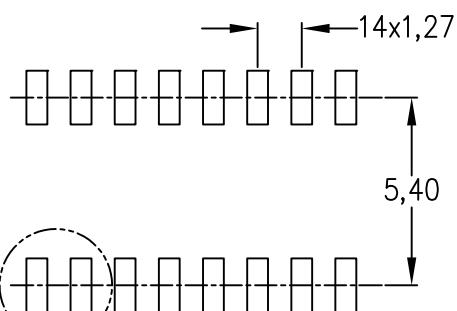
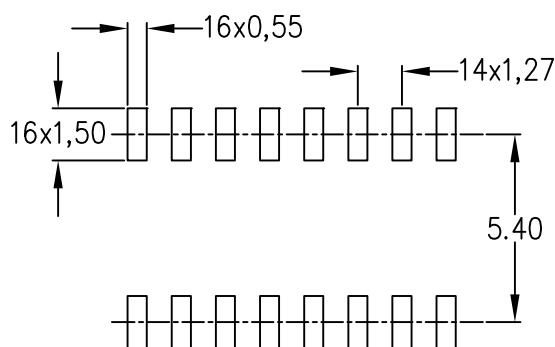
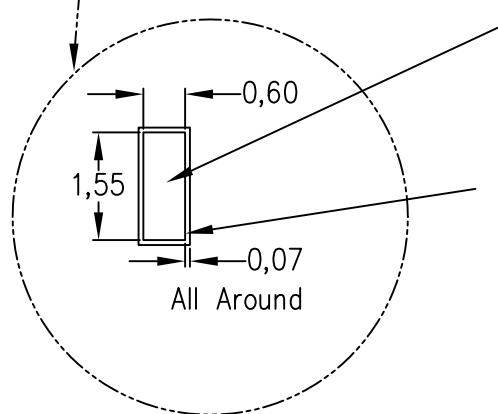
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

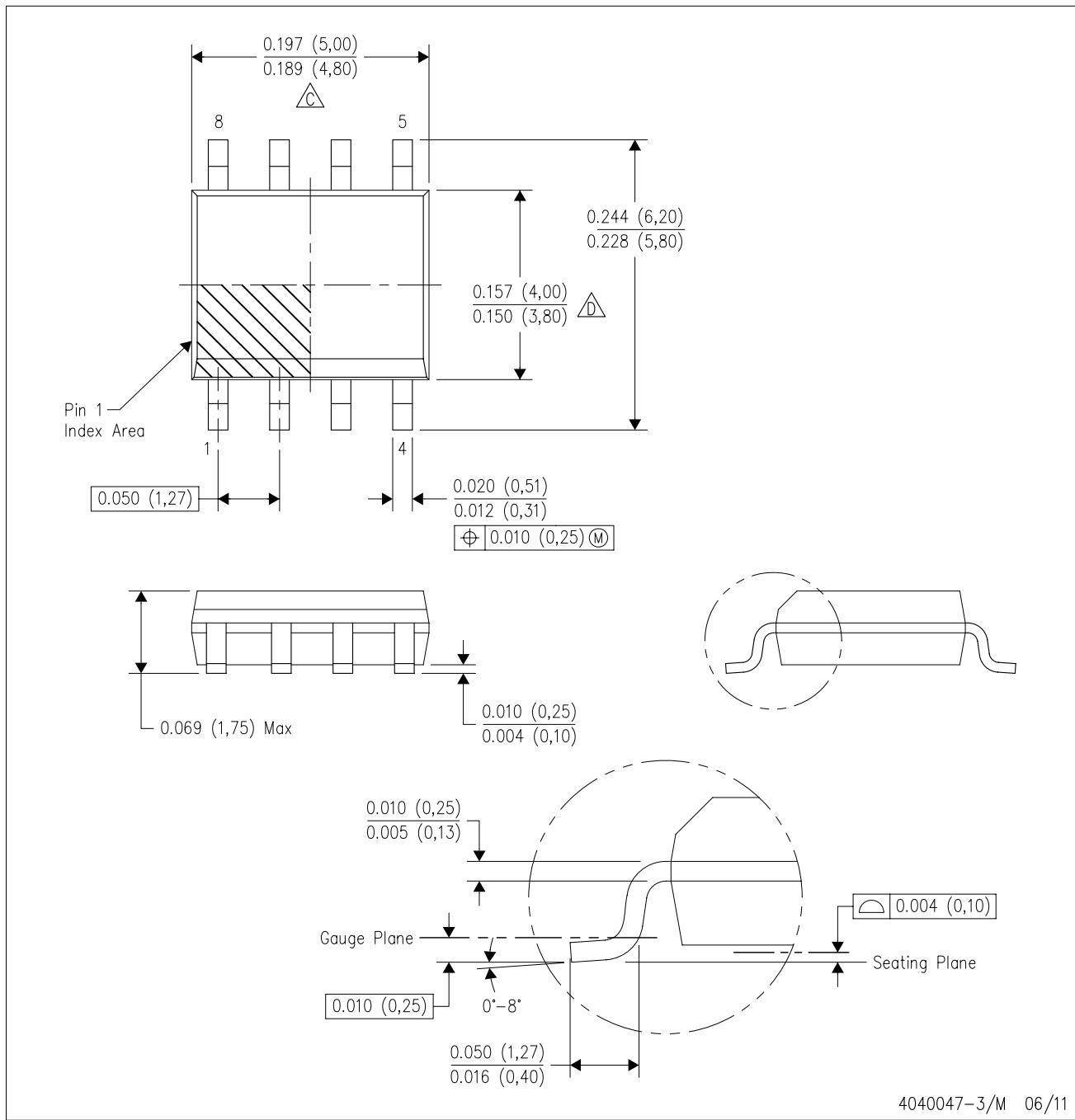
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
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- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

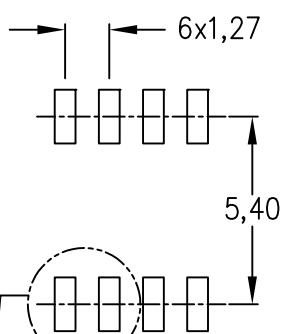
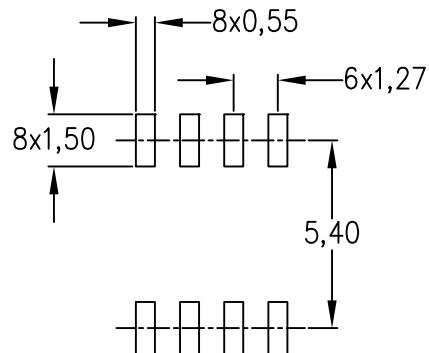
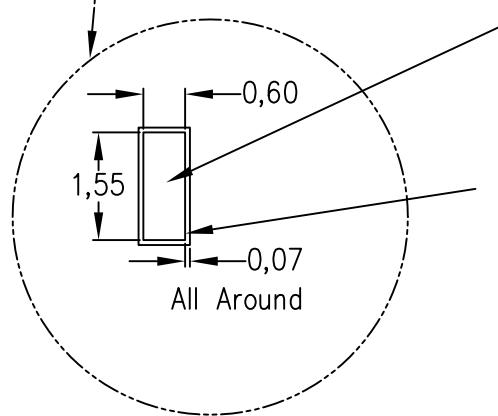
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

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NOTES:

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- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
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	<b>TI E2E Community</b>
	<a href="http://e2e.ti.com">e2e.ti.com</a>