Broadband Modem Mixed-Signal Front End

AD9875

FEATURES

Low Cost 3.3 V-CMOS Mixed-Signal Front End (MxFE™)
Converter for Broadband Modems
10-/12-Bit D/A Converter (TxDAC+®)
- **64/32 MSPS Input Word Rate**
- **2×/4× Interpolating LPF or BPF Transmit Filter**
- **128 MSPS DAC Output Update Rate**
- **Wide (26 MHz) Transmit Bandwidth**
- **Power-Down Mode**

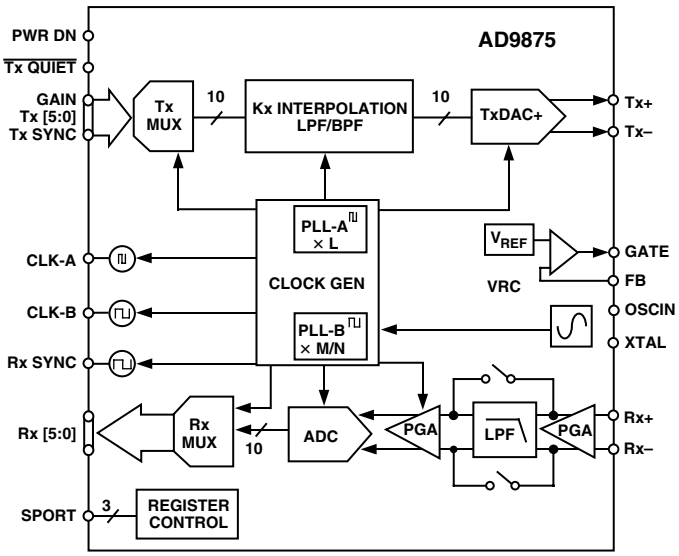
10-/12-Bit, 50 MSPS A/D Converter
- **Fourth Order Low-Pass Filter 12 MHz or 26 MHz with Bypass**
- **–6 dB to +36 dB Programmable Gain Amplifier**

Internal Clock Multiplier (PLL)
Clock Outputs
Voltage Regulator Controller
48-Lead LQFP Package

APPLICATIONS

Powerline Networking
Home Phone Networking
xDSL
Broadband Wireless
Home RF

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9875 is a single-supply broadband modem mixed-signal front end (MxFE) IC. The devices contain a transmit path Interpolation Filter and DAC, and a receive path PGA, LPF, and ADC supporting a variety of broadband modem applications. Also on chip is a PLL clock multiplier that provides all required clocks from a single crystal or clock input. The AD9875 provides 10-bit converter performance on both the Tx and Rx paths.

The TxDAC+ uses a selectable digital 2× or 4× interpolation low-pass or band-pass filter to further oversample transmit data and reduce the complexity of analog reconstruction filtering. The transmit path signal bandwidth can be as high as 26 MHz at an input data rate of 64 MSPS. The 10-bit DAC provides differential current outputs for optimum noise and distortion performance. The DAC full-scale current can be adjusted from 2 mA to 20 mA by a single resistor, providing 20 dB of additional gain range.

The receive path consists of a PGA, LPF, and ADC. The two-stage PGA has a gain range of –6 dB to +36 dB, and is programmable in 2 dB steps, adding 42 dB of dynamic range to the receive path.

The receive path LPF cutoff frequency can be programmed to either 12 MHz or 26 MHz. The filter cutoff frequency can also be tuned or bypassed where filter requirements differ. The 10-bit ADC uses a multistage differential pipeline architecture to achieve excellent dynamic performance with low power consumption.

The AD9875 provides a voltage regulator controller (VRC) that can be used with an external power MOSFET transistor to form a cost-effective 1.3 V linear regulator.

The digital transmit and receive ports are each multiplexed to a bus width of 5/6 bits and are clocked at a frequency of twice the 10-bit word rate.

The AD9875 ADC and/or DAC can also be used at higher sampling rates as high as 64 MSPS in a 5-bit resolution non-multiplexed mode.

The AD9875 is pin compatible with the 12-bit AD9876. Both are available in a space-saving 48-lead LQFP package. They are specified over the industrial (–40°C to +85°C) temperature range.

REV. A

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AD9875–SPECIFICATIONS (V_S = 3.3 V ± 10%, f_{OSCIN} = 32 MHz, f_{DAC} = 128 MHz, Gain = –6 dB, R_{SET} = 4.02 kΩ, 100 Ω DAC single-ended load, unless otherwise noted.)

Parameter	Temp	Test Level	Min	Typ	Max	Unit
OSC IN CHARACTERISTICS						
Frequency Range	Full	II	10		64	MHz
Duty Cycle	25°C	II	40	50	60	%
Input Capacitance	25°C	III		3		pF
Input Impedance	25°C	III		100		MΩ
CLOCK OUTPUT CHARACTERISTICS						
CLKA Jitter (f_{CLKA} Derived from PLL)	25°C	III		14		ps rms
CLKA Duty Cycle	25°C	III		50 ±5		%
CLKB Jitter (f_{CLKB} Derived from PLL)	25°C	III		33		ps rms
CLKB Duty Cycle	25°C	III		50 ±5		%
Tx CHARACTERISTICS						
Tx Path Latency, 4× Interpolation	Full	II		82		f_{DAC} Cycles
Interpolation Filter Bandwidth (–0.1 dB)						
4× Interpolation, LPF	Full	II		13		MHz
2× Interpolation, LPF	Full	II		26		MHz
TxDAC						
Resolution	Full	II		10		Bits
Conversion Rate	Full	II	10		128	MHz
Full-Scale Output Current	Full	II	2	10	20	mA
Voltage Compliance Range	Full	II	–0.5		+1.5	V
Gain Error	Full	II	–5	±2	+5	% FS
Output Offset	Full	II	0	7	19	µA
Differential Nonlinearity	25°C	III		0.5		LSB
Integral Nonlinearity	25°C	III			1	LSB
Output Capacitance	25°C	III		5		pF
Phase Noise @ 1 kHz Offset, 10 MHz Signal	25°C	III		–90		dBc/Hz
Signal-to-Noise and Distortion (SINAD)						
10 MHz Analog Out AD9875 (20 MHz BW)	Full	I	59	61		dB
Wideband SFDR (to Nyquist, 64 MHz Max)	25°C	III				
5 MHz Analog Out	25°C	III		78		dBc
10 MHz Analog Out	25°C	III		72		dBc
Narrowband SFDR (3 MHz Window)						
10 MHz Analog Out	25°C	III		80		dBc
IMD (f1 = 6.9 MHz, f2 = 7.1 MHz)	25°C	III		–76		dBFS
Rx PATH CHARACTERISTICS						
Resolution	Full	II		10		Bits
Conversion Rate	Full	II	7.5		55	MHz
Pipeline Delay, ADC Clock Cycles	Full	II		5.5		Cycles
DC Accuracy						
Differential Nonlinearity	25°C	II	–1.0	±0.25	+1.0	LSB
Integral Nonlinearity	25°C	II	–2.0	±0.5	+2.0	LSB
Dynamic Performance						
(A_{IN} = –0.5 dBFS, f = 5 MHz)						
@ f_{OSCIN} = 32 MHz						
Signal-to-Noise and Distortion Ratio (SINAD)	25°C	III		59.6		dB
Effective Number of Bits (ENOB)	25°C	III		9.5		Bits
Signal-to-Noise Ratio (SNR)	25°C	III		60		dB
Total Harmonic Distortion (THD)	25°C	III		–65		dB
Spurious Free Dynamic Range (SFDR)	25°C	III		68		dB
Dynamic Performance						
(A_{IN} = –0.5 dBFS, f = 10 MHz)						
@ $F_{PLLB/2}$ = 50 MHz						
Signal-to-Noise and Distortion Ratio (SINAD)	25°C	III		54		dB
Effective Number of Bits (ENOB)	25°C	III		8.6		Bits
Signal-to-Noise Ratio (SNR)	25°C	III		55		dB
Total Harmonic Distortion (THD)	25°C	III		–61		dB
Spurious Free Dynamic Range (SFDR)	25°C	III		68		dB

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Rx PATH GAIN/OFFSET						
Minimum Programmable Gain	25°C	III		–6		dB
Maximum Programmable Gain						
(12 MHz Filter)	25°C	III		36		dB
(26 MHz Filter)	25°C	III		30		dB
Gain Step Size	25°C	III		2		dB
Gain Step Accuracy	25°C	III		±0.4		dB
Gain Range Error	25°C	III		±1.0		dB
Offset Error, PGA Gain = 0 dB (AD9875)	25°C	III		±4.0		LSB
Absolute Gain Error, PGA Gain = 0 dB	25°C	III		±0.8		dB
Rx PATH INPUT CHARACTERISTICS						
Input Voltage Range	25°C	III		4		Vppd
Input Capacitance	25°C	III		4		pF
Differential Input Resistance	25°C	III		270		Ω
Input Bandwidth (–3 dB)	25°C	III		50		MHz
Input Referred Noise (at +36 dB Gain with Filter)	25°C	III		16		µV rms
Input Referred Noise (at –6 dB Gain with Filter)	25°C	III		684		µV rms
Common-Mode Rejection	25°C	III		40		dB
Rx PATH LPF (Low Cutoff Frequency)						
Cutoff Frequency	25°C	III		12		MHz
Cutoff Frequency Variation	25°C	III		±7		%
Attenuation @ 22 MHz	25°C	III		20		dB
Passband Ripple	25°C	III		±1.0		dB
Group Delay Variation	25°C	III		30		ns
Settling Time						
(to 1% FS, Min to Max Gain Change)	25°C	III		150		ns
Total Harmonic Distortion at Max Gain (THD)	25°C	III		–68		dBc
Rx PATH LPF (High Cutoff Frequency)						
Cutoff Frequency	25°C	III		26		MHz
Cutoff Frequency Variation	25°C	III		±7		%
Attenuation @ 44 MHz	25°C	III		20		dB
Passband Ripple	25°C	III		±1.2		dB
Group Delay Variation	25°C	III		15		ns
Settling Time						
(to 1% FS, Min to Max Gain Change)	25°C	III		80		ns
Total Harmonic Distortion at Max Gain (THD)	25°C	III		–65		dBc
Rx PATH DIGITAL HPF						
Latency (ADC Clock Source Cycles)	Full	II		1		Cycle
Roll-Off in Stopband	Full	II		6		dB/Octave
–3 dB Frequency	Full	II		f_{ADC}/400		Hz
Rx PATH DISTORTION PERFORMANCE						
IMD: f1 = 6.9 MHz, f2 = 7.1 MHz						
12 MHz Filter: 0 dB	25°C	III		–65		dBc
: 30 dB	25°C	III		–57		dBc
28 MHz Filter: 0 dB	25°C	III		–65		dBc
: 30 dB	25°C	III		–56		dBc
POWER-DOWN/DISABLE TIMING						
Power-Up Delay (Power-Down-to-Active)						
DAC	25°C	II			40	µs
PLL	25°C	II			10	µs
ADC	25°C	II			1000	µs
PGA	25°C	II			1	µs
LPF	25°C	II			1	µs
Interpolator	25°C	II			200	ns
VRC	25°C	II			2	µs
Minimum RESET Pulsewidth Low (t_{RL})	Full	III			5	f_{OSCIN} Cycle
DAC I_{OUT} Off after Tx QUIET Asserted	25°C	II			200	ns
DAC I_{OUT} On after Tx QUIET Deasserted	25°C	II			1	µs
Power-Down Delay (Active-to-Power-Down)						
DAC	25°C	II			400	ns
Interpolator	25°C	II			200	ns

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Tx PATH INTERFACE						
Maximum Input Nibble Rate, 2× Interpolation	Full	II	128			MHz
Tx-Set Up Time (t_{SU})	Full	II	3.0			ns
Tx-Hold Time (t_{HD})	Full	II	0			ns
Rx PATH INTERFACE						
Maximum Output Nibble Rate	Full	I	110			MHz
Rx-DataValid Time (t_{VT})	Full	II			3.0	ns
Rx-Data Hold Time (t_{HT})	Full	II	1.5			ns
CMOS LOGIC INPUTS						
Logic "1" Voltage	Full	II	V_{DRVDD} – 0.7			V
Logic "0" Voltage	Full	II			0.4	V
Logic "1" Current	Full	II			12	µA
Logic "0" Current	Full	II			12	µA
Input Capacitance	25°C	III		3		µF
CMOS LOGIC OUTPUTS (1 mA Load)						
Logic "1" Voltage	Full	II	V_{DRVDD} – 0.6			V
Logic "0" Voltage	Full	II			0.4	V
Digital Output Rise/Fall Time	Full	II	1.5		2.5	ns
POWER SUPPLY						
All Blocks Powered Up						
I_{S_TOTAL} (Total Supply Current)	Full	I		262	288	mA
I_{S_TOTAL} (Tx_QUIET Pin Asserted)	25°C	III		172		mA
Digital Supply Current (I_{DRVDD} + I_{DVDD})	25°C	III		77		mA
Analog Supply Current (I_{AVDD})	25°C	III		185		mA
Power Consumption of Functional Blocks						
Rx LPF	25°C	III		110		mA
ADC and FPGA	25°C	III		55		mA
Rx Reference	25°C	III		2		mA
Interpolator	25°C	III		33		mA
DAC	25°C	III		18		mA
PLL-B	25°C	III		8		mA
PLL-A	25°C	III		24		mA
Voltage Regulator Controller	25°C	III		1		mA
All Blocks Powered Down						
Supply Current I_S, f_{OSCIN} = 32 MHz	Full	II		19	22	mA
Supply Current I_S, f_{OSCIN} Idle	Full	II		10	12	mA
Power Supply Rejection						
Tx Path (ΔV_S = ±10%)	25°C	III		62		dB
Rx Path (ΔV_S = ±10%)	25°C	III		54		dB
SERIAL CONTROL BUS						
Maximum SCLK Frequency (f_{SCLK})	Full	II	25			MHz
Clock Pulsewidth High (t_{PWH})	Full	II	18			ns
Clock Pulsewidth Low (t_{PWL})	Full	II	18			ns
Clock Rise/Fall Time	Full	II			1	ms
Data/Chip-Select Setup Time (t_{DS})	Full	II	25			ns
Data Hold Time (t_{DH})	Full	II	0			ns
Data Valid Time (t_{DV})	Full	II			20	ns
RECEIVE-TO-TRANSMIT ISOLATION (10 MHz, Full-Scale Sinewave Output/Output)						
Isolation: Tx Path to Rx Path, Gain = +36 dB	25°C	III		–75		dB
Isolation: Rx Path to Tx Path, Gain = –6 dB	25°C	III		–70		dB
VOLTAGE REGULATOR CONTROLLER						
Output Voltage (V_{FB} with SI2301 Connected)	Full	I	1.25	1.30	1.35	V
Line Regulation ($\Delta V_{FB\%}/\Delta V_{DVDD\%} \times 100\%$)	25°C	III		100		%
Load Regulation ($\Delta V_{FB}/\Delta I_{LOAD}$)	25°C	III		60		mΩ
Maximum Load Current (I_{LOAD})	Full	II	250			mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Power Supply (V_S) . . . . . 3.9 V
Digital Output Current . . . . . 5 mA
Digital Inputs . . . . . –0.3 V to DRVDD 0.3 V
Analog Inputs . . . . . –0.3 V to AVDD 0.3 V
Operating Temperature . . . . . –40°C to +85°C
Maximum Junction Temperature . . . . . 150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . 300°C

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I – Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range (–40°C to +85°C).
II – Parameter is guaranteed by design and/or characterization testing.
III – Parameter is a typical value only.

THERMAL CHARACTERISTICS

Thermal Resistance
48-Lead LQFP
θ_{JA} = 57°C/W
θ_{JC} = 28°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9875BST	–40°C to +85°C	48-Lead LQFP	ST-48
AD9875-EB	–40°C to +85°C	Evaluation Board	
AD9875BSTRL	–40°C to +85°C	BST Reel	

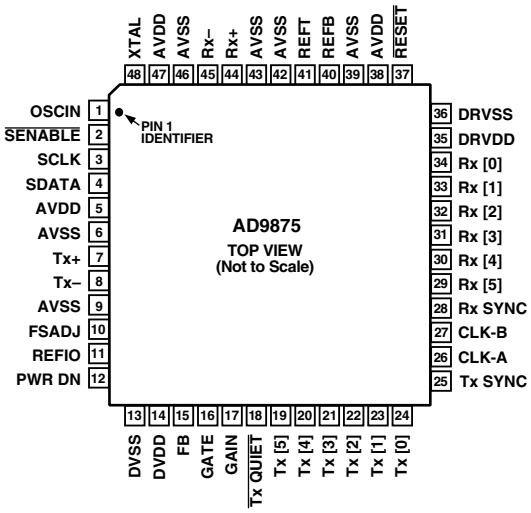
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9875 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin	Name	Function
1	OSCIN	Crystal Oscillator Inverter Input
2	$\overline{\text{SENABLE}}$	Serial Bus Enable Input
3	SCLK	Serial Bus Clock Input
4	SDATA	Serial Bus Data I/O
5, 38, 47	AVDD	Analog 3.3 V Power Supply
6, 9, 39, 42, 43, 46	AVSS	Analog Ground
7	Tx+	Transmit DAC+ Output
8	Tx–	Transmit DAC– Output
10	FSADJ	DAC Full-Scale Output Current Adjust with External Resistor
11	REFIO	DAC Bandgap Decoupling Node
12	PWR DN	Power-Down Input
13	DVSS	Digital Ground
14	DVDD	Digital 3.3 V Power Supply
15	FB	Regulator Feedback Input
16	GATE	Regulator Output to FET Gate
17	GAIN	Transmit Data Port (Tx[5:0]) Mode Select Input
18	$\overline{\text{Tx QUIET}}$	Transmit Quiet Input
19–24	Tx[5:0]	Transmit Data Input
25	Tx SYNC	Transmit Synchronization Strobe Input
26	CLK-A	$L \times f_{OSCIN}$ Clock Output
27	CLK-B	$M/N \times f_{OSCIN}$ Clock Output
28	Rx SYNC	Receive Data Synchronization Strobe Output
29–34	Rx[5:0]	Receive Data Output
35	DRVDD	Digital I/O 3.3 V Power Supply
36	DRVSS	Digital I/O Ground
37	$\overline{\text{RESET}}$	Reset Input
40	REFB	ADC Reference Decoupling Node
41	REFT	ADC Reference Decoupling Node
44	Rx+	Receive Path + Input
45	Rx–	Receive Path – Input
48	XTAL	Crystal Oscillator Inverter Output

PIN CONFIGURATION



DEFINITIONS OF SPECIFICATIONS

CLOCK JITTER

The clock jitter is a measure of the *intrinsic* jitter of the PLL generated clocks. It is a measure of the jitter from one rising and of the clock with respect to another edge of the clock nine cycles later.

DIFFERENTIAL NONLINEARITY ERROR (DNL, NO MISSING CODES)

An ideal converter exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 10-bit resolution indicates that all 1024 codes respectively, must be present over all operating ranges.

INTEGRAL NONLINEARITY ERROR (INL)

Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

PHASE NOISE

Single-sideband phase noise power density is specified relative to the carrier (dBc/Hz) at a given frequency offset (1 kHz) from the carrier. Phase noise can be measured directly on a generated single tone with a spectrum analyzer that supports noise marker measurements. It detects the relative power between the carrier and the offset (1 kHz) sideband noise and takes the resolution bandwidth (rbw) into account by subtracting 10 log(rbw). It also adds a correction factor that compensates for the implementation of the resolution bandwidth, log display and detector characteristic.

OUTPUT COMPLIANCE RANGE

The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation, resulting in nonlinear performance or breakdown.

SPURIOUS–FREE DYNAMIC RANGE (SFDR)

The difference, in dB, between the rms amplitude of the DACs output signal (or ADC's input signal) and the peak spurious signal over the specified bandwidth (Nyquist bandwidth unless otherwise noted).

PIPELINE DELAY (LATENCY)

The number of clock cycles between conversion initiation and the associated output data being made available.

OFFSET ERROR

First transition should occur for an analog value 1/2 LSB above negative full scale. Offset error is defined as the deviation of the actual transition from that point.

GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur for an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

INPUT REFERRED NOISE

The rms output noise is measured using histogram techniques. The ADC output codes' standard deviation is calculated in LSB, and converted to an equivalent voltage. This results in a noise figure that can be directly referred to the Rx input of the AD9875.

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)\ \text{dB}/6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

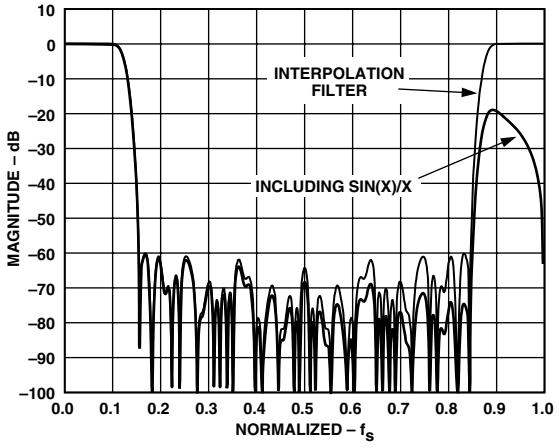
TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

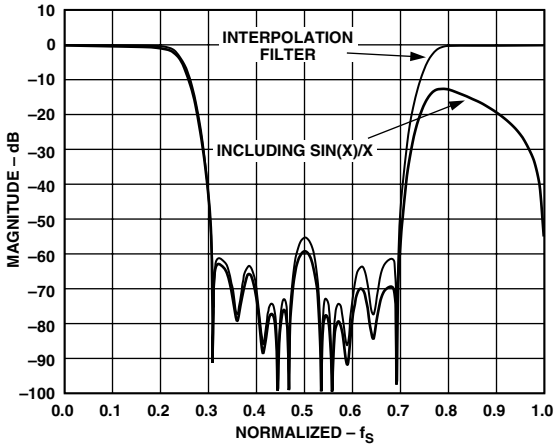
POWER SUPPLY REJECTION

Power Supply Rejection specifies the converters maximum full-scale change when the supplies are varied from nominal to minimum and maximum specified voltages.

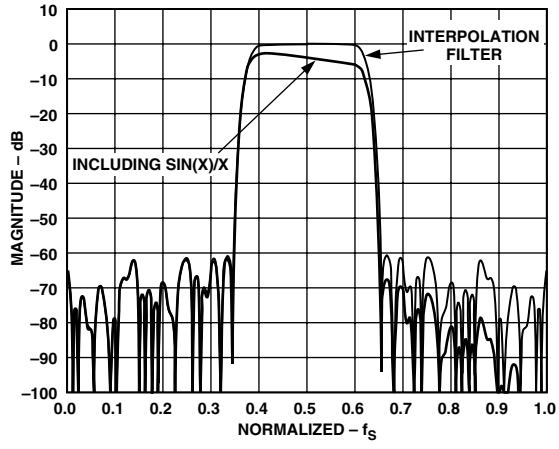
AD9875–Typical Tx Digital Filter Performance Characteristics



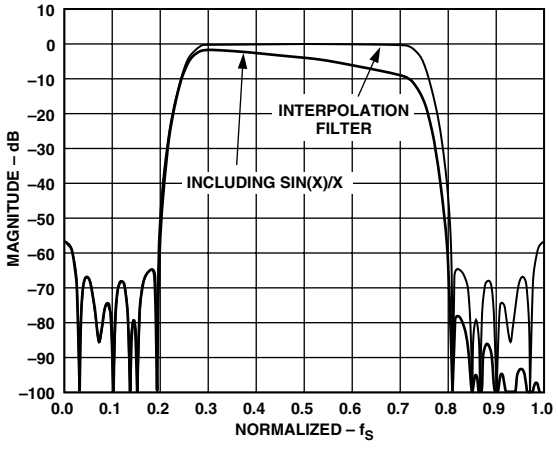
TPC 1. 4× Low-Pass Interpolation Filter



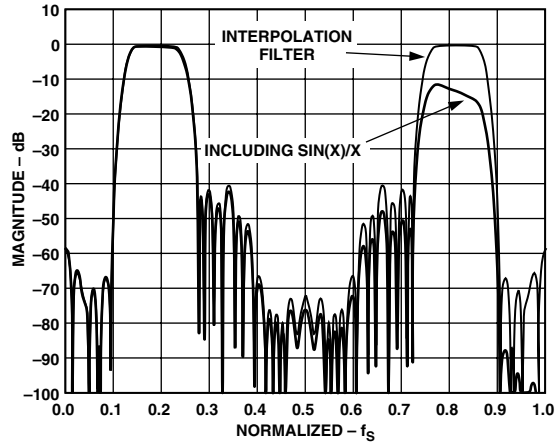
TPC 2. 2× Low-Pass Interpolation Filter



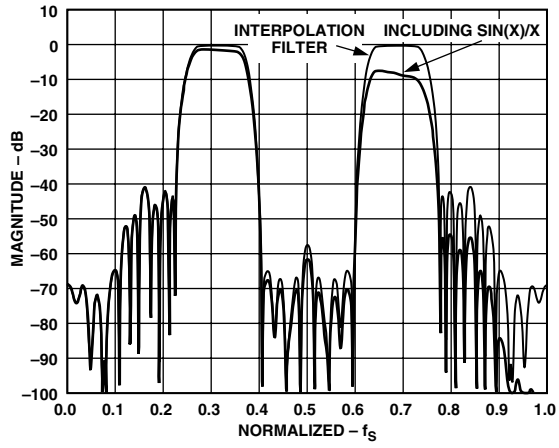
TPC 3. 4× Bandpass Interpolation Filter, $f_S/2$ Modulation, Adjacent Image Preserved



TPC 4. 2× Bandpass Interpolation Filter, $f_S/2$ Modulation, Adjacent Image Preserved

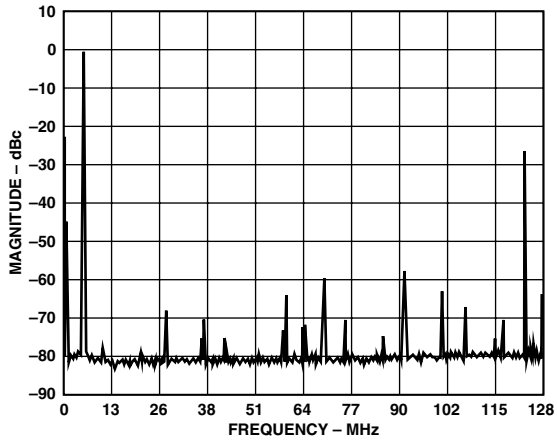


TPC 5. 4× Bandpass Interpolation Filter, $f_S/4$ Modulation, Lower Image Preserved

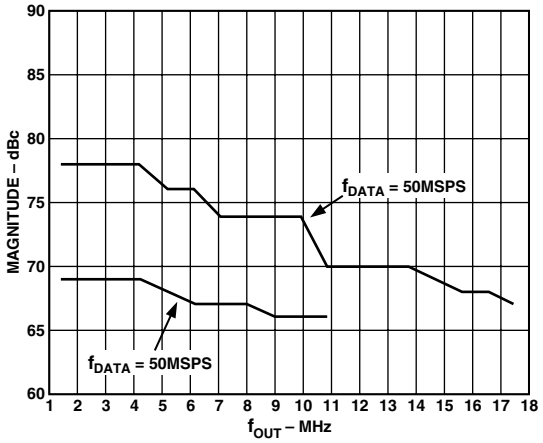


TPC 6. 4× Bandpass Interpolation Filter, $f_S/4$ Modulation, Upper Image Preserved

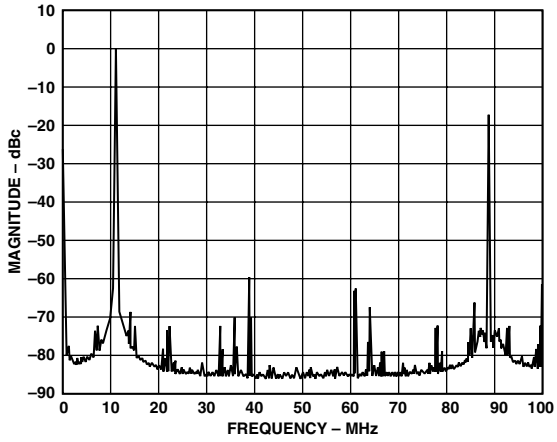
Typical AC Characteristics Curves for TxDAC (R_{SET} = 4.02 kΩ, R_{DAC} = 100 Ω)



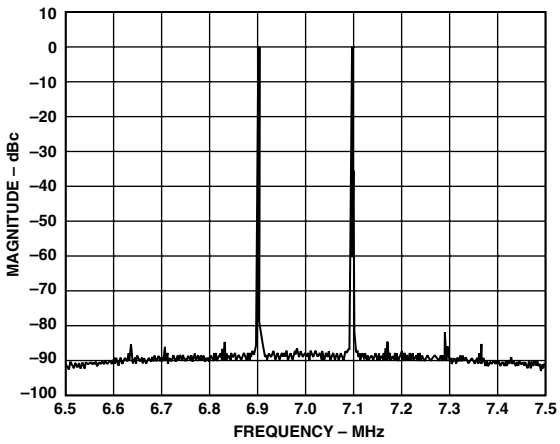
TPC 7. Single Tone Spectral Plot @ f_{DATA} = 32 MSPS, f_{OUT} = 5 MHz, 4× LPF



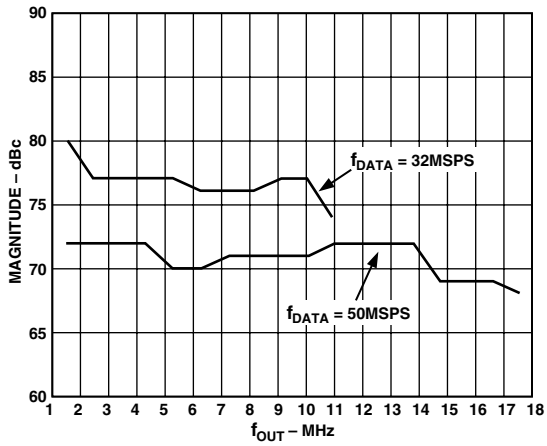
TPC 10. "Out of Band" SFDR vs. f_{OUT} @ f_{DATA} = 32 MSPS and 50 MSPS



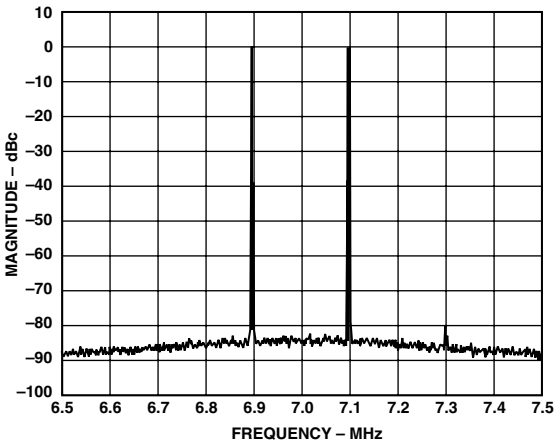
TPC 8. Single Tone Spectral Plot @ f_{DATA} = 50 MSPS, f_{OUT} = 11 MHz, 2× LPF



TPC 11. Dual Tone Spectral Plot @ f_{DATA} = 32 MSPS, f_{OUT} = 6.9 MHz and 7.1 MHz, 4× LPF

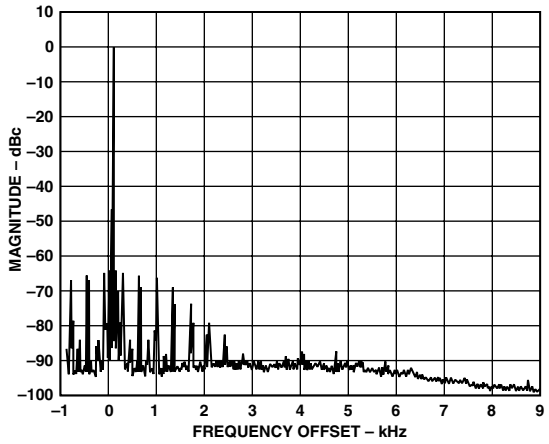


TPC 9. "In Band" SFDR vs. f_{OUT} @ f_{DATA} = 32 MSPS and 50 MSPS

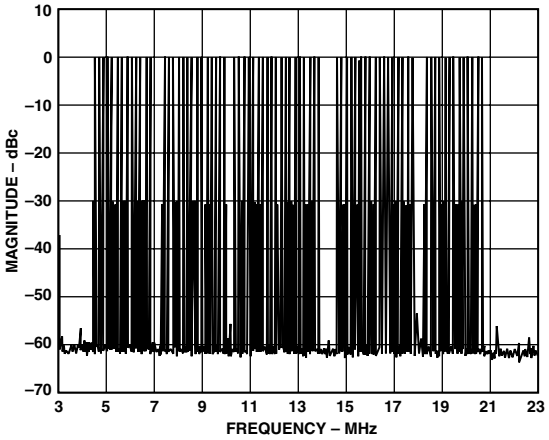


TPC 12. Dual Tone Spectral Plot @ f_{DATA} = 50 MSPS, f_{OUT} = 6.9 MHz and 7.1 MHz, 2× LPF

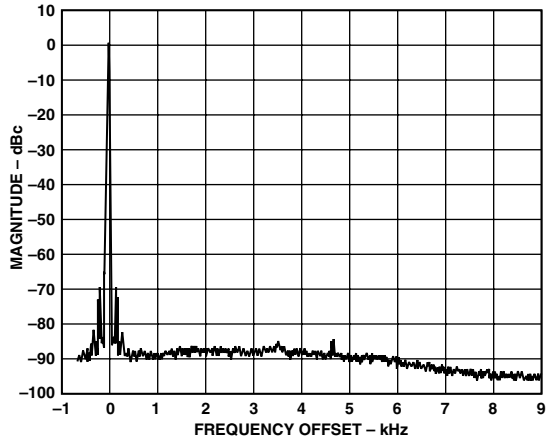
Typical AC Characteristics Curves for TxDAC (R_{SET} = 4.02 kΩ, R_{DAC} = 10.0 Ω)



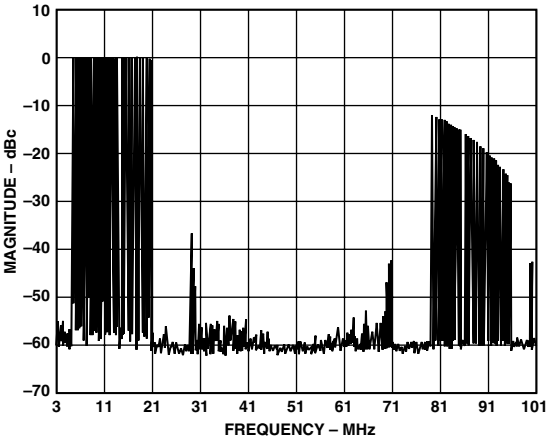
TPC 13. Phase Noise Plot @ f_{DATA} = 32 MSPS, f_{OUT} = 10 MHz, 4× LPF



TPC 15. "In Band" Multitone Spectral Plot @ f_{DATA} = 50 MSPS, f_{OUT} = k × 195 kHz, 2× LPF

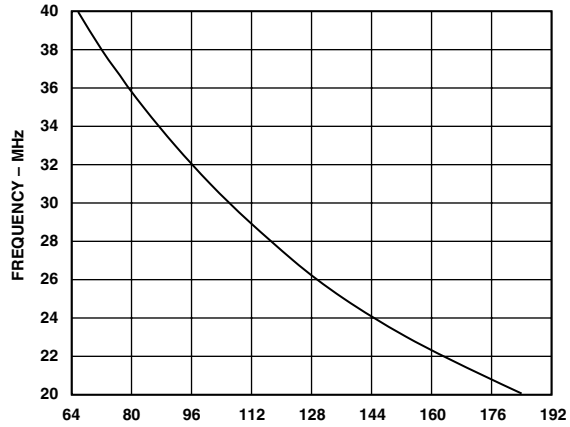


TPC 14. Phase Noise Plot @ f_{DATA} = 50 MSPS, f_{OUT} = 10 MHz, 2× LPF

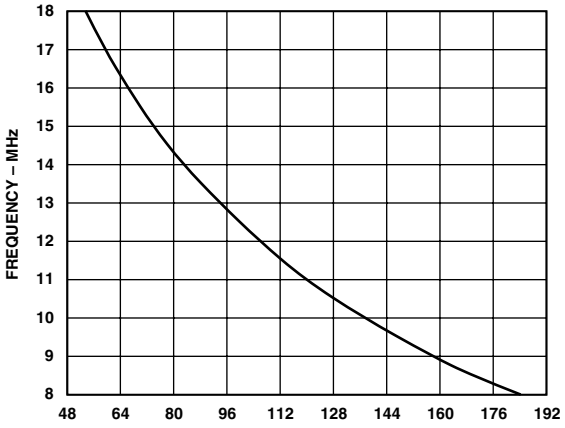


TPC 16. "Wide-Band" Multitone Spectral Plot @ f_{DATA} = 50 MSPS, f_{OUT} = k × 195 kHz, 2× LPF

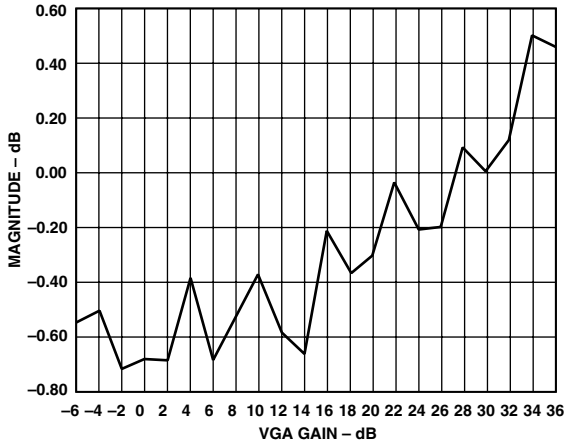
Typical AC Characterization Curves for Rx Path



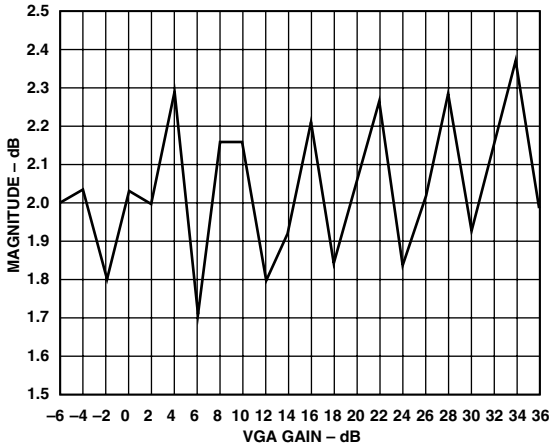
TPC 17. Rx vs. Tuning Target, f_{ADC} = 32 MHz, LPF with Wideband Rx LPF = 1



TPC 19. f_C vs. Tuning Target, f_{ADC} = 32 MHz, LPF with Wideband Rx LPF = 0

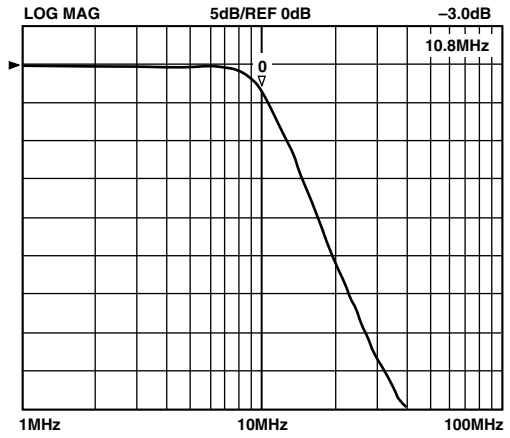


TPC 18. PGA Gain Error vs. Gain

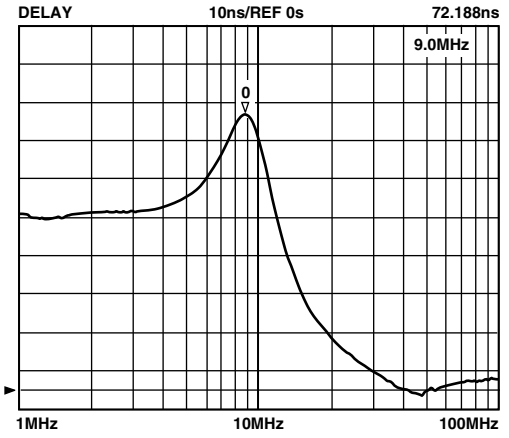


TPC 20. PGA Gain Step Size vs. Gain

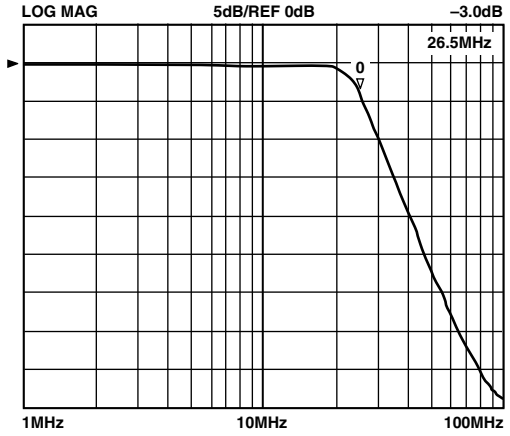
Typical AC Characterization Curves for Rx Path (f_{ADC} = 32 MHz)



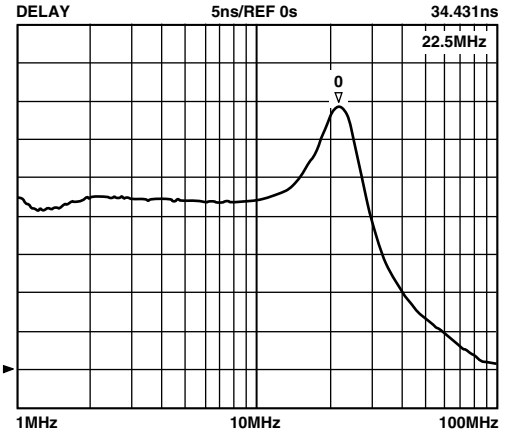
TPC 21. Rx LPF Frequency Response, Low f_C Nominal Tuning Targets



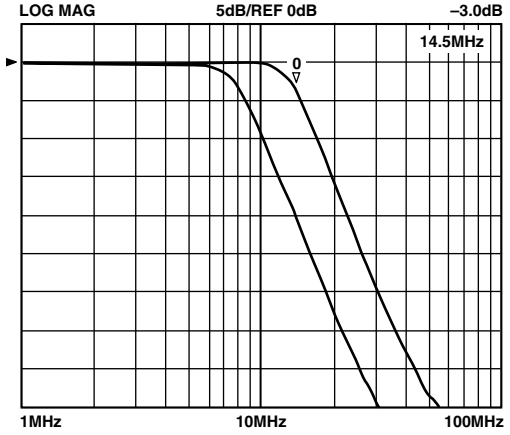
TPC 24. Rx LPF Group Delay, Low f_C Nominal Tuning Targets



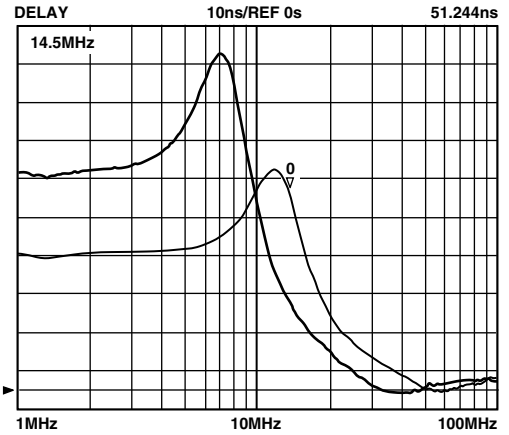
TPC 22. Rx LPF Frequency Response, High f_C Nominal Tuning Targets



TPC 25. Rx LPF Group Delay, High f_C, Nominal Tuning Targets

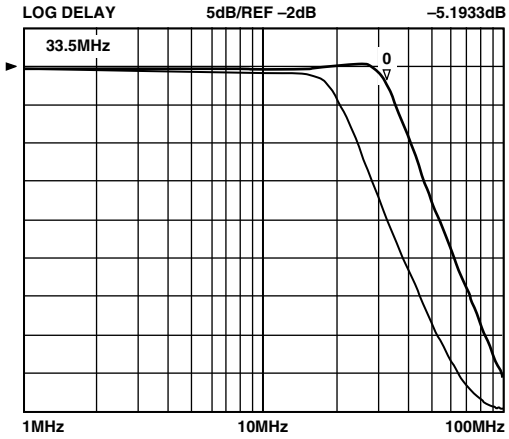


TPC 23. Rx LPF Frequency Response, Low f_C, 0 × 60 and 0 × 96 Tuning Targets

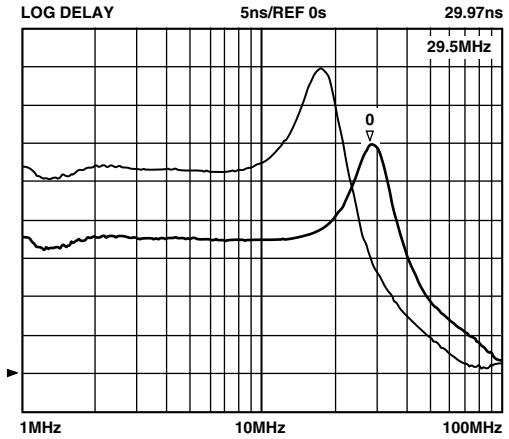


TPC 26. Rx LPF Group Delay, Low f_C, 0 × 60 and 0 × 96 Tuning Targets

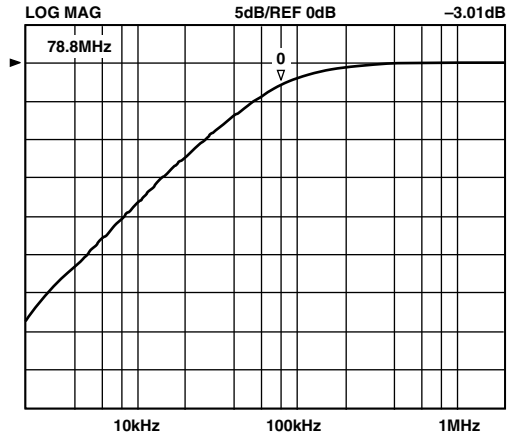
Typical AC Characterization Curves for Rx Path (f_{ADC} = 32 MHz)



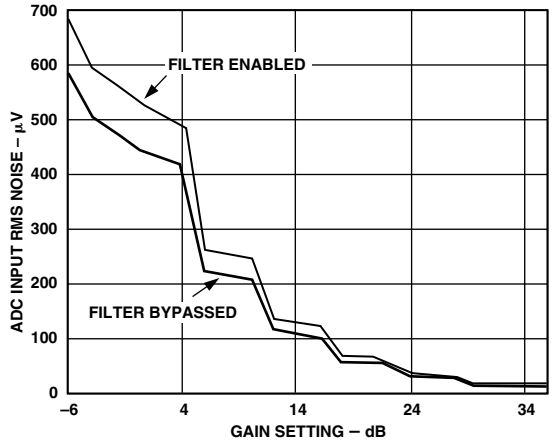
TPC 27. Rx LPF Frequency Response, High f_C, 0 × 60 and 0 × 96 Tuning Targets



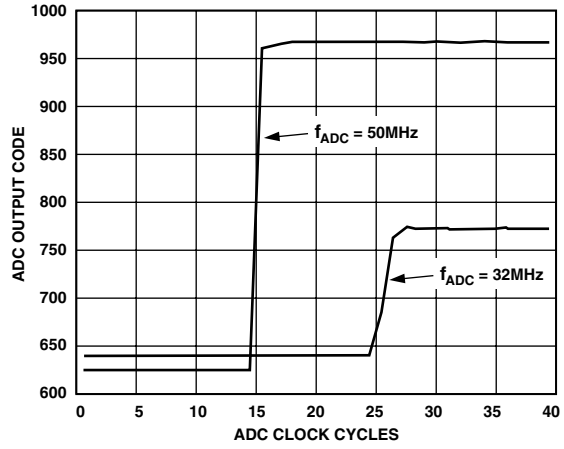
TPC 30. Rx LPF Group Delay, High f_C, 0 × 60 and 0 × 96 Tuning Targets



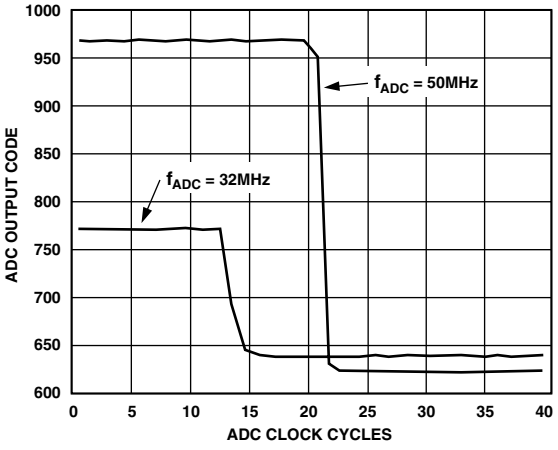
TPC 28. Rx HPF Frequency Response, f_{ADC} = 32 MHz



TPC 31. Rx Input Referred Noise vs. Gain @ f_{ADC} = 32 MSPS, f_{IN} = 1 MHz

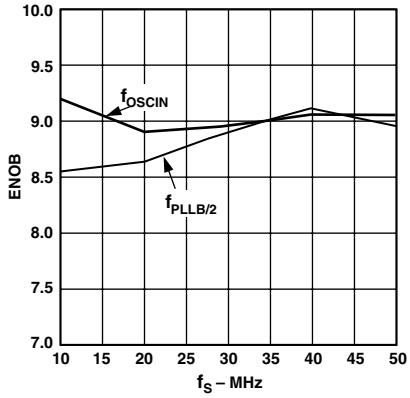


TPC 29. Rx Path Setting, 1/2 Scale Rising Step with Gain Change

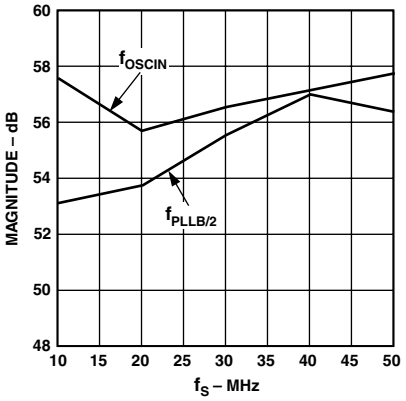


TPC 32. Rx Path Setting, 1/2 Scale Falling Step with Gain Change

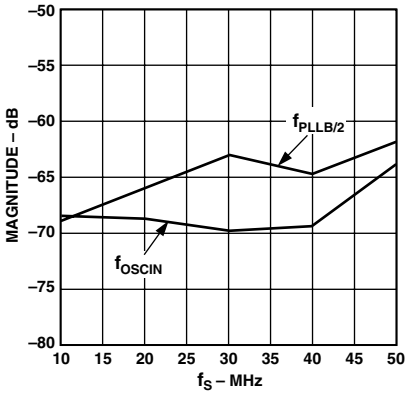
Typical AC Characterization Curves for Rx Path (Gain = –6 dB, f_{IN} = 5 MHz)



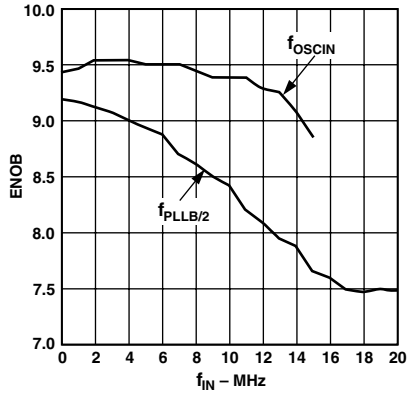
TPC 33. Rx Path ENOB vs. f_{ADC}



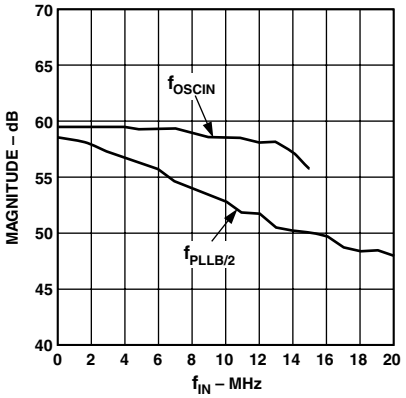
TPC 34. Rx Path SNR vs. f_{ADC}



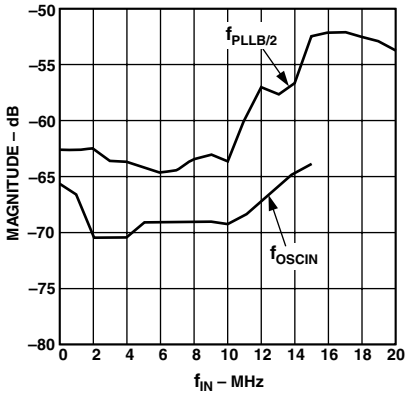
TPC 35. Rx Path THD vs. f_{ADC}



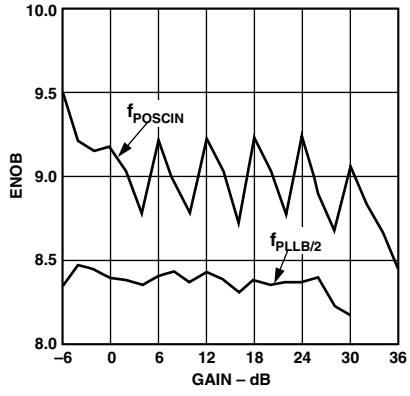
TPC 36. Rx Path ENOB vs. f_{IN}



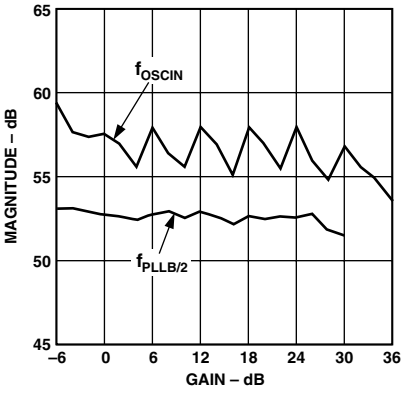
TPX 37. Rx Path SNR vs. f_{IN}



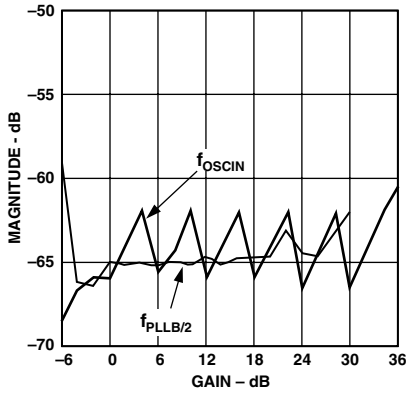
TPC 38. Rx Path THD vs. f_{IN}



TPC 39. Rx Path ENOB vs. Gain



TPC 40. Rx Path SNR vs. Gain



TPC 41. Rx Path THD vs. Gain

TRANSMIT PATH

The AD9875 transmit path consists of a Digital Interface Port, a Programmable Interpolation Filter, and a Transmit DAC. All clock signals required by these blocks are generated from the f_{OSCIN} signal by the PLL-A clock generator. The block diagram below shows the interconnection between the major functional components of the transmit path.

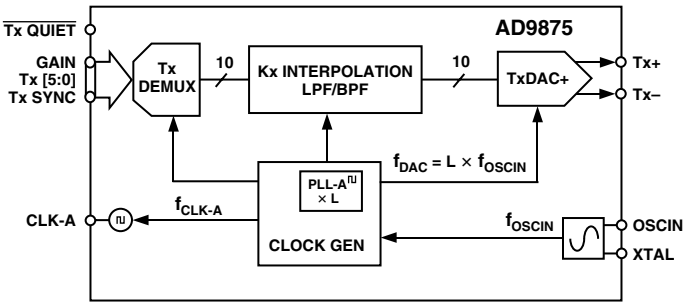


Figure 1. Transmit Path Block Diagram

Digital Interface Port

The transmit Digital Interface Port has several modes of operation. In its default configuration, the Tx Port accepts six bit nibbles through the Tx[5:0] and TxSYNC pins and demultiplexes the data into 12-bit words before passing it to the Interpolation Filter. The input data is sampled on the rising edge of f_{CLK-A}.

Additional programming options for the Tx Port allow; sampling the input data on the falling edge of f_{CLK-A}, inversion or disabling of f_{CLK-A}, reversing the order of the nibbles, and inputting nibble widths of 5 bits/5 bits. Also, the Tx Port interface can be controlled by the GAIN pin to provide direct access to the Rx Path Gain Adjust register. All of these modes are fully described in the Register Programming Definitions section of this data sheet.

The data format is two's complement, as shown below:

011 . . 11: Maximum

000 . . 01: Midscale + 1 LSB
000 . . 00: Midscale
111 . . 11: Midscale – 1 LSB
111 . . 10: Midscale – 2 LSB

100 . . 00: Minimum

The data can be translated to straight binary data format by simply inverting the most significant bit.

The timing of the interface is fully described in the Transmit Timing section of this data sheet.

PLL-A Clock Distribution

Figure 1 shows the clock signals used in the transmit path. The DAC sampling clock, f_{DAC}, is generated by DPLL-A. f_{DAC} has a frequency equal to $L \times f_{OSCIN}$, where f_{OSCIN} is the internal signal generated either by the crystal oscillator when a crystal is connected between the OSCIN and XTAL pins, or by the clock that is fed into the OSCIN pin, and L is the multiplier programmed through the serial port. L can have the values of 1, 2, 4, or 8.

The transmit path expects a new half-word of data at the rate of f_{CLK-A}. When the Tx multiplexer is enabled, the frequency of the Tx port is:

$$f_{CLK-A} = 2 \times f_{DAC}/K = 2 \times L \times f_{OSCIN}/K$$

where K is the interpolation factor that can be programmed to be 1, 2, or 4.

When the Tx multiplexer is disabled, the frequency of the Tx port is:

$$f_{CLK-A} = f_{DAC}/K = L \times f_{OSCIN}/K$$

Interpolation Filter

The interpolation filter can be programmed to run at 2× and 4× upsampling ratios in each of three different modes. The transfer functions of these six configurations are shown in TPCs 1–6. The X-axis of each of these figures corresponds to the frequency normalized to f_{DAC}. These transfer functions show both the discrete time transfer function of the interpolation filters alone and with the SIN(x)/x transfer function of the DAC. The Interpolation Filter can also be programmed into a pass-through mode if no interpolation filtering is desired.

The contents of the interpolation filters are not cleared by hardware or software resets. It is recommended to "flush" the transmit data path with zeros before transmitting data.

Table I contains the following parameters as a function of the mode that it is programmed:

Latency – the number of clock cycles from the time a digital impulse is written to the DAC until the peak value is output at the Tx± pins.

Flush – the number of clock cycles from the time a digital impulse is written to the DAC until the output at the Tx± pins settles to zero.

f_{LOWER} *(0.1 dB, 3 dB)* – This indicates the lower 0.1 dB or 3 dB cutoff frequency of the interpolation filter as a fraction of f_{DAC}, the DAC sampling frequency.

f_{UPPER} *(0.1 dB, 3 dB)* – This indicates the upper 0.1 dB or 3 dB cutoff frequency of the interpolation filter as a fraction of f_{DAC}, the DAC sampling frequency.

Table I. Interpolation Filter Parameters vs. Mode

Register 7[7:4]	0 × 0	0 × 1	0 × 4	0 × 5	0 × 8	0 × C
Mode	4 × LPF	2 × LPF	4 × BPF Adj.	2 × BPF Adj.	4 × BPF Lower	4 × BPF Upper
Latency, f_{DAC} Clock Cycles	86	30	86	30	86	86
Flush, f_{DAC} Clock Cycles	128	48	128	48	142	142
f_{LOWER}, 0.1 dB	0	0	0.398	0.276	0.148/ 0.774	0.274/ 0.648
f_{UPPER}, 0.1 dB	0.102	0.204	0.602	0.724	0.226/ 0.852	0.352/ 0.762
f_{LOWER}, 3 dB	0	0	0.381	0.262	0.131/ 0.757	0.257/ 0.631
f_{UPPER}, 3 dB	0.119	0.238	0.619	0.738	0.243/ 0.869	0.369/ 0.743

D/A Converter

The AD9875 DAC provides differential output current on the Tx+ and Tx– pins. The value of the output currents are complimentary, meaning that they will always sum to I_{FS}, the full-scale current of the DAC. For example, when the current from Tx+ is at full-scale, the current from Tx– is zero. The two currents will

typically drive a resistive load which will convert the output currents to a voltage. The Tx+ and Tx– output currents are inherently ground seeking and should each be connected to matching resistors, R_L, that are tied directly to AGND.

The full-scale output current of the DAC is set by the value of the resistor placed from the FSADJ pin to AGND. The relationship between the resistor, R_{SET}, and the full-scale output current is governed by the following equation:

$$I_{FS} = 39.4/R_{SET}$$

The full-scale current can be set from 2 mA to 20 mA. Generally, there is a trade-off between DAC performance and power consumption. The best DAC performance will be realized at an I_{FS} of 20 mA. However, the value of I_{FS} adds directly to the overall current consumption of the device.

The single-ended voltage output appearing at the *Tx+* and *Tx–* nodes are:

$$V_{TX+} = I_{TX+} \times R_L$$

$$V_{TX-} = I_{TX-} \times R_L$$

Note that the full-scale voltage of V_{Tx+} and V_{Tx-} should not exceed the maximum output compliance range of 1.5 V to prevent signal compression. To maintain optimum distortion and linearity performance, the maximum voltages at V_{Tx+} and V_{Tx-} should not exceed 0.5 V.

The single ended full-scale voltage at either output node will be:

$$V_{FS} = I_{FS} \times R_L$$

The differential voltage, V_{DIFF}, appearing across V_{Tx+} and V_{Tx-} is:

$$V_{DIFF} = \left(I_{TX+} - I_{TX-}\right) \times R_L$$

and

$$V_{DIFF\_FS} = I_{FS} \times R_L$$

For optimum performance, a differential output interface is recommended since any common-mode noise or distortion can be suppressed.

It should be noted that the differential output impedance of the DAC is $2 \times R_L$ and any load connected across the two output resistors will load down the output voltage accordingly.

RECEIVE PATH DESCRIPTION

The receive path consists of a two-stage PGA, a continuous time, 4-pole LPF, an ADC, a digital HPF and a digital data multiplexer. Also working in conjunction with the receive path is an offset correction circuit and a digital phase lock loop. Each of these blocks will be discussed in detail in the following sections.

Programmable Gain Amplifier

The PGA has a programmable gain range from –6 dB to +36 dB if the narrower (approximately 12 MHz) LPF bandwidth is selected, or if the LPF is bypassed. If the wider (approximately 26 MHz) LPF bandwidth is selected, the gain range is –6 dB to +30 dB. The PGA is comprised of two sections, a Continuous Time PGA (CPGA) and a Switched Capacitor PGA (SPGA). The CPGA has possible gain settings of –6, 0, 6, 12, 18, and 24. The SPGA has possible gain settings of 0, 2, 4, 6, 8, 10, and 12 dB. Table I shows how the gain is distributed for each programmed gain setting.

The CPGA input appears at the device Rx+ and Rx– input pins. The input impedance of this stage is nominally 270 Ω differential and is not gain dependent. It is best to ac-couple the input signal to this stage and let the inputs self bias. This will lower the offset voltage of the input signal, which is important at higher gains, as any offset will lower the output compliance range of the CPGA output. When the inputs are driven by direct coupling, the dc level should be AVDD/2. However, this could lead to larger dc offsets and consequently reduce the dynamic range of the Rx path.

Low-Pass Filter

The Low-Pass Filter (LPF) is a programmable, multistage, fourth order low-pass filter comprised of two real poles and a complex pole pair. The first real pole is implemented within the CPGA. The second filter stage implements a complex pair of poles. The last real pole is implemented in a buffer stage that drives the SPGA.

There are two passband settings for the LPF. Within each passband the filters are tunable over about a ±30% frequency range. The formula for the cutoff frequency is:

$$f_{CUTOFF\ LOW} = f_{ADC} \times 64/\left(64 + Target\right)$$

$$f_{CUTOFF\ HIGH} = f_{ADC} \times 158/\left(64 + Target\right)$$

Where *Target* is the decimal value programmed as the tuning target in Register 5.

This filter may also be bypassed by setting Bit 0 of Register 4. In this case, the bandwidth of the Rx path will decrease with increasing gain and be approximately 50 MHz at the highest gain settings.

ADC

The AD9875's analog-to-digital converter implements a pipelined multistage architecture to achieve high sample rates while consuming low power. The ADC distributes the conversion over several smaller A/D subblocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage. As a consequence of the distributed conversion, ADCs require a small fraction of the 2^N comparators used in a traditional n-bit flash-type A/D. A sample-and-hold function within each of the stages permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Each stage of the pipeline, excluding the last, consists of a low resolution flash A/D connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier amplifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each one of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash A/D.

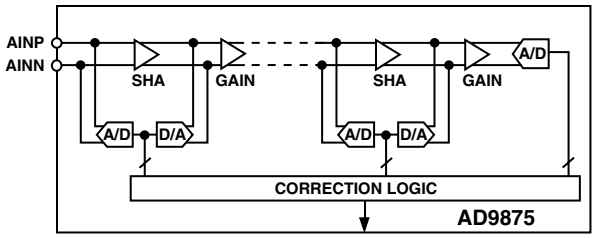


Figure 2. ADC Theory of Operation

The digital data outputs of the ADC are represented in two's complement format. They saturate to full-scale or zero when the input signal exceeds the input voltage range.

The two's complement data format is shown below:

011 . . 11: Maximum

000 . . 01: Midscale + 1 LSB
000 . . 00: Midscale
111 . . 11: Midscale – 1 LSB
111 . . 10: Midscale – 2 LSB

100 . . 00: Minimum

The Maximum value will be output from the ADC when the Rx+ input is 1V or more greater than the Rx– input. The Minimum value will be output from the ADC when the Rx– input is 1 V or more greater than the Rx+ input. This results in a full-scale ADC voltage of 2 Vppd.

The data can be translated to straight binary data format by simply inverting the most significant bit.

The best ADC performance will be achieved when the ADC clock source is selected from f_{OSCIN} and f_{OSCIN} is provided from a low jitter clock source. The amount of degradation from jitter on the ADC clock will depend on how quickly the input is varying at the sampling instance. TPC 36 charts this effect in the form of ENOB vs. input frequency for the two clocking scenarios.

The maximum sample rate of the ADC in full-precision mode, that is outputting 10 bits, is 55 MSPS. TPC 33 shows the ADC performance in ENOB vs. f_{ADCCLK}. The maximum sample rate of the ADC in half-precision mode, that is outputting five bits, is 64 MSPS. The timing of the interface is fully described in the Receive Timing section of this data sheet.

Digital HPF

Following the ADC there is a bypassable digital HPF. The response is a single pole IIR HPF. The transfer function is approximately:

$$H(z) = (Z - 0.99994)/(Z - 0.98466)$$

Where the sampling period is equal to the ADC clock period. This results in a 3 dB frequency approximately 1/400th of the ADC sampling rate. The transfer functions are plotted for 32 MSPS and 50 MSPS in TPC 31 and TPC 32.

The digital HPF introduces a 1 ADC clock cycle latency. If the HPF function is not desired, the HPF can be bypassed and the latency will not be incurred.

Clock and Oscillator Circuitry

The AD9875's internal oscillator generates all sampling clocks from a fundamental frequency quartz crystal. Figure 3a shows how the quartz crystal is connected between OSCIN (Pin 1) and XTAL (Pin 48) with parallel resonant load capacitors as specified by the crystal manufacturer. The internal oscillator circuitry can also be overdriven by a TTL level clock applied to OSCIN with XTAL left unconnected.

The PLL has a frequency capture range between 10 MHz and 64 MHz.

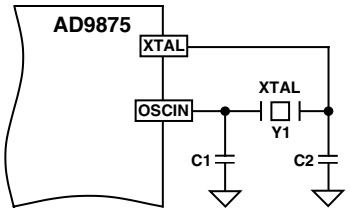


Figure 3a. Connections for Fundamental Mode Crystal

VOLTAGE REGULATOR CONTROLLER

The AD9875 contains an on-chip voltage regulator controller (VRC) for providing a linear 1.3 V supply for low voltage digital circuitry or other external use. The VRC consists of an op amp and a resistive voltage divider. As shown in Figure 3b, the resistive divider establishes a voltage of 1.3 V at the inverting input of the amplifier when DVDD is equal to its nominal voltage of 3.3 V. The feedback loop around the op amp will adjust the gate voltage such that the voltage at the FB pin, V_{FB}, will be equal to the voltage at the inverting input of the op amp.

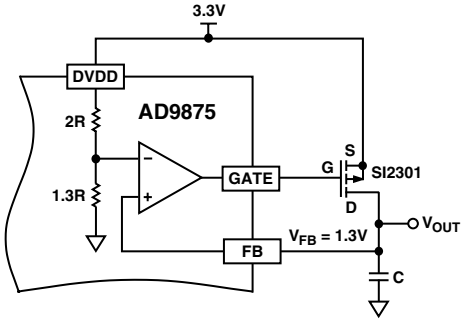


Figure 3b. Connections for a 1.3 V Linear Regulator

The maximum current output from the circuit is largely dependent on the MOSFET device. For the SI2301 shown, 250 mA can be delivered. The regulated output voltage should have bulk decoupling and high frequency decoupling capacitors to ground as required by the load. The regulator circuit will be stable for capacitive loads between 0.1 µF and 47 µF.

It should be noted that the regulated output voltage, V_{FB}, is proportional to DVDD. Therefore, the percentage variation in DVDD will also be seen at the regulated output voltage. The load regulation is roughly equal to the on resistance of the MOSFET device chosen. For the SI2301, this is about 60 mΩ.

AGC TIMING CONSIDERATIONS

When implementing the AGC timing loop it is important to consider the delay and settling time of the Rx path in response to a change in gain. Figure 4 shows the delay the receive signal experiences through the blocks of the Rx path. Whether the gain is programmed through the serial port or over the TX[5:0] pins, the gain takes effect immediately with the delays shown below. When gain changes do not involve the CPGA, the new gain will be evident in samples after seven ADC clock cycles. When the gain change does involve the CPGA, it takes an additional 45 ns to 70 ns due to the propagation delays of the buffer, LPF and PGA. Table III, in the Register Programming section, details the PGA programming map.

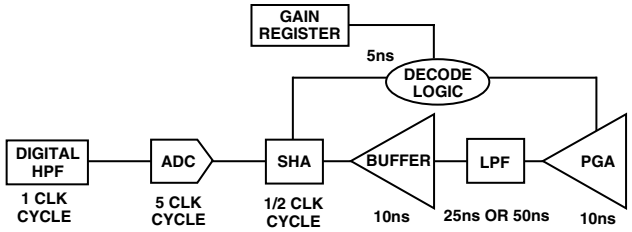


Figure 4. AGC Timing

Transmit Port Timing

The AD9875 transmit port consists of a 6-bit data bus Tx[5:0], a clock and a Tx SYNC signal. Two consecutive nibbles of the Tx data are multiplexed together to form a 10-bit data word. The clock appearing on the CLK-A pin is a buffered version of the internal Tx data sampling clock. Data from the Tx port is read on the rising edge of this sampling clock. The Tx SYNC signal is used to indicate to which word a nibble belongs. The first nibble of every word is read while Tx SYNC is low, the second nibble of that same word is read on the following Tx SYNC high level. The timing is illustrated in the Figure 5.

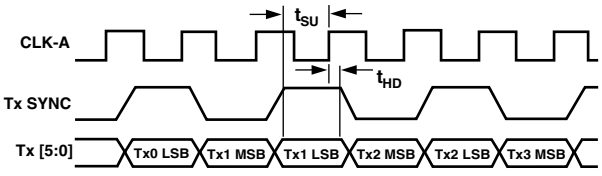


Figure 5. Transmit Timing Diagram AD9875

The Tx port is highly configurable and offers the following options:

Negative edge sampling can be chosen by two different methods; either by setting the *Tx Port Negative Edge Sampling* bit (Register 3, Bit 7) or the *Invert CLK-A* bit (Register 8, Bit 6). The main difference between the two methods is that setting Register 3, Bit 7 inverts the internal sampling clock and will affect only the transmit path, even if CLK–A is used to clock the Rx data. Inverting CLK-A would affect both the Rx and Tx paths if they both use CLK-A.

The first nibble of each word can be read in as the least significant nibble by setting the *Tx LS Nibble First* bit (Register 7, Bit 2).

For the AD9875, the most significant nibble defaults to six bits and the least significant nibble defaults to form four bits. This can be changed so that the least significant nibble and most significant nibble have five bits each. This is done by setting the *Tx Port Width Five Bits* bit (Register 7, Bit 1). In all cases, the nibbles are justified toward Bit 5.

Also, the Tx path can be used in a reduced resolution mode by setting the *Tx Port Multiplexer Bypass* bit (Register 7, Bit 0). In this mode the Tx data word becomes six bits and is read in a single cycle. The clocking modes are the same as described above, but the level of Tx SYNC is irrelevant.

If Tx SYNC is low for more than one clock cycle, the last transmit data will read continuously until Tx SYNC is brought high for the second nibble of a new transmit word. This feature can be used to "flush" the interpolator filters with zeros.

PGA Gain Adjust Timing

In addition to the serial port, the Tx[5:1] pins can be used to write to the Rx Path Gain Adjust bits (Register 6, Bits 4:0). This provides a faster way to update the PGA gain. A high level on the GAIN pin with Tx SYNC low programs the PGA setting on the rising edge of CLK-A. A low level on the GAIN pin enables data to be fed to the interpolator and DAC. The GAIN pin must be held high, the Tx SYNC must be held low, and the GAIN data must be stable for three clock cycles to successfully update the PGA GAIN value.

It should be noted that Tx SYNC must be held low and Tx GAIN must be held high to update the gain register. If Tx GAIN and Tx SYNC are both high, no data is written to the gain register of the Tx data path.

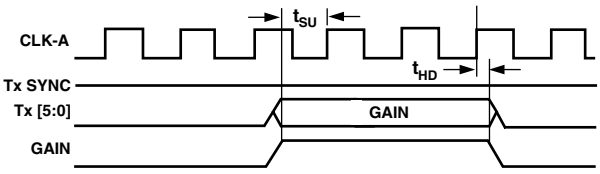


Figure 6. GAIN Programming

Receive Port Timing

The AD9875 receives port consists of a six bit data bus Rx[5:0], a clock and an Rx SYNC signal. Two consecutive nibbles of the Rx data are multiplexed together to form a 10-bit data word. The Rx data is valid on the rising edge of CLK-A when the *ADC Clock Source PLL-B/2* bit (Register 3, Bit 6) is set to 0. The Rx SYNC signal is used to indicate to which word a nibble belongs. The first nibble of every word is transmitted while Rx SYNC is low, the second nibble of that same word is transmitted on the following Rx SYNC high level. When Rx SYNC is low, the sampled nibble is read as the most significant nibble. When the Rx SYNC is high, the sampled nibble is read as the least significant nibble. The timing is illustrated in Figure 7.

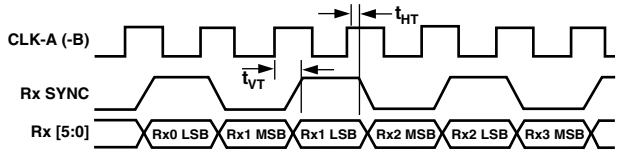


Figure 7. Receive Timing Diagram

The Rx port is highly configurable and offers the following options:

Negative edge sampling can be chosen by setting the *Invert CLK-A* bit (Register 8, Bit 6) or the *Invert CLK-B* bit (Register 8, Bit 7), depending on the clock selected as the ADC sampling source. Inverting CLK-A would affect the Tx sampling edge as well as the Rx sampling edge.

The first nibble of each word can be read in as the least significant nibble by setting the *Rx LS Nibble First* bit (Register 8, Bit 2).

For the AD9875, the most significant nibble defaults to six bits and the least significant nibble defaults to four bits. This can be changed so that the least significant nibble and most significant nibble have five bits each. This is done by setting the *Rx Port Width Five Bits* bit (Register 8, Bit 1). In all cases, the nibbles are justified toward Bit 5.

Also, the Rx path can be used in a reduced resolution mode by setting the *Rx Port Multiplexer Bypass* bit (Register 8, Bit 0). In this mode the Rx data word becomes six bits and is read in a single cycle. The clocking modes are the same as described above, but the level of Rx SYNC will stay low.

The Rx[5:0] pins can be put into a high impedance state by setting the *Three-State Rx Port* bit (Register 8, Bit 3).

SERIAL INTERFACE FOR REGISTER CONTROL

The serial port is a three wire serial communications port consisting of a clock (SCLK), chip select ($\overline{\text{SENABLE}}$), and a bidirectional data (SDATA) signal. The interface allows read/write access to all registers that configure the AD9875 internal parameters. Single or multiple byte transfers are supported as well as MSB first or LSB first transfer formats.

General Operation of the Serial Interface

Serial communication over the serial interface can be from 1 to 5 bytes in length. The first byte is always the instruction byte. The instruction byte establishes whether the communication is going to be a read or write access, the number of data bytes to be transferred and the address of the first register to be accessed. The instruction byte transfer is complete immediately upon the eighth rising edge of SCLK after $\overline{\text{SENABLE}}$ is asserted. Likewise, the data registers change *immediately* upon writing to the eighth bit of each data byte.

Instruction Byte

The instruction byte contains the following information as shown below:

Table II. Instruction Byte Information

MSB							LSB
I7	I6	I5	I4	I3	I2	I1	I0
R/W	N1	N0	A4	A3	A2	A1	A0

Bit I7 – R/W

This bit determines whether a read or a write data transfer will occur after the instruction byte write. Logic high indicates read operation; logic zero indicates a write operation.

Bits I6:I5 – N1:N0

These two bits determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in the table below:

Table III. Decode Bits

N1:N0	Description
0:0	Transfer 1 Byte
0:1	Transfer 2 Bytes
1:0	Transfer 3 Bytes
1:1	Transfer 4 Bytes

Bits I4:I0 – A4:A0

These bits determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9875.

SERIAL INTERFACE PORT PIN DESCRIPTION

SCLK—Serial Clock

The serial clock pin is used to synchronize data transfers to and from the AD9875 and to run the internal state machines. SCLK maximum frequency is 25 MHz. All data transmitted to the AD9875 is sampled on the rising edge of SCLK. All data read from the AD9875 is validated on the rising edge of SCLK and is updated on the falling edge.

$\overline{\text{SENABLE}}$—Serial Interface Enable

The $\overline{\text{SENABLE}}$ pin is active low. It enables the serial communication to the device. $\overline{\text{SENABLE}}$ select should stay low during the entire communication cycle. All input on the serial port is ignored when $\overline{\text{SENABLE}}$ is inactive.

SDATA—Serial Data I/O

The signal on this line is sampled on the first eight rising edges of SCLK after $\overline{\text{SENABLE}}$ goes active. Data is then read from or written to the AD9875 depending on what was read.

Figures 8 and 9 show the timing relationships between the three SPI signals.

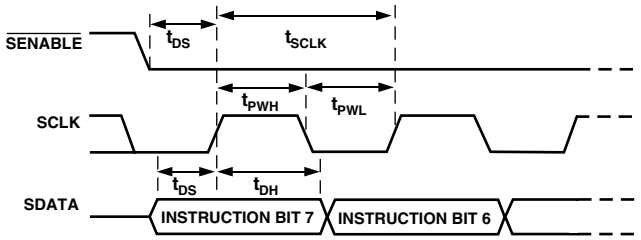


Figure 8. Timing Diagram Register Write to AD9875/AD9876

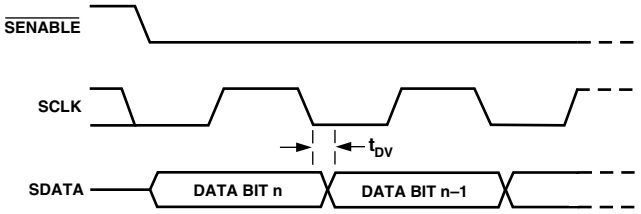


Figure 9. Timing Diagram Register Read from AD9875/AD9876

MSB/LSB TRANSFERS

The AD9875 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. The bit order is controlled by the *SPI LSB First* bit (Register 0, Bit 6). The default is value is 0, MSB first. Multibyte data transfers in MSB format can be completed by writing an instruction byte that includes the register address of the last address to be accessed. The AD9875 will automatically decrement the address for each successive byte required for the multibyte communication cycle.

When the *SPI LSB First* bit (Register 0, Bit 6) is set high, the serial port interprets both instruction and data bytes LSB first. Multibyte data transfers in LSB format can be completed by writing an instruction byte that includes the register address of the first address to be accessed. The AD9875 will automatically

increment the address for each successive byte required for the multibyte communication cycle. Figures 10a and 10b show how the serial port words are built for each of these modes.

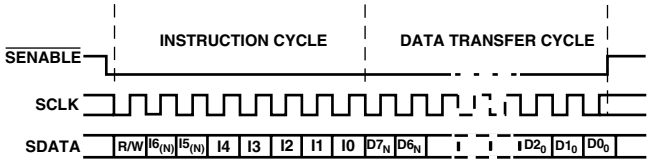


Figure 10a. Serial Register Interface Timing MSB-First

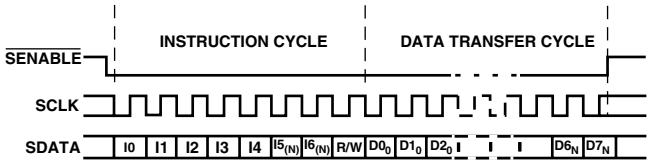


Figure 10b. Serial Register Interface Timing LSB-First

Notes on Serial Port Operation

The serial port is disabled and all registers are set to their default values during a hardware reset. During a software reset, all registers except register 0 are set to their default values. Register 0 will remain at the last value sent, with the exception that the *Software Reset* bit will be set to 0.

The serial port is operated by an internal state machine and is dependent on the number of SCLK cycles since the last time $\overline{\text{SENABLE}}$ went active. On every eighth rising edge of SCLK, a byte is transferred over the SPI. During a multibyte write cycle, this means the registers of the AD9875 are not simultaneously updated, but occur sequentially. For this reason, it is recommended that single byte transfers be used when changing the SPI configuration or performing a software reset.

Table IV. Register Layout

Address (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (hex)	Comments
0		SPI LSB First	Software Reset						0 × 00	Read/Write
1	Power-Down Regulator	Power-Down PLL-B	Power-Down PLL-A	Power-Down DAC	Power-Down Interpolator	Power-Down Rx Reference	Power-Down ADC and FPGA	Power-Down Rx LPF and CPGA	0 × 00	Read/Write PWR DN Pin Low
2	Power-Down Regulator	Power-Down PLL-B	Power-Down PLL-A	Power-Down DAC	Power-Down Interpolator	Power-Down Rx Reference	Power-Down ADC and FPGA	Power-Down Rx LPF and CPGA	0 × 9F	Read/Write PWR DN Pin High
3	Tx Port Negative Edge Sampling	ADC Clock Source PLL-B/2	PLL-B (×M) Multiplier < 5:4>		PLL-B (/N) Divider < 3:2>		PLL-A (×L) Multiplier < 1:0>		0 × 02	Read/Write
4	Rx LPF Tuning Update Disable	Rx LPF Tuning In Progress (Read Only)	Rx Path DC Offset Correction	Rx Digital HPF Bypass	Fast ADC Sampling	Wideband Rx LPF	Enable 1-Pole Rx LPF	Rx LPF Bypass	0 × 01	Read/Write
5	Rx LPF Fc Adjust <7:0>								0 × 80	Read/Write
6			PGA Gain Set by Register	Rx Path Gain Adjust <4:0>					0 × 00	Read/Write
7		Interpolation Filter Select <3:0>			Power-Down Interpolator at Tx QUIET Pin Low	Tx Port LS Nibble First	Tx Port Width 5-bits	Tx Port Multiplexer Bypass	0 × 00	Read/Write
8	Invert CLK B	Invert CLK A	Disable CLK B	Disable CLK A	Three-State Rx Port	Rx Port LS Nibble First	Rx Port Width 5-bits	Rx Port Multiplexer Bypass	0 × 00	Read/ Write
F					Die Revision Number <3:0>					Read Only

REGISTER PROGRAMMING DEFINITIONS

REGISTER 0—RESET/SPI Configuration

Bit 5: Software Reset
Setting this bit high resets the chip. The PLLs will relock to the input clock and all registers (except Register 0 × 0, Bit 6) revert to their default values. Upon completion of the reset, Bit 5 is reset to 0.

The content of the interpolator stages are not cleared by software or hardware resets. It is recommended to "flush" the transmit path with zeros before transmitting data.

Bit 6: LSB/MSB First
Setting this bit high causes the serial port to send and receive data least significant bit (LSB) first. The default low state configures the serial port to send and receive data most significant bit (MSB) first.

REGISTERS 1 AND 2—POWER-DOWN

The combination of the PWR DN pin and Registers 1 and 2 allow for the configuration of two separate pin selectable power settings. The PWR DN pin selects between two sets of individually programmed operation modes.

When the PWR DN pin is low, the functional blocks corresponding to the bits set in register 1 will be powered down.

When the PWR DN pin is high, the functional blocks corresponding to the bits set in Register 2 will be powered down

Bit 0: Power-Down Receive Filter and CPGA
Setting this bit high powers down and bypasses the Rx LPF and coarse programmable gain amplifier.

Bit 1: Power-Down ADC and FPGA
Setting this bit high powers down the ADC and fine programmable gain amplifier (FPGA).

Bit 2: Power-Down Rx Reference
Setting this bit high powers down the ADC reference. This bit should be set if an external reference is applied.

Bit 3: Power-Down Interpolators
Setting this bit high powers down the transmit digital interpolators. It does not clear the content of the data path.

Bit 4: Power-Down DAC
Setting this bit high powers down the transmit DAC.

Bit 5, Bit 6: Power-Down PLL-A, PLL-B
Setting these bits high powers down the on-chip phase lock loops which generated CLK-A and CLK-B respectively. When powered down these clocks are high impedance.

Bit 7: Power-Down Regulator
Setting this bit high powers down the on-chip voltage control regulator.

REGISTER 3—CLOCK SOURCE CONFIGURATION

The AD9875 integrates two independently programmable PLLs referred to as PLL-A and PLL-B. The outputs of the PLLs are used to generate all the chips internal and external clock signals from the f_{CLKIN} signal. All Tx path clock signals are derived from PLL-A. If f_{CLKIN} is programmed as the ADC sampling clock source, the Rx port clocks are also derived from PLL-A. Otherwise, the ADC sampling clock is PLL-B/2 and the Rx path clocks are derived from PLL-B.

The best Rx path performance will be gained when the ADC sampling clock is derived from f_{CLKIN}. When f_{CLKIN} provides the ADC sampling clock, the PLL-A multiplier, L, must be set to 4. This restriction is due to the way the output clocking for the Rx path is implemented.

Bit 1,0: PLL-A Multiplier
Bits 1 and 0 determine the multiplication factor (L) for PLL-A and the DAC sampling clock frequency, f_{DAC}.

$$f_{DAC} = L \times f_{CLKIN}$$

Bit 1,0
0,0: L = 1
0,1: L = 2
1,0: L = 4
1,1: L = 8

Bit 5 to 2: PLL-B Multiplier/Divider
Bits 5 to 2 determine the multiplication factor (M) and division factor (N) for PLL-B and the CLK-B frequency. For multiplexed 10-/12-bit data, $f_{CLK\text{-}B} = f_{CLKIN} \times M/N$. For nonmultiplexed 6-bit data, $f_{CLK\text{-}B} = (f_{CLKIN}/2) \times M/N$. All nine combinations of M and N values are valid, yielding seven unique M/N ratios.

Bit 5,4	Bit 3,2
0,0: M = 3	0,0: N = 2
0,1: M = 4	0,1: N = 4
1,0: M = 6	1,0: N = 1

Bit 6: ADC Clock Source PLL-B/2
Setting Bit 6 high selects PLL-B/2 as the ADC sampling Clock source. In this mode, the Rx data and CLK-B will run at a rate of $f_{CLK\text{-}B}$. RxSYNC will run at $f_{CLK\text{-}B}/2$.

Setting Bit 6 low selects the f_{CLKIN} signal as the ADC sampling clock source. This mode of operation yields the best ADC performance if an external crystal is used or a low jitter clock source drives the OSCIN pin.

Bit 7: Tx Port Negative Edge Sampling
Setting Bit 7 high will cause the Tx port to sample the TxDATA and TxSYNC on the falling edge of CLK-A. By default, the Tx Port sampling occurs on the rising edge of CLK-A. The timing is shown in Figure 5.

REGISTER 4—RECEIVE FILTER SELECTION

The AD9875 receive path has a continuous time 4-pole LPF and a 1-pole digital HPF. The 4-pole LPF has two selectable cutoff frequencies. Additionally, the filter can be tuned around those two cutoff frequencies. These filters can also be bypassed to different degrees as described below.

The continuous time 4-pole low-pass filter is automatically calibrated to one of two selectable cutoff frequencies.

The cutoff frequency f_{CUTOFF} is described as a function of the ADC sampling frequency f_{ADC} and can be influenced (±30%) by the Rx-Filter Tuning Target word in Register 5.

$$f_{CUTOFF\ LOW} = f_{ADC} \times 64/\left(Target + 64\right)$$

$$f_{CUTOFF\ HIGH} = f_{ADC} \times 158/\left(Target + 64\right)$$

Bit 0: Rx LPF Bypass
Setting this bit high bypasses the 4-pole LPF. The filter is automatically powered down when this bit is set.

Bit 1: Enable 1-Pole Rx LPF
The AD9875 can be configured with an additional 1-pole ~16 MHz input filter for applications that require steeper filter roll-off or want to use the 1-pole filter instead of the 4-pole receive Low-Pass filter. The 1-pole filter is untrimmed and subject to cutoff frequency variations of ±20%.

Bit 2: Wideband Rx LPF
This bit selects the nominal cutoff frequency of the 4-pole LPF. Setting this bit high selects a nominal cutoff frequency of 28.8 MHz. When the wideband filter is selected, the Rx path gain is limited to 30 dB.

Bit 3: Fast ADC Sampling
Setting this bit increases the quiescent current in the SVGA block. This may provide some performance improvement when the ADC sampling frequency is greater than 50 MSPS (in 6-bit mode).

Bit 4: Rx Digital HPF Bypass
Setting this bit high bypasses the 1-pole digital HPF that follows the ADC. The digital filter must be bypassed for ADC sampling above 50 MSPS.

Bit 5: Rx Path DC Offset Correction
Writing a One to this bit triggers an immediate receive path offset correction and reads back zero after the completion of the offset correction.

Bit 6: Rx LPF Tuning Update In Progress
This bit indicates when receive filter calibration is in progress. The duration of a receive filter calibration is about 500 ms. Writing to this bit has no effect.

Bit 7: Rx LPF Tuning Update Disable
Setting this bit high disables the automatic background receive filter calibration. The AD9875 automatically calibrates the receive filter on reset and every few (~2) seconds thereafter to compensate for process and temperature variation, power supply and long term drift. Programming a one to this bit disables this function. Programming a zero triggers an immediate first calibration and enables the periodic update.

REGISTER 5—RECEIVE FILTER TUNING TARGET

This register sets the filter tuning target as a function of f_{OSCIN}. See Register 4 description.

REGISTER 6—Rx PATH GAIN ADJUST

The AD9875 uses a combination of a continuous time PGA (CPGA) and a switched capacitor PGA (SPGA) for a gain range of –6 to 36 dB with a resolution of 2 dB. The Rx path gain can be programmed over the serial interface by writing to the Rx Path Gain Adjust register or directly using the GAIN and MSB aligned Tx[5:1] bits. The register default value is 0×00 for lowest gain setting (–6 dB). The register always reads back the actual gain setting irrespective of which of the two programming modes were used.

Table V describes the gains and how they are achieved as a function of the Rx Path adjust bits.

Bit 5: PGA Gain Set through Register
Setting this bit high will result in the Rx Path Gain being set by writing to the PGA Gain Control register. Default is zero which selects writing the gain through the Tx[5:1] pins in conjunction with the gain pin.

Table V. PGA Programming Map

Rx Path Gain [4:0]	Rx Path Gain	CPGA Gain	SPGA Gain
0×00	–6	–6	0
0×01	–4	–6	2
0×02	–2	–6	4
0×03	0	–6	6
0×04	2	–6	8
0×05	4	–6	10
0×06	6	0	6
0×07	8	0	8
0×08	10	0	10
0×09	12	6	6
$0 \times 0A$	14	6	8
$0 \times 0B$	16	6	10
$0 \times 0C$	18	12	6
$0 \times 0D$	20	12	8
$0 \times 0E$	22	12	10
$0 \times 0F$	24	18	6
0×10	26	18	8
0×11	28	18	10
0×12*	30/30	18/24	12/6
0×13*	30/32	18/24	12/8
0×14*	30/34	18/24	12/10
0×15*	30/36	18/24	12/12

*When the Wideband Rx Filter bit is set high, the Rx Path Gain is limited to 30 dB. The first of the two values in the chart refers to this mode. The second number refers to the mode when the lower Rx LPF cutoff frequency is chosen, or the Rx LPF filter is bypassed.

REGISTER 7—TRANSMIT PATH SETTINGS

The AD9875 transmit path has a programmable interpolation filter that precedes the transmit DAC. The interpolation filter can be programmed to operate in seven different modes. Also, the digital interface can be programmed to operate in several different modes. These modes are described below.

Bit 0: Transmit Port Demultiplexer Bypass
Setting Bit 0 high bypasses the input data demultiplexer. In this mode, consecutive nibbles on the TxDATA(5:0) pins are treated as individual words to be sent through the Tx path. This creates a six bit data path. The state of TxSYNC is ignored in this mode.

Bit 1: Transmit Port Width
If Bit 1 is set high, the Tx port will operate such that the most significant nibble and the least significant nibble are each five bits wide. The default mode is six bits for the most significant nibble and four bit for the least significant nibble. The data is always aligned to the MSB pin Tx[5]. Enabling this pin on the AD9875 allows for a five pin versus the default six pin interface.

Bit 2: Transmit Port Least Significant Nibble First
Setting Bit 2 high reconfigures the AD9875 for a transmit mode that expects least significant nibble before the most significant nibble.

Bit 3: Power-Down Interpolator at TxQUIET Pin Low
Setting Bit 3 high enables the TxQUIET pin to shut off the DAC output. If the bit is set to one, then pulling the TxQUIET pin low will power down the interpolator filters. In most applications the interpolator filter will need to be flushed with zeros before or after being powered down.

Bit 4 to Bit 7: Interpolation Filter Select
Bits 4 to 7 define the Interpolation filter characteristic and interpolation rate.

Bits 7:4;
0 × 2; Interpolation Bypass.
0 × 0; see TPC 1. 4× Interp, LPF.
0 × 1; see TPC 2. 2× Interp, LPF.
0 × 4; see TPC 3. 4× Interp, BPF, Adj image.
0 × 5; see TPC 4. 2× Interp, BPF, Adj image.
0 × 8; see TPC 5. 4× Interp, BPF, lower image.
0 × C; see TPC 6. 4× Interp, BPF, upper image.

The interpolation factor has a direct influence on the CLK-A output frequency. When the transmit input data multiplexer is enabled (10-bit mode):

$$f_{CLK-A} = 2 \times f_{DAC}/K$$

where K is the interpolation factor.

When the transmit input data multiplexer is disabled (5-/6-bit mode):

$$f_{CLK-A} = f_{DAC}/K$$

where K is the interpolation factor.

REGISTER 8—RECEIVER AND CLOCK OUTPUT SETTINGS
Bit 0: Rx Port Multiplexer Bypass
Setting this bit high bypasses the Rx port output multiplexer. This will output only the 6 MSBs of the ADC word. This mode enables ADC sampling rates above 55 MSPS.

Bit 1: Rx Port Width Five Bits
If the bit is set high, the Rx port data will be output in two nibbles of five bits each (on pins Rx[5:1]). When this bit is low (default), the most significant nibble will contain six bits and the least significant nibble will have four bits. The default mode makes the AD9875 pin compatible with the AD9876.

Bit 2: Rx Port LS Nibble First
Reconfigures the AD9875 for a receive mode that expects less significant bits before the most significant bits.

Bit 3: Three-State Rx Port
This bit sets the receive output Rx[5:0] into a high impedance three-state mode. It allows for sharing the bus with other devices.

Bit 4, Bit 5: Disable CLK-A, Disable CLK-B
Setting Bit 4 or Bit 5 stops CLK-A or CLK-B respectively, from toggling. The output is held to a logic 0 level.

Bit 4, Bit 5: Disable CLK-A, Disable CLK-B
Setting Bit 4 or Bit 5 fixes CLK-A or CLK-B to a low output level, respectively.

Bit 6: CLK-A Output Invert
Setting Bit 6 high inverts the CLK-A output signal.

Bit 7: CLK-B Output Invert
Setting this bit high inverts the CLK-B output signal. This effectively changes the timing of the Rx[5:0] and RxSYNC signals from rising edge triggered to falling edge triggered with respect to the CLK-B signal.

REGISTER F—DIE REVISION
This register stores the die revision of the chip. It is a read-only register.

PCB DESIGN CONSIDERATIONS
Although the AD9875 is a mixed-signal device, the part should be treated as an analog component. The digital circuitry on-chip has been specially designed to minimize the impact that the digital switching noise will have on the operation of the analog circuits. Following the power, grounding and layout recommendations in this section will help you get the best performance from the MxFE.

Component Placement
If the three following guidelines of component placement are followed, chances for getting the best performance from the MxFE are greatly increased. First, manage the path of return currents flowing in the ground plane so that high frequency switching currents from the digital circuits do not flow on the ground plane under the MxFE or analog circuits. Second, keep noisy digital signal paths and sensitive receive signal paths as short as possible. Third, keep digital (noise generating) and analog (noise susceptible) circuits as far away from each other as possible.

In order to best manage the return currents, pure digital circuits that generate high switching currents should be closest to the power supply entry. This will keep the highest frequency return current paths short, and prevent them from traveling over the sensitive MxFE and analog portions of the ground plane. Also, these circuits should be generously bypassed at each device which will further reduce the high frequency ground currents. The MxFE should be placed adjacent to the digital circuits, such that the ground return currents from the digital sections will not flow in the ground plane under the MxFE. The analog circuits should be placed furthest from the power supply.

The AD9875 has several pins which are used to decouple sensitive internal nodes. These pins are REFIO, REFB, and REFT. The decoupling capacitors connected to these points should have low ESR and ESL. These capacitors should be placed as close to the MxFE as possible and be connected directly to the analog ground plane.

The resistor connected to the FSADJ pin should also be placed close to the device and connected directly to the analog ground plane.

Power Planes and Decoupling
The AD9875 evaluation board demonstrates a good power supply distribution and decoupling strategy. The board has four layers; two signal layers, one ground plane and one power plane. The power plane is split into a 3VDD section used for the 3 V digital logic circuits, a DVDD section used to supply the digital supply pins of the AD9875, an AVDD section used to supply the analog supply pins of the AD9875, and a VANLG section that supplies the higher voltage analog components on the board. The 3VDD section will typically have the highest frequency currents on the power plane and should be kept the furthest from the MxFE and analog sections of the board. The DVDD portion of the plane brings the current used to power the digital portion of the MxFE to the device. This should be treated similarly to the 3VDD power plane and be kept from going underneath the MxFE or analog components. The MxFE should largely sit on the AVDD portion of the power plane.

The AVDD and DVDD power planes may be fed from the same low noise voltage source; however, they should be decoupled from each other to prevent the noise generated in the DVDD portion of the MxFE from corrupting the AVDD supply. This can be done by using ferrite beads between the voltage source and DVDD, and between the source and AVDD. Both DVDD and AVDD should have a low ESR, bulk decoupling capacitor on the MxFE side of the ferrite as well as a low ESR, ESL decoupling capacitors on each supply pin (i.e., the AD9875 requires five power supply decoupling caps, one each on Pins 5, 38, 47, 14, and 35). The decoupling caps should be placed as close to the MxFE supply pins as possible. An example of the proper decoupling is shown in the AD9875 evaluation board schematic.

Ground Planes

In general, if the component placing guidelines discussed earlier can be implemented, it is best to have at least one continuous ground plane for the entire board. All ground connections should be made as short as possible. This will result in the lowest impedance return paths, and the quietest ground connections.

If the components cannot be placed in a manner that will keep the high-frequency ground currents from traversing under the MxFE and analog components, it may be necessary to put current steering channels into the ground plane to route the high-frequency currents around these sensitive areas. These current steering channels should be made only when and where necessary.

Signal Routing

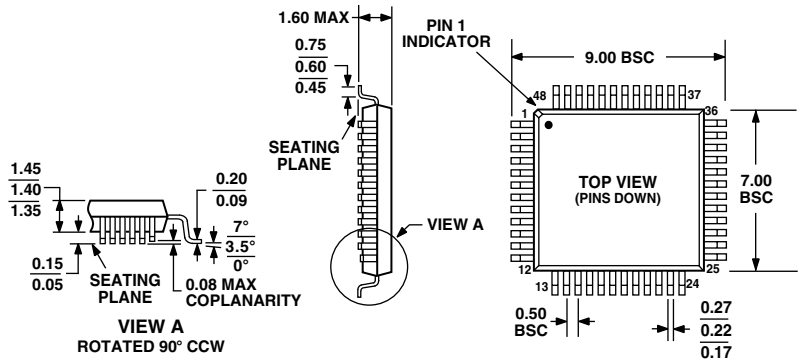
The digital Rx and Tx signal paths should be kept as short as possible. Also, the impedance of these traces should have a controlled characteristic impedance of about 50 Ω. This will prevent poor signal integrity and the high currents that can occur during undershoot or overshoot caused by ringing. If the signal traces cannot be kept shorter than about 1.5 inches, then series-termination resistors (33 Ω to 47 Ω) should be placed close to all signal sources. It is a good idea to series-terminate all clock signals at their source, regardless of trace length.

The receive Rx± signals are the most sensitive signals on the entire board. Careful routing of these signals is essential for good receive path performance. The Rx± signals form a differential pair and should be routed together as a pair. By keeping the traces adjacent to each other, noise coupled onto the signals will appear as common-mode and will be largely rejected by the MxFE receive input. Keeping the driving point impedance of the receive signal low and placing any low-pass filtering of the signals close to the MxFE will further reduce the possibility of noise corrupting these signals.

OUTLINE DIMENSIONS

48-Lead Plastic Quad Flatpack [LQFP]
(ST-48)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BBC

Revision History

Location	Page
8/02—Data Sheet changed from REV. 0 to REV. A.	
Changes to Table IV	20
Changes to REGISTER 3–CLOCK SOURCE CONFIGURATION	21
ST-48 package updated	25

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