



3.3V CMOS 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

IDT74ALVC162834

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels (0.4 μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVC162834:

- *Balanced Output Drivers: $\pm 12\text{mA}$*
- *Low switching noise*

APPLICATIONS:

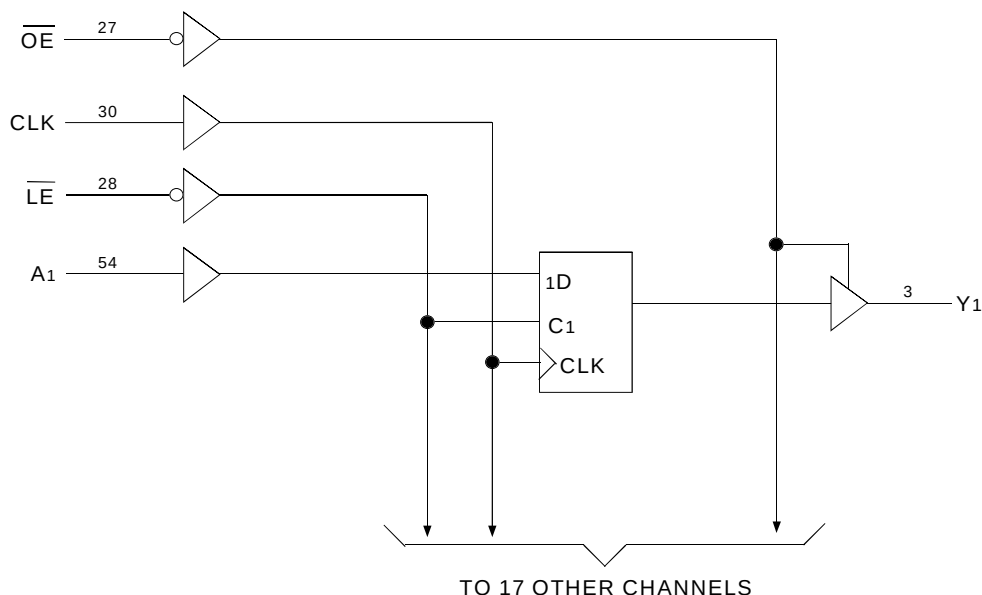
- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

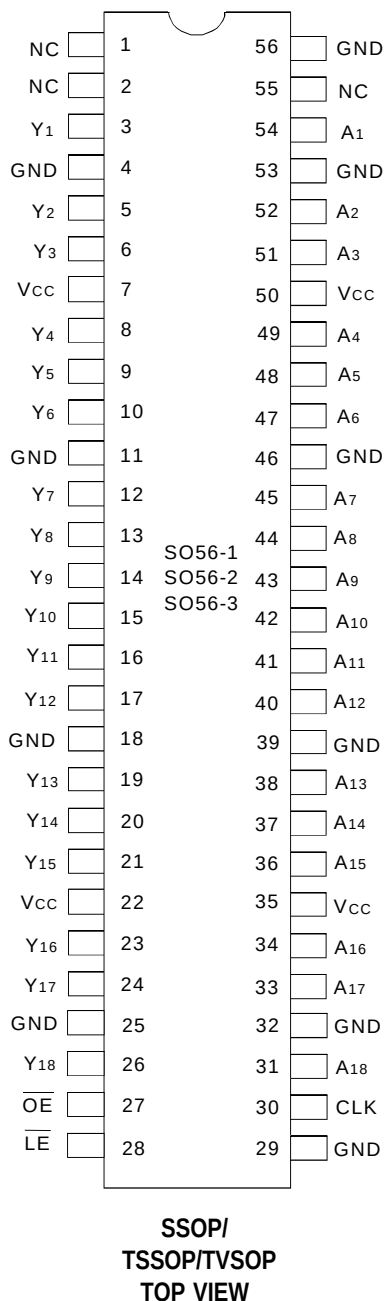
This 18-bit universal bus driver is built using advanced dual metal CMOS technology. Data flow from A to Y is controlled by the output-enable ($\overline{\text{OE}}$). The device operates in the transparent mode when the latch enable ($\overline{\text{LE}}$) input is low. The A data is latched if the clock (CLK) input is held at a high or low logic level. If $\overline{\text{LE}}$ is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{\text{OE}}$ is high, the outputs are in the high-impedance state.

The ALVC162834 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12\text{mA}$ at the designated threshold levels.

Functional Block Diagram



PIN CONFIGURATION



PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
CLK	Register Input Clock
$\overline{LE}$	Latch Enable (Transparent LOW)
Ax	Data Inputs
Yx	3-State Outputs
NC	No Internal Connection

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	- 0.5 to $V_{CC} + 0.5$	V
TSTG	Storage Temperature	- 65 to + 150	°C
IOUT	DC Output Current	- 50 to + 50	mA
I _{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I _{OK}	Continuous Clamp Current, $V_O < 0$	- 50	mA
I _{CC}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC} .

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	$V_{IN} = 0V$	5	7	pF
C _{OUT}	Output Capacitance	$V_{OUT} = 0V$	7	9	pF
C _{I/O}	I/O Port Capacitance	$V_{IN} = 0V$	7	9	pF

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NOTE:

- As applicable to the device type.

FUNCTION TABLE (1)

Inputs				Outputs
$\overline{OE}$	$\overline{LE}$	CLK	Ax	Yx
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y0 ⁽²⁾
L	H	L	X	Y0 ⁽³⁾

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
- Output level before indicated steady-state input conditions were established, provided that CLK is HIGH before $\overline{LE}$ went HIGH.
- Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	$V_{CC} = 3.6\text{V}$	$V_I = V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current	$V_{CC} = 3.6\text{V}$	$V_I = \text{GND}$	—	—	± 5	
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = V_{CC}$	—	—	± 10	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 10	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$ $V_{IN} = \text{GND}$ or V_{CC}		—	0.1	40	μA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	750	μA

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NOTE:

- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -4\text{mA}$	1.9	—	
			$I_{OH} = -6\text{mA}$	1.7	—	
		$V_{CC} = 2.7\text{V}$	$I_{OH} = -4\text{mA}$	2.2	—	
			$I_{OH} = -8\text{mA}$	2	—	
		$V_{CC} = 3.0\text{V}$	$I_{OH} = -6\text{mA}$	2.4	—	
			$I_{OH} = -12\text{mA}$	2	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OL} = 0.1\text{mA}$	—	0.2	V
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 4\text{mA}$	—	0.4	
			$I_{OL} = 6\text{mA}$	—	0.55	
		$V_{CC} = 2.7\text{V}$	$I_{OL} = 4\text{mA}$	—	0.4	
			$I_{OL} = 8\text{mA}$	—	0.6	
		$V_{CC} = 3.0\text{V}$	$I_{OL} = 6\text{mA}$	—	0.55	
			$I_{OL} = 12\text{mA}$	—	0.8	

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NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	VCC = 2.5V $\pm$ 0.2V	VCC = 3.3V $\pm$ 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	—	—	pF
CPD	Power Dissipation Capacitance Outputs disabled		—	—	pF

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	VCC = 2.5V $\pm$ 0.2V		VCC = 2.7V		VCC = 3.3V $\pm$ 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Ax to Yx	1	5	—	5	1	4.2	ns
t _{PLH} t _{PHL}	Propagation Delay $\overline{\text{LE}}$ to Yx	1.4	6.3	—	6.1	1.4	5.4	ns
t _{PLH} t _{PHL}	Propagation Delay CLK to Yx	1.4	6.3	—	6.1	1.4	5.4	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{\text{OE}}$ to Yx	1.4	6.3	—	6.5	1.1	5.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{\text{OE}}$ to Yx	1	4.7	—	4.9	1.3	4.5	ns
tw	Pulse Duration, $\overline{\text{LE}}$ LOW	3.3	—	3.3	—	3.3	—	ns
tw	Pulse Duration, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
tsu	Setup Time, data before CLK $\uparrow$	2.2	—	2.1	—	1.7	—	ns
tsu	Setup Time, data before $\overline{\text{LE}}$ $\uparrow$, CLK HIGH	1.2	—	1.6	—	1.3	—	ns
tsu	Setup Time, data before $\overline{\text{LE}}$ $\uparrow$, CLK LOW	1.4	—	1.5	—	1.2	—	ns
th	Hold Time, data after CLK $\uparrow$	0.6	—	0.6	—	0.7	—	ns
th	Hold Time, data after $\overline{\text{LE}}$ $\uparrow$, CLK HIGH or LOW	1.2	—	1.1	—	1.1	—	ns
tsk(o)	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:1. See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

2. Skew between any two outputs of the same package and switching in the same direction.

SWITCHING CHARACTERISTICS FROM 0°C TO 65°C , CL = 50 pF

Symbol	Parameter	VCC = 3.3V $\pm$ 0.15V		Unit
		Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay CLK to Yx	1.9	4.5	ns

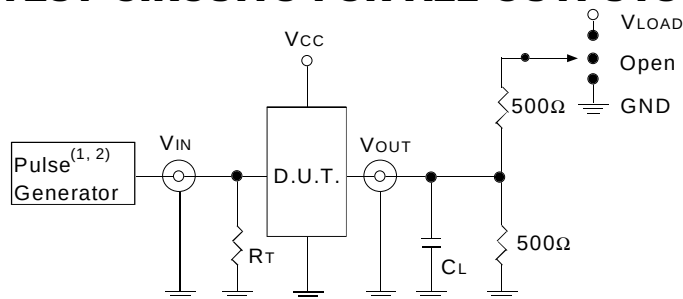
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

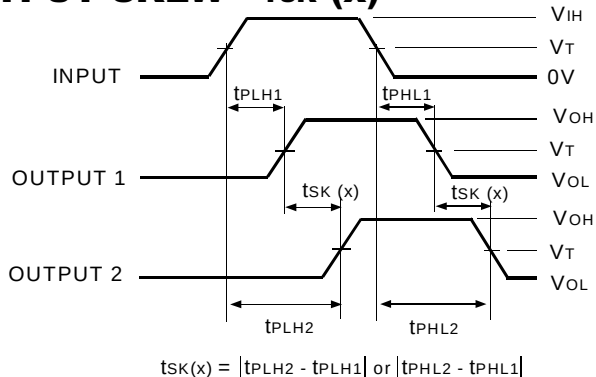
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)

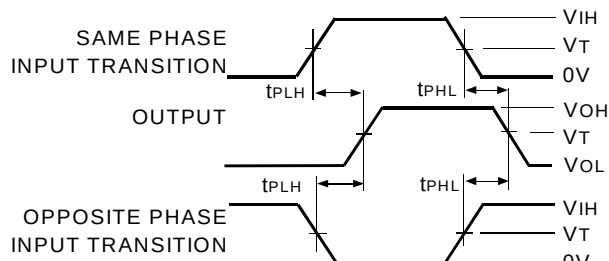


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NOTES:

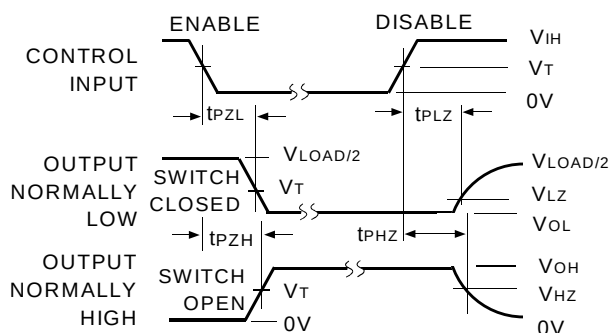
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

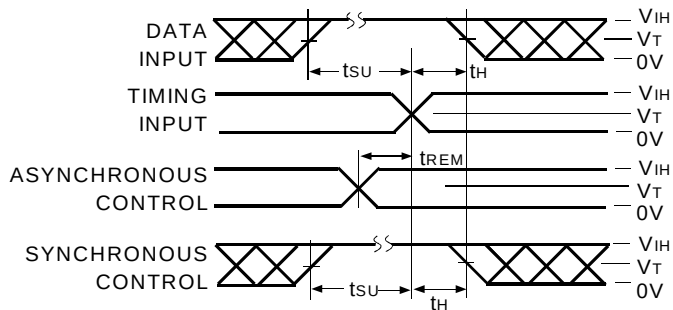


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NOTE:

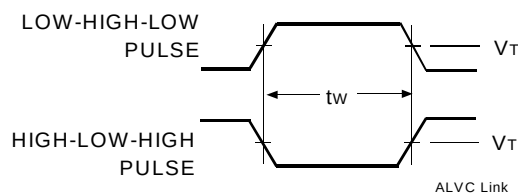
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT XX ALVC X XXX XXX XX
 Temp. Range Bus-Hold Family Device Type Package

					PV	Shrink Small Outline Package (SO56-1)
					PA	Thin Shrink Small Outline Package (SO56-2)
					PF	Thin Very Small Outline Package (SO56-3)
					834	18-Bit Universal Bus Driver with 3-State Outputs
					162	Double-Density with Resistors, ±12mA
					Blank	No Bus-Hold
					74	−40°C to +85°C



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

for SALES:
 800-345-7015 or 408-727-6116
 fax: 408-492-8674
www.idt.com*

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