



STQ1NK60ZR STD1LNK60Z-1

N-CHANNEL 600V - 13Ω - 0.8A TO-92/IPAK
Zener-Protected SuperMESH™ Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _W
STQ1NK60ZR	600 V	< 15 Ω	0.3 A	3 W
STD1LNK60Z-1	600 V	< 15 Ω	0.8 A	25 W

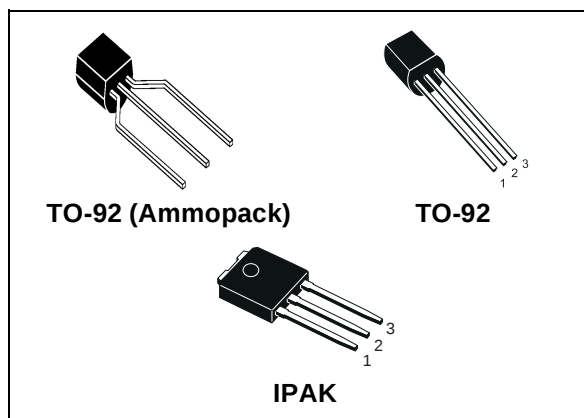
- TYPICAL R_{DS(on)} = 13Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- ESD IMPROVED CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

DESCRIPTION

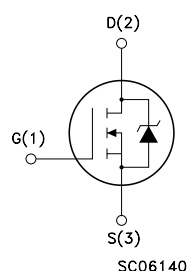
The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- AC ADAPTORS AND BATTERY CHARGERS
- SWITCH MODE POWER SUPPLIES (SMPS)



INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STQ1NK60ZR	1NK60ZR	TO-92	BULK
STQ1NK60ZR-AP	1NK60ZR	TO-92	AMMOPAK
STD1LNK60Z-1	D1LNK60Z	IPAK	TUBE

STQ1NK60ZR - STD1LNK60Z-1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		IPAK	TO-92	
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	600		V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	600		V
V_{GS}	Gate- source Voltage	± 30		V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	0.8	0.3	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	0.5	0.189	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	3.2	1.2	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	25	3	W
	Derating Factor	0.24	0.025	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5K Ω)	800		V
$dv/dt(1)$	Peak Diode Recovery voltage slope	4.5		V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150		$^\circ\text{C}$

(●) Pulse width limited by safe operating area

(1) $I_{SD} \leq 0.3\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

THERMAL DATA

		IPAK	TO-92	
$R_{thj-case}$	Thermal Resistance Junction-case Max	5	--	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	100	120	$^\circ\text{C}/\text{W}$
$R_{thj-lead}$	Thermal Resistance Junction-lead Max	--	40	$^\circ\text{C}/\text{W}$
T_l	Maximum Lead Temperature For Soldering Purpose	275	260	$^\circ\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	0.8	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	60	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{mA}$ (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED)
ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V$, $I_D = 0.4\text{ A}$		13	15	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = V$, $I_D = 0.4\text{ A}$		0.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, $f = 1\text{ MHz}$, $V_{GS} = 0$		94 17.6 2.8		pF pF pF
$C_{oss\text{ eq.}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0V$, $V_{DS} = 0V$ to $480V$		11		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 300V$, $I_D = 0.4\text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load see, Figure 3)		5.5 5		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 480V$, $I_D = 0.8\text{ A}$, $V_{GS} = 10V$		4.9 1 2.7	6.9	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 300V$, $I_D = 0.4A$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load see, Figure 3)		13 28		ns ns
$t_r(V_{off})$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 480V$, $I_D = 0.8A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$ (Inductive Load see, Figure 5)		28 12.5 48		ns ns ns

SOURCE DRAIN DIODE

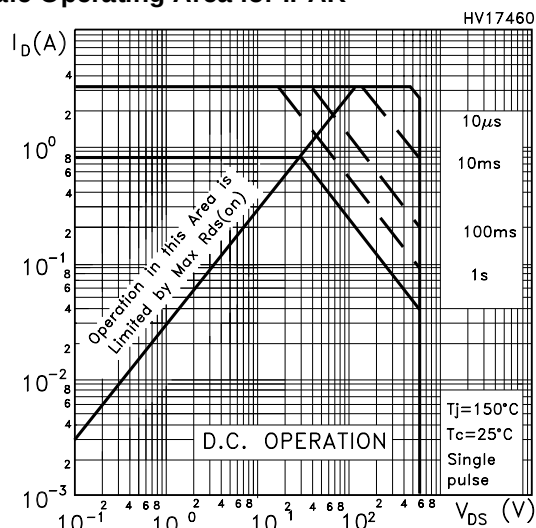
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				0.8 2.4	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 0.8A$, $V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 0.8\text{ A}$, $di/dt = 100A/\mu s$ $V_{DD} = 20V$, $T_J = 150^{\circ}C$ (see test circuit, Figure 5)		140 224 3.2		ns nC A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

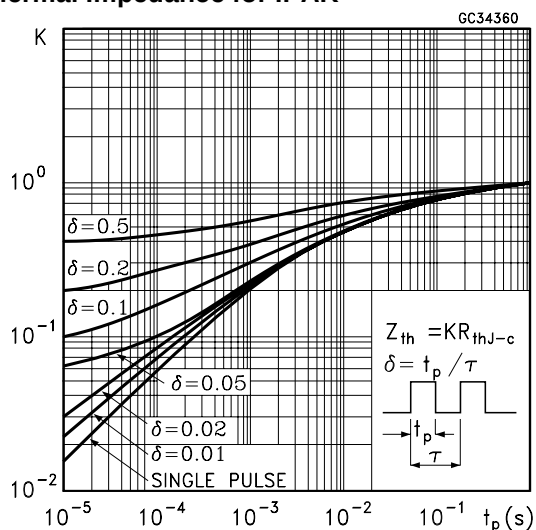
2. Pulse width limited by safe operating area.

3. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

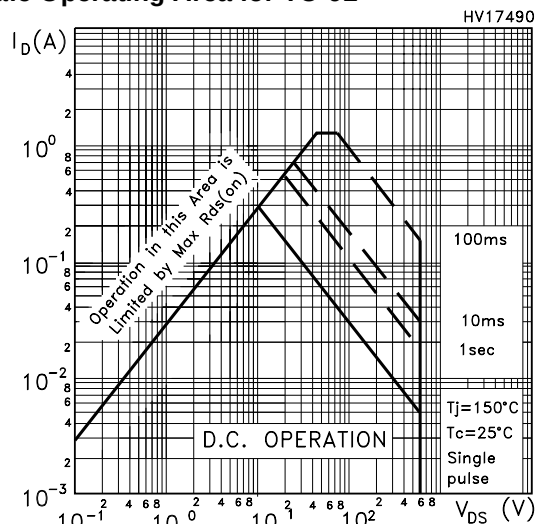
Safe Operating Area for IPAK



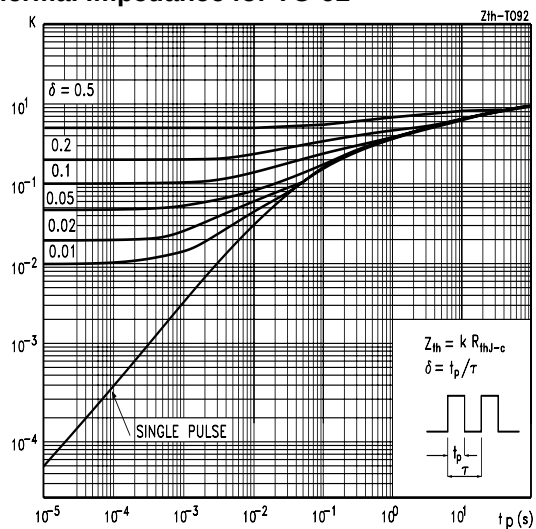
Thermal Impedance for IPAK



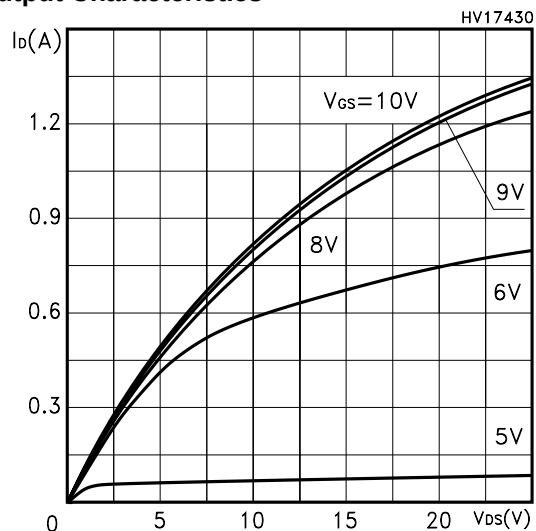
Safe Operating Area for TO-92



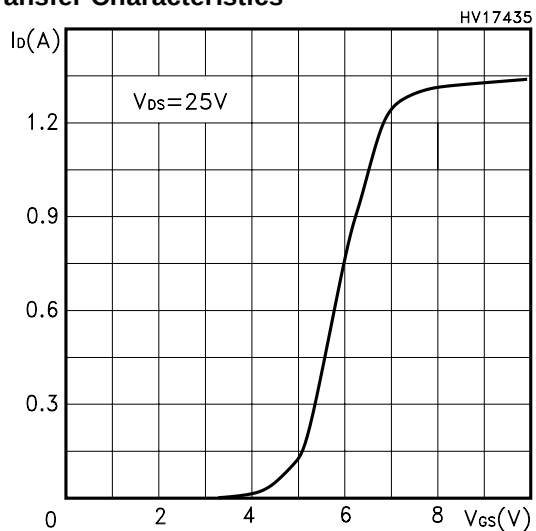
Thermal Impedance for TO-92



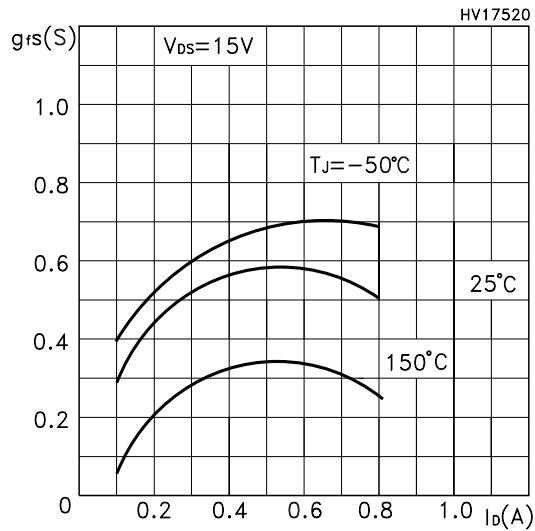
Output Characteristics



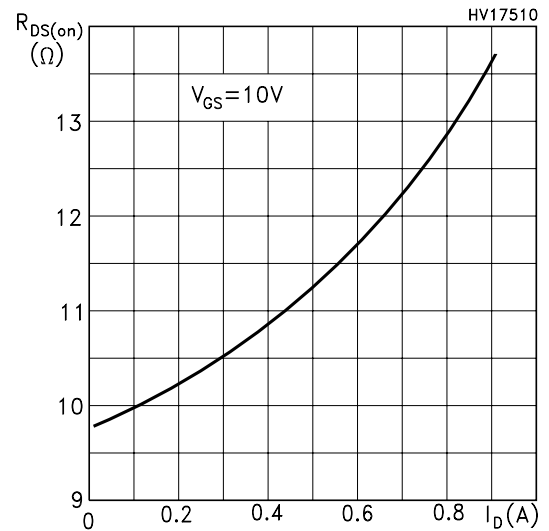
Transfer Characteristics



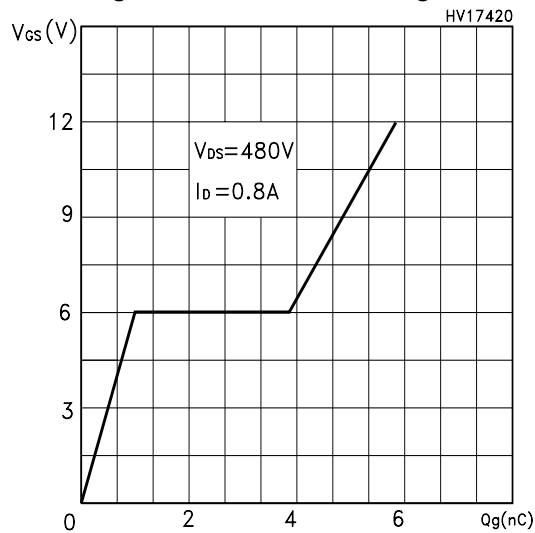
Transconductance



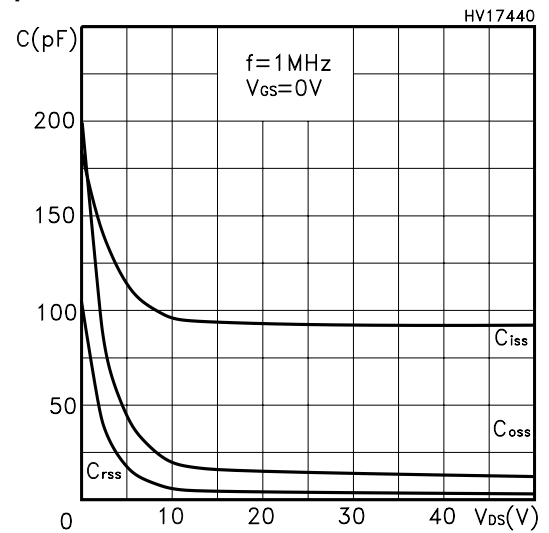
Static Drain-source On Resistance



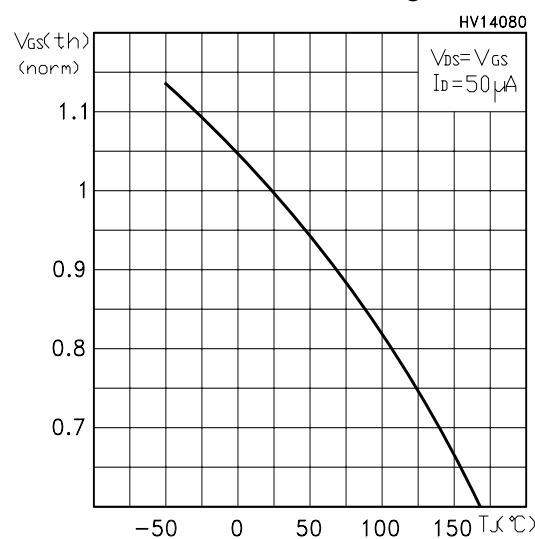
Gate Charge vs Gate-source Voltage



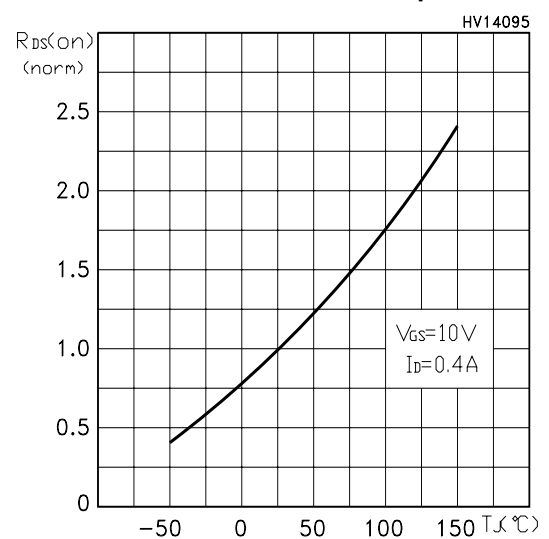
Capacitance Variations



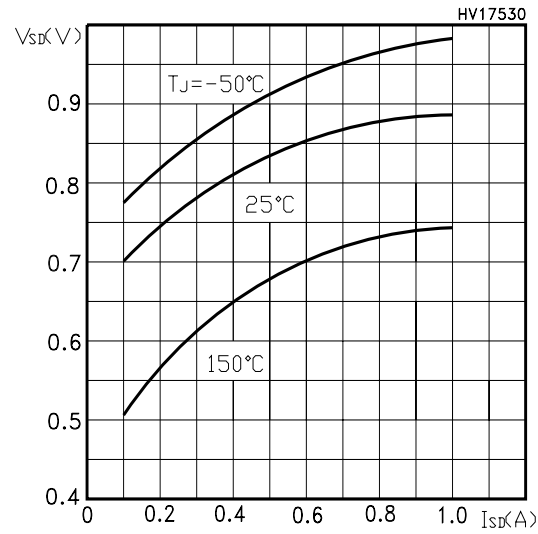
Normalized Gate Threshold Voltage vs Temp.



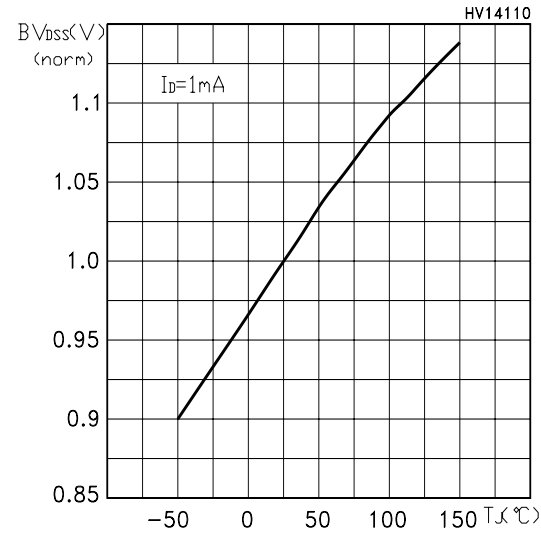
Normalized On Resistance vs Temperature



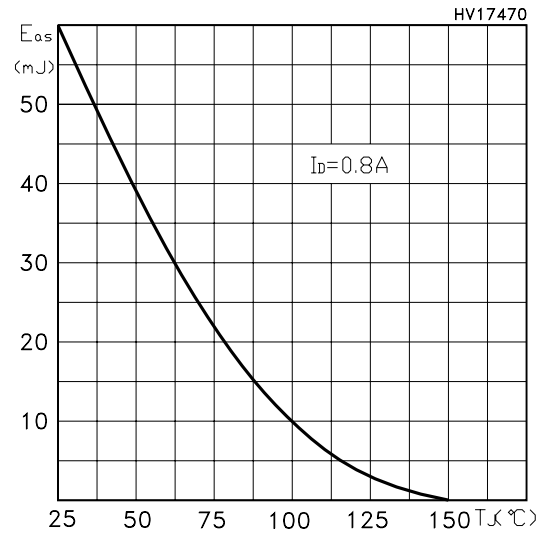
Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature



Maximum Avalanche Energy vs Temperature



Max Id Current vs Tc

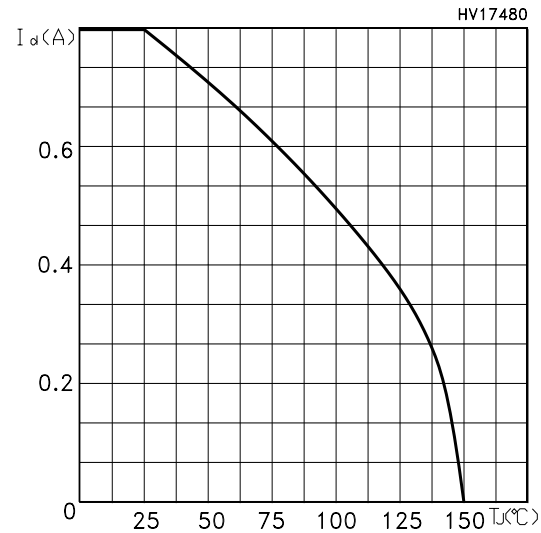


Fig. 1: Unclamped Inductive Load Test Circuit

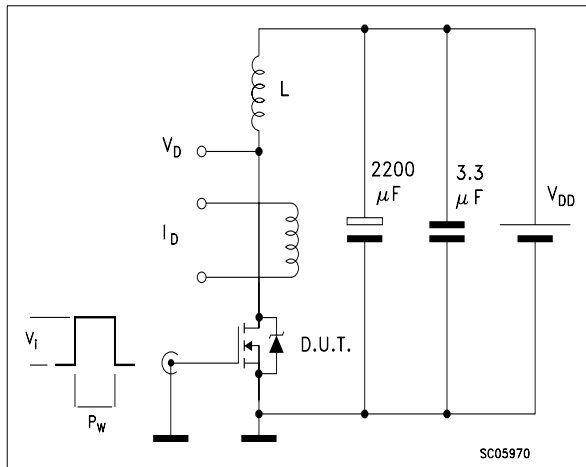


Fig. 2: Unclamped Inductive Waveform

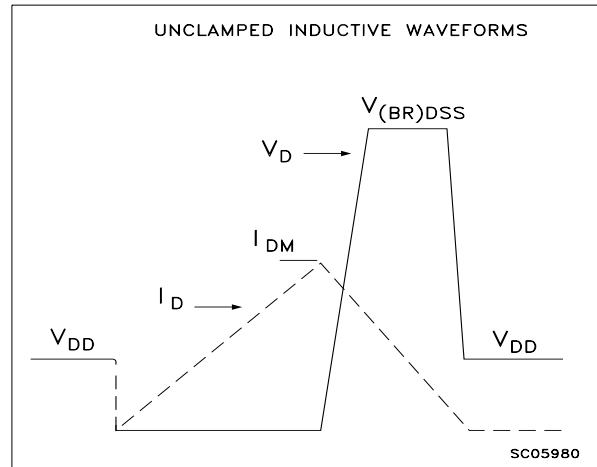


Fig. 3: Switching Times Test Circuit For Resistive Load



Fig. 4: Gate Charge test Circuit

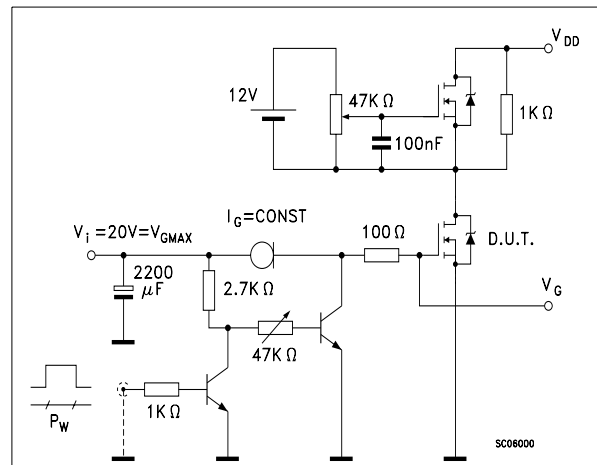
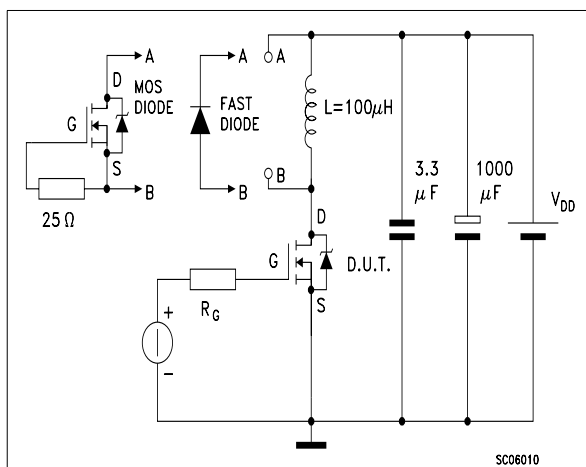
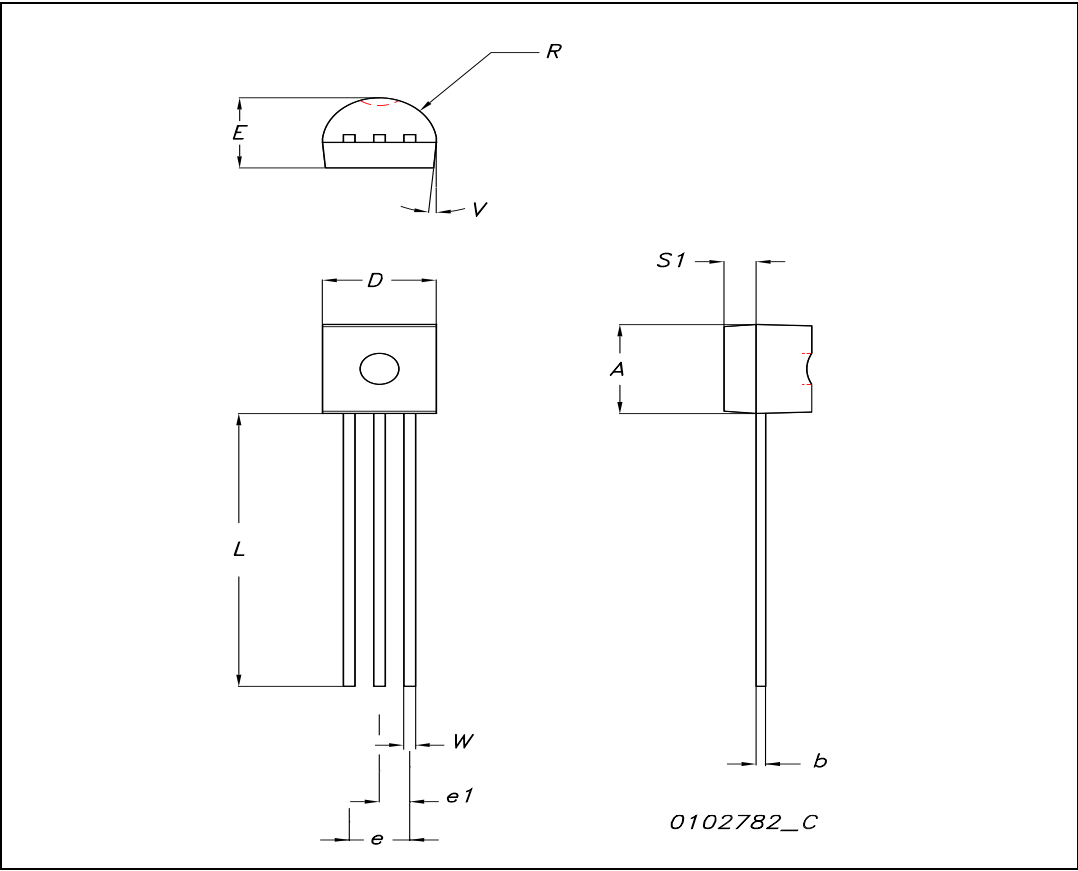


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



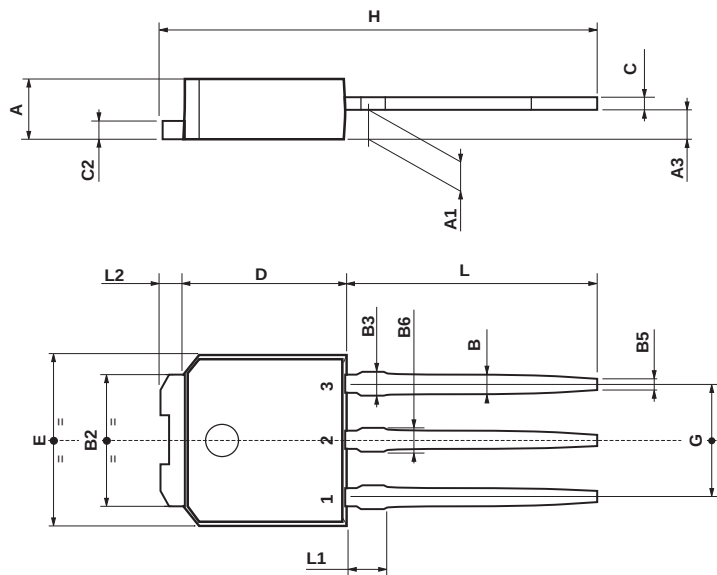
TO-92 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	



TO-251 (IPAK) MECHANICAL DATA

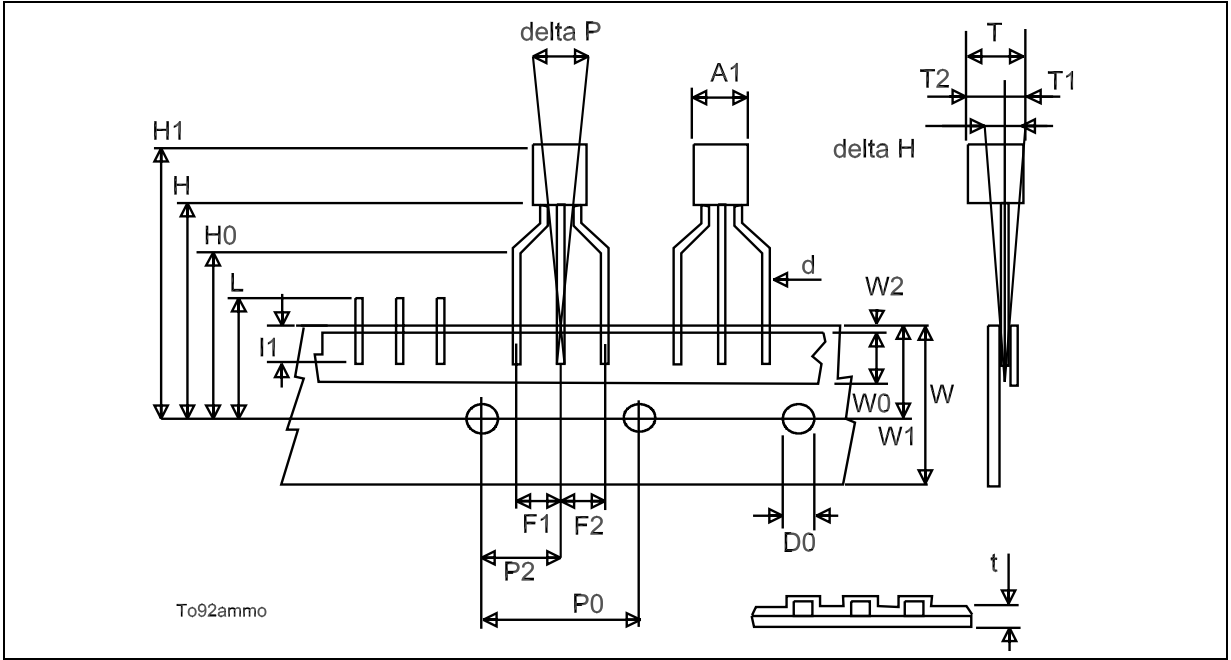
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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TO-92 AMMOPACK

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A1	4.45		4.95	0.170		0.194
T	3.30		3.94	0.130		0.155
T1			1.6			0.06
T2			2.3			0.09
d	0.41		0.56	0.016		0.022
P0	12.5	12.7	12.9	0.49	0.5	0.51
P2	5.65	6.35	7.05	0.22	0.25	0.27
F1, F2	2.44	2.54	2.94	0.09	0.1	0.11
delta H	-2		2	-0.08		0.08
W	17.5	18	19	0.69	0.71	0.74
W0	5.7	6	6.3	0.22	0.23	0.24
W1	8.5	9	9.25	0.33	0.35	0.36
W2			0.5			0.02
H	18.5		20.5	0.72		0.80
H0	15.5	16	16.5	0.61	0.63	0.65
H1			25			0.98
D0	3.8	4	4.2	0.15	0.157	0.16
t			0.9			0.035
L			11			0.43
I1	3			0.11		
delta P	-1		1	-0.04		0.04



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