

N-Channel Power MOSFET

800V, 9.5A, 1.05Ω

FEATURES

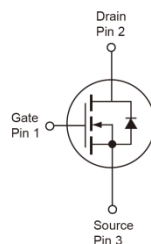
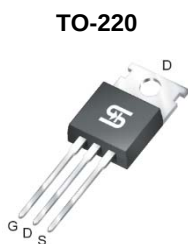
- Low $R_{DS(on)}$ 1.05Ω (Max.)
- Low gate charge typical @ 53nC (Typ.)
- Improve dV/dt capability
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

APPLICATION

- Power Supply
- Lighting

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
V_{DS}	800	V
$R_{DS(on)}$ (max)	1.05	Ω
Q_g	53	nC



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TO-220	ITO-220	UNIT
Drain-Source Voltage	V_{DS}	800		V
Gate-Source Voltage	V_{GS}	±30		V
Continuous Drain Current (Note 1)	I_D	9.5		A
		5.7		
Pulsed Drain Current (Note 2)	I_{DM}	38		A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	290	48	W
Single Pulsed Avalanche Energy	E_{AS}	267		mJ
Single Pulsed Avalanche Current	I_{AS}	10		A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150		°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TO-220	ITO-220	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	0.43	2.6	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62.5		°C/W

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static ^(Note 3)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	800	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	V _{GS(TH)}	2.0	--	4.0	V
Gate Body Leakage	V _{GS} = ±30, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = 800V, V _{GS} = 0V	I _{DSS}	--	--	10	μA
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 4.75A	R _{DS(on)}	--	0.9	1.05	Ω
Forward Transconductance	V _{DS} = 30V, I _D = 4.75A	g _{fs}	--	6.3	--	S
Dynamic ^(Note 4)						
Total Gate Charge	V _{DS} = 640V, I _D =9.5A, V _{GS} = 10V	Q _g	--	53	--	nC
Gate-Source Charge		Q _{gs}	--	10	--	
Gate-Drain Charge		Q _{gd}	--	23	--	
Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	2336	--	pF
Output Capacitance		C _{oss}	--	214	--	
Reverse Transfer Capacitance		C _{rss}		29		
Switching ^(Note 5)						
Turn-On Delay Time	V _{DS} = 400V, V _{GS} = 10V R _G = 25Ω, I _D = 9.5A	t _{d(on)}	--	63	--	ns
Turn-On Rise Time		t _r	--	62	--	
Turn-Off Delay Time		t _{d(off)}	--	256	--	
Turn-Off Fall Time		t _f	--	72	--	
Source-Drain Diode ^(Note 3)						
Forward On Voltage	I _S = 9.5A, V _{GS} = 0V	V _{SD}	--	--	1.5	V
Reverse Recovery Time	I _S = 9.5A, V _{GS} = 0V dI _F /dt = 100A/μs	t _{rr}	--	450	--	ns
Reverse Recovery Charge		Q _{rr}	--	5.3	--	μC

Notes:

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3. $L = 5mH, I_{AS} = 10A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
100% Eas Test Condition: $L = 5mH, I_{AS} = 5A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$.
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

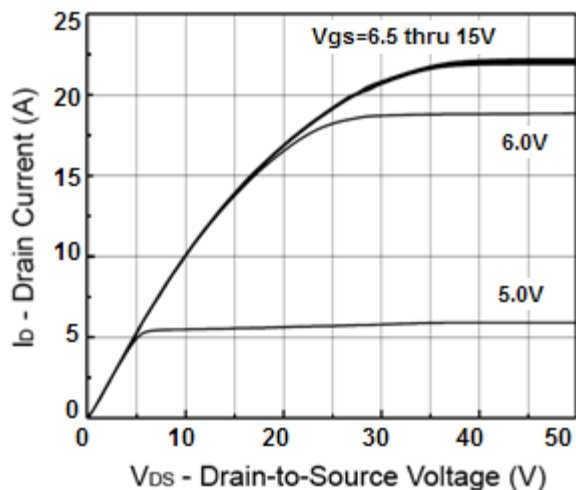
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM10N80CZ C0G	TO-220	50pcs / Tube
TSM10N80CI C0G	ITO-220	50pcs / Tube

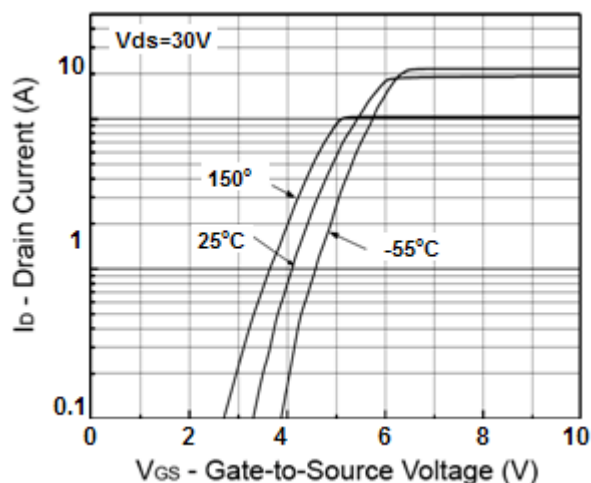
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

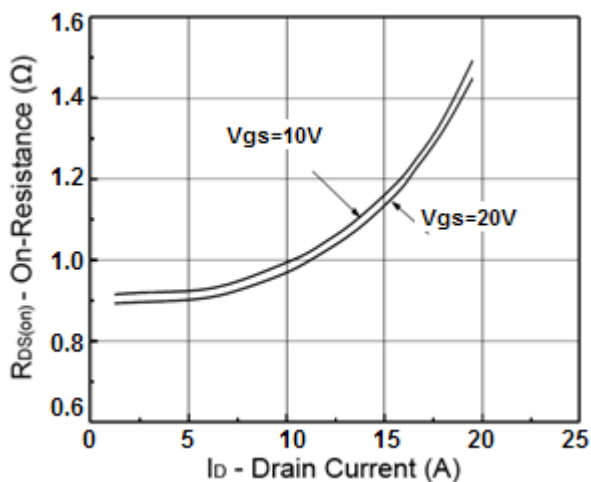
Output Characteristics



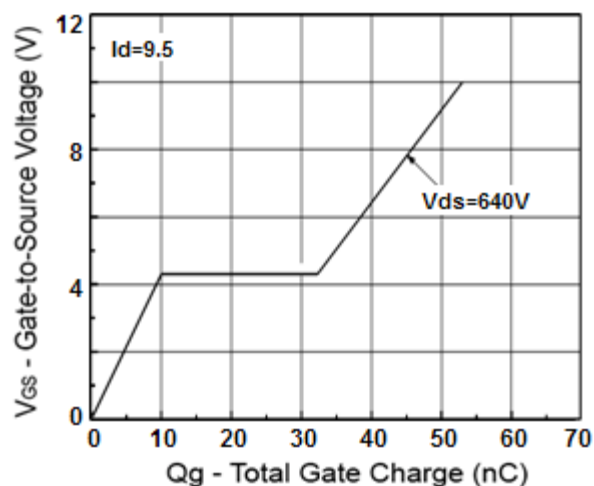
Transfer Characteristics



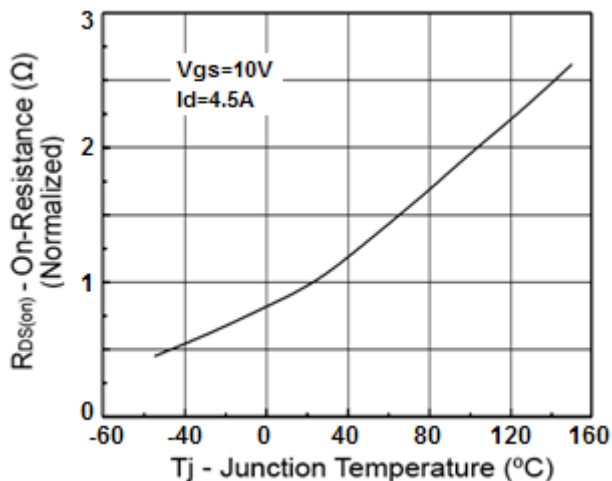
On-Resistance vs. Drain Current



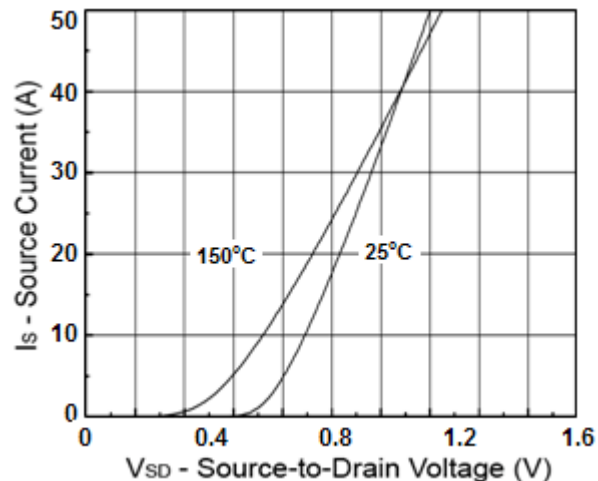
Gate Charge



On-Resistance vs. Junction Temperature



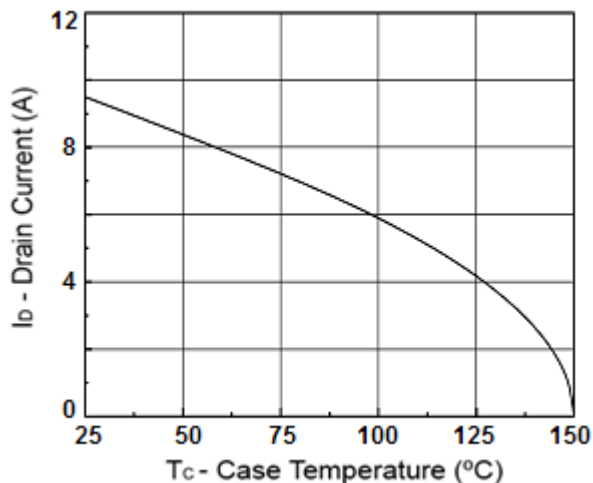
Source-Drain Diode Forward Voltage



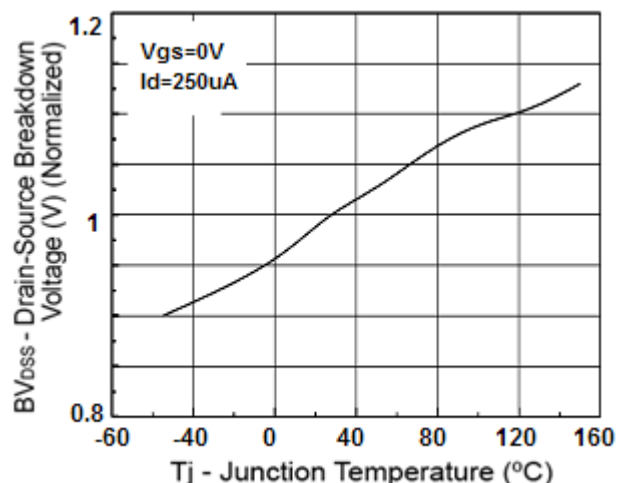
CHARACTERISTICS CURVES

($T_c = 25^\circ\text{C}$ unless otherwise noted)

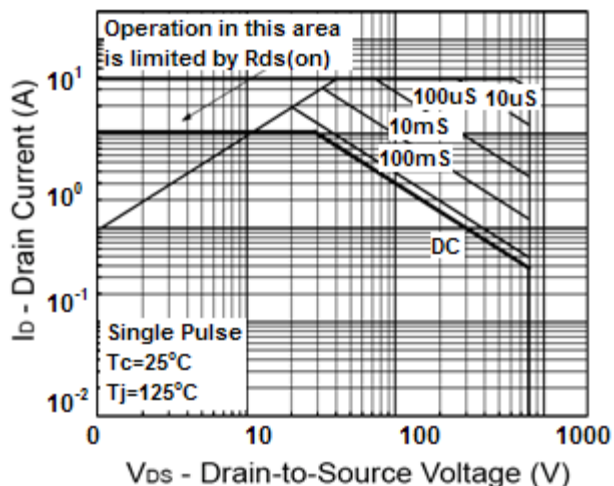
Drain Current vs. Case Temperature



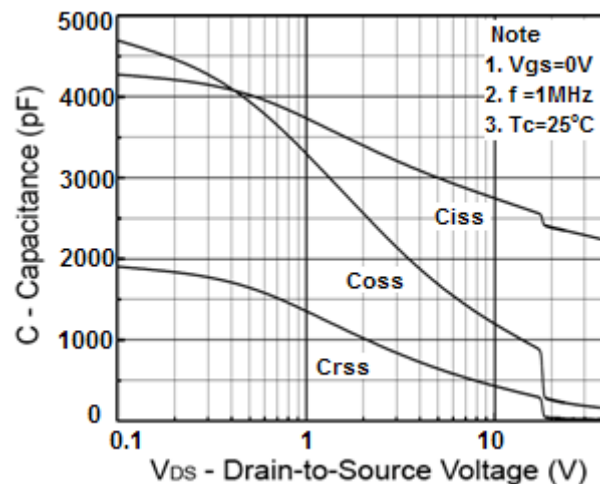
BV_{DSS} vs. Junction Temperature



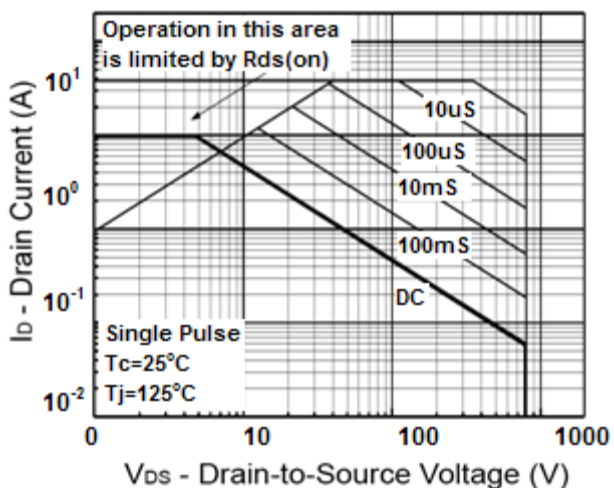
Maximum Safe Operating Area



Capacitance vs. Drain-Source Voltage



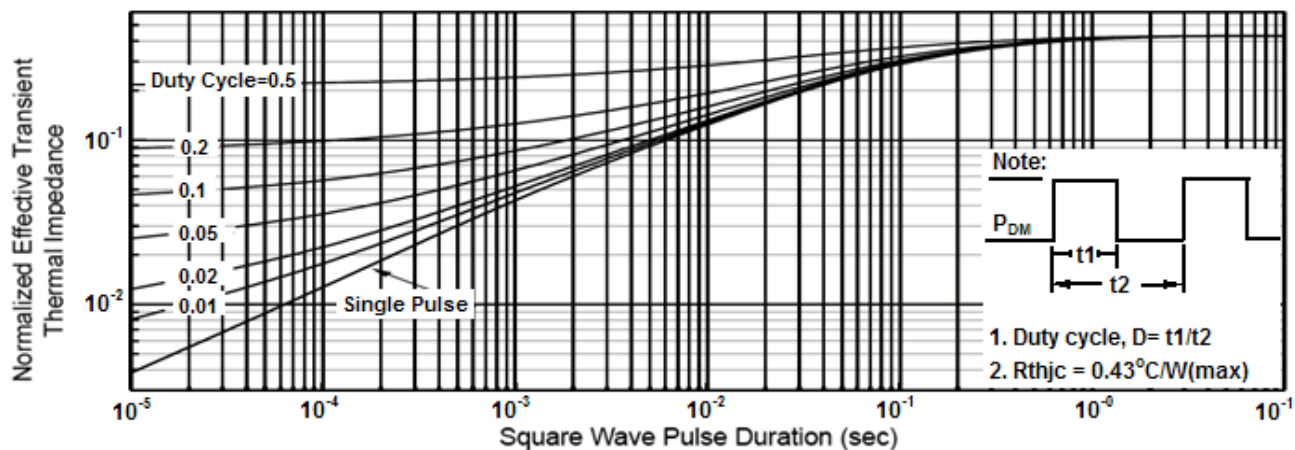
Maximum Safe Operating Area (ITO-220)



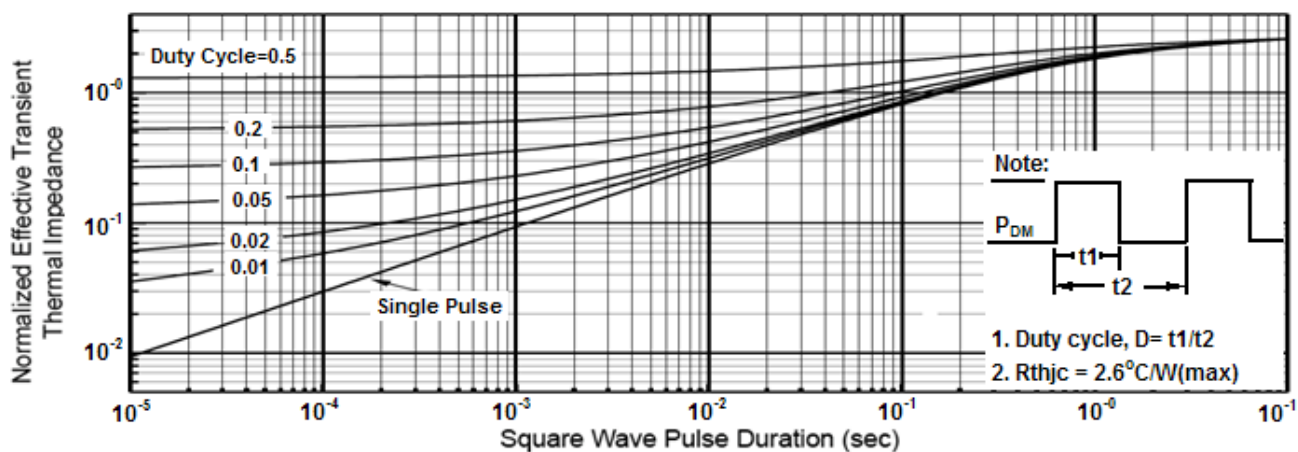
CHARACTERISTICS CURVES

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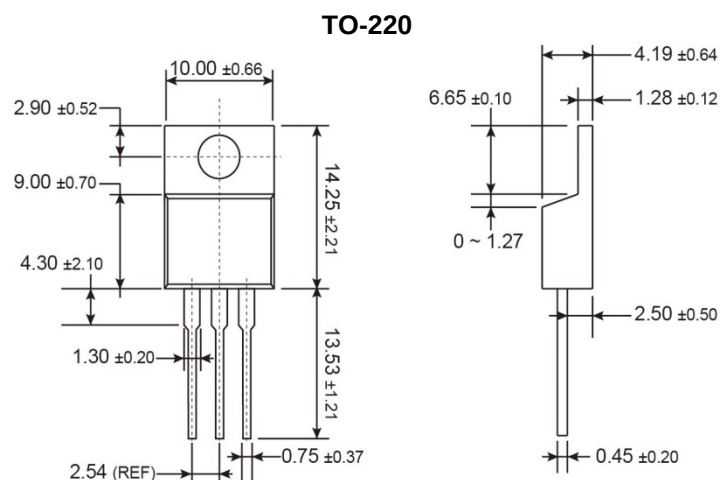
Normalized Thermal Transient Impedance, Junction-to-Ambient



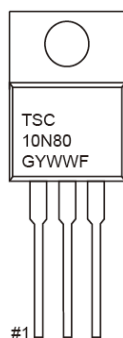
Normalized Thermal Transient Impedance, Junction-to-Ambient(ITO-220)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

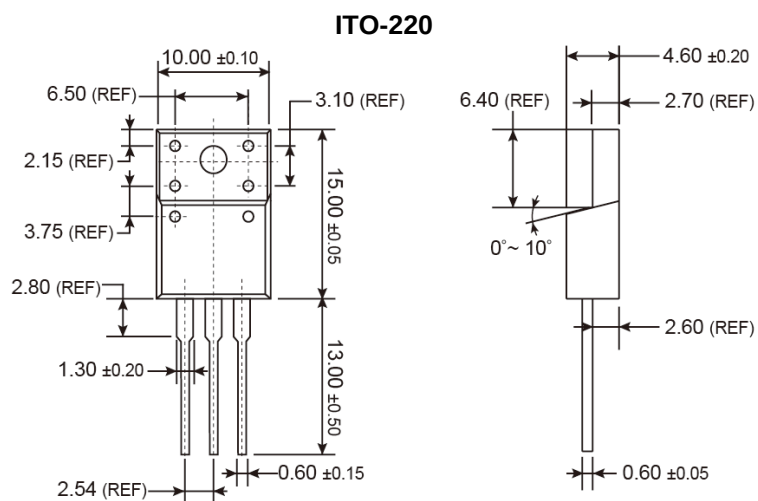


MARKING DIAGRAM

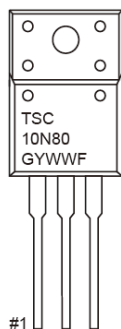


- G** = Halogen Free Product
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



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