

# DATA SHEET

Part No.	MN88441
Package Code No.	LQFP128-P-1818C

SEMICONDUCTOR COMPANY  
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

# MN88441

## OFDM Demodulation LSI for Digital Terrestrial Broadcasting in Japan

### ■ Overview

This LSI is a channel decoder LSI supporting ISDB-T/ISDB-T<sub>SB</sub>.

Widely used for digital terrestrial broadcasting receiver equipment that takes advantage of UHF and VHF frequency bands in Japan.

This LSI performs the following operations:

- IF signal input
- OFDM<sup>\*1</sup> demodulation
- Error correction
- TSP<sup>\*2</sup> output

\*1 Orthogonal Frequency Division Multiplexing

\*2 Transport Stream Packet

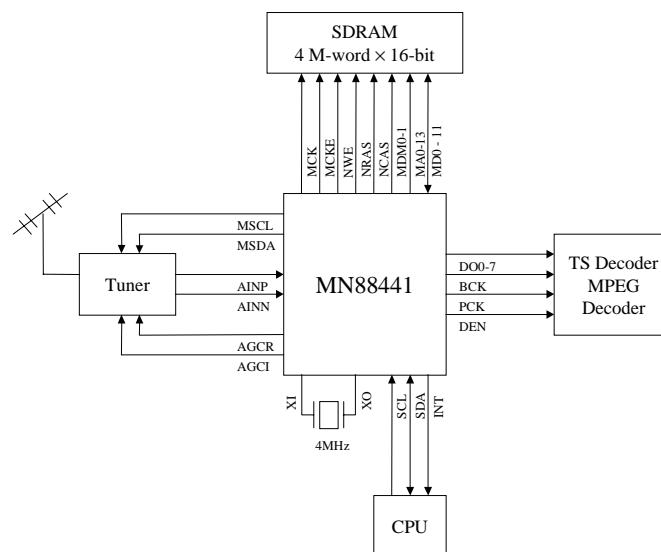
### ■ Features

- Supports digital terrestrial broadcasting (ISDB-T) and Digital terrestrial sound broadcasting (ISDB-T<sub>SB</sub>)
- Strong suppression of co-channel interference with analog broadcasting signal
- AGC with 2 output signals (PWM output)
- On-chip CPU/IF circuits compliant with I2C bus
- On-chip ADC for input signal
- On-chip boundary scan test circuits compliant with IEEE1149.1

### ■ Applications

- Set-top box for digital terrestrial broadcasting
- TV with receiving function for digital terrestrial broadcasting
- DVHS with receiving function for digital terrestrial broadcasting

### ■ System structure block diagram

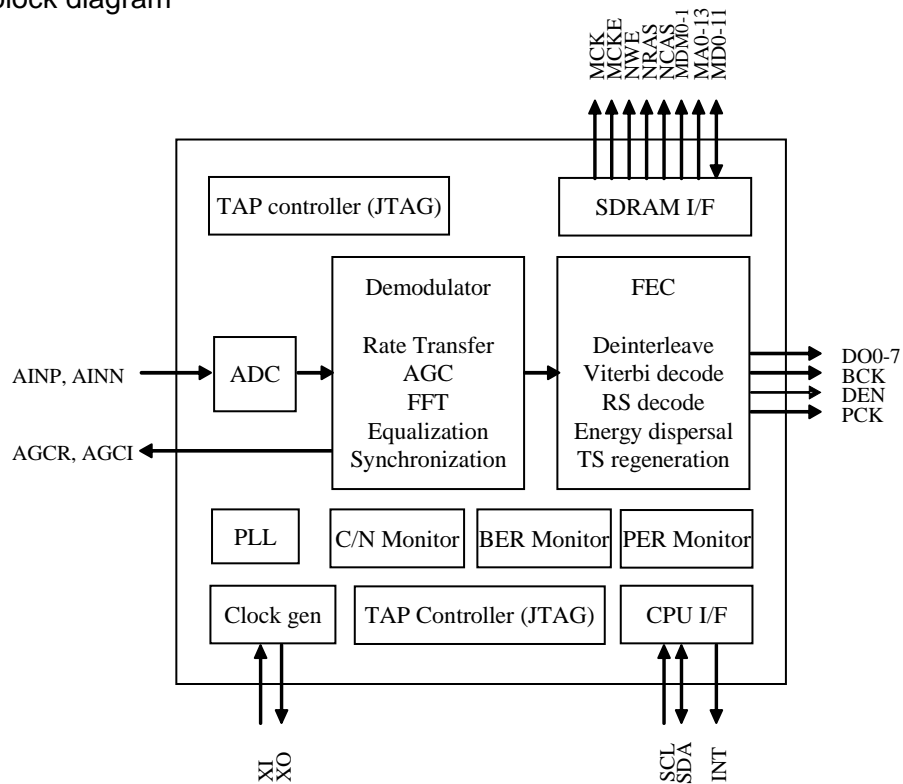


Note : The detailed information for this product is disclosed after non-disclosure agreement between your company and MEI.

## ■ LSI specifications

Modulation	Transmission mode:	Mode1, Mode2, Mode3
	Guard interval duration:	1/32, 1/16, 1/8, 1/4
	Carrier modulation:	DQPSK, QPSK, 16QAM, 64QAM
	Coding rate:	1/2, 2/3, 3/4, 5/6, 7/8
IF Input	Center frequency:	4.063 MHz
TSP output		Parallel or serial (alternative)
BER measurement output		Serial (Output from TSP pin with alternative Viterbi decode out or RS decode out)
Clock	PLL reference frequency:	4 MHz (Self-excited or clock input alternative)
	Master clock frequency:	40 MHz
CPU Interface		Compliant with standard I2C bus mode Tuner control with I2C format
External memory		64 M-bit, 128 M-bit, 256 M-bit SDRAM (larger than 4 M-word × 16-bit)
Supply voltage	For external I/F:	3.3 V
	For internal section:	1.8 V
Input voltage		3.3 V (LVTTL)
Output voltage		3.3 V (LVCMOS)
Package		128-pin LQFP (□ 18 mm, 0.5 mm pitch)

■ LSI block diagram



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