# 300-mA Low-Noise LDO Regulator With Error Flag and Discharge Option

## FEATURES

- Ultra Low Dropout—300 mV at 300-mA Load
- Low Noise—75 $\mu V_{RMS}$ (10-Hz to 100-kHz)
- Out-of-Regulation Error Flag (power good)
- Shutdown Control
- 130-μA Ground Current at 300-mA Load
- Fast Start-Up (50 μS)
- 1.5% Guaranteed Output Voltage Accuracy
- 400-mA Peak Output Current Capability
- Uses Low ESR Ceramic Capacitors
- Fast Line and Load Transient Response (≤ 30 μs)
- 1-μA Maximum Shutdown Current
- Output Current Limit
- Reverse Battery Protection
- Built-in Short Circuit and Thermal Protection

Pb-free Available

- Output—Auto-Discharge In Shutdown Mode
- Fixed 1.2, 1.8, 2.5, 2.6, 2.8, 3.0, 3.3, 5.0-V Output Voltage Options
- MLP33-5 PowerPAK® Package

## APPLICATIONS

- Cellular Phones, Wireless Handsets
- Noise-Sensitive Electronic Systems, Laptop and Palmtop Computers
- PDAs
- Pagers
- Digital Cameras
- MP3 Player
- Wireless Modem

## DESCRIPTION

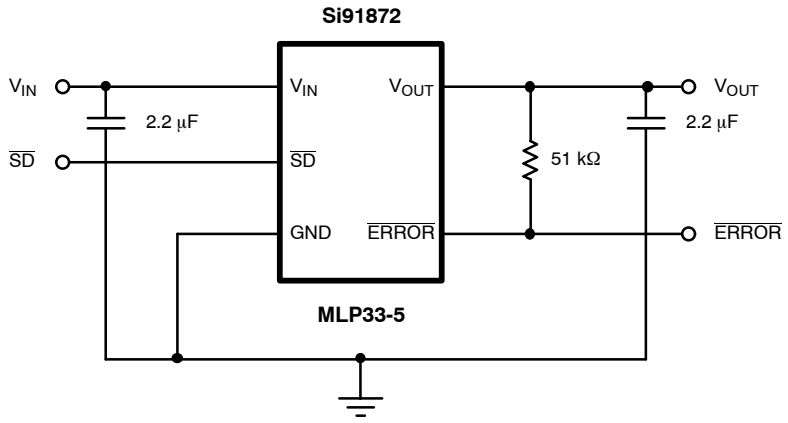
The Si91872 is a 300-mA CMOS LDO (low dropout) voltage regulator. It is the perfect choice for low voltage, low power applications. An ultra low ground current and ultra fast turn-on make this part attractive for battery operated power systems. The Si91872 also offers ultra low dropout voltage to prolong battery life in portable electronics. Systems requiring a quiet voltage source will benefit from the Si91872's low output noise. The Si91872 is designed to maintain regulation while delivering 400-mA peak current, making it ideal for systems that have a high surge current upon turn-on.

For better transient response and regulation, an active pull-down circuit is built into the Si91872 to clamp the output voltage when it rises beyond normal regulation. The Si91872 automatically discharges the output voltage by connecting the output to ground through a 100-Ω n-channel MOSFET when the device is put in shutdown mode.

The Si91872 features reverse battery protection to limit reverse current flow to approximately 1-μA in the event reversed battery is applied at the input, thus preventing damage to the IC.

The Si91872 is available in both the standard and lead (Pb)-free 5-pin MLP33 PowerPAK packages and is specified to operate over the industrial temperature range of –40°C to 85°.

## TYPICAL APPLICATION CIRCUIT



## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings
Input Voltage, $V_{IN}$ to GND . . . . . –6.0 to 6.5 V
$V_{\overline{ERROR}}$, $V_{\overline{SD}}$ (See Detailed Description) . . . . . –0.3 V to $V_{IN}$
Output Current, $I_{OUT}$ . . . . . Short Circuit Protected
Output Voltage, $V_{OUT}$ . . . . . –0.3 V to $V_{IN}$ + 0.3 V
Package Power Dissipation, $(P_d)^b$ . . . . . 2.3 W

Thermal Resistance $(\theta_{JA})^a$ . . . . . 55°C/W
$R_{(\theta JA)}{}^a$ . . . . . 8°C/W
Maximum Junction Temperature, $T_{J(max)}$ . . . . . 150°C
Storage Temperature, $T_{STG}$ . . . . . –65°C to 150°C
Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 20 mW/°C above $T_A$ = 25°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## RECOMMENDED OPERATING RANGE

Input Voltage, $V_{IN}$ . . . . . 2 V to 6 V
Input Voltage, $V_{\overline{SD}}$ . . . . . 0 V to $V_{IN}$
Output Current . . . . . 0 to 300 mA
$C_{IN}$, $C_{OUT}{}^a$ (Ceramic) . . . . . 2.2 µF

Operating Ambient Temperature, $T_A$ . . . . . –40°C to 85°C
Operating Junction Temperature, $T_J$ . . . . . –40°C to 125°C
Notes
a. Maximum ESR of $C_{OUT:}$ 0.2 Ω.

## SPECIFICATIONS

| Parameter | Symbol | Test Conditions Unless Specified<br>$T_A$ = 25°C, $V_{IN} = V_{OUT(nom)}$ + 1 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 2 µF, $C_{OUT}$ = 2.0 µF, $V_{\overline{SD}}$ = 1.5 V | | Temp[a] | Limits –40 to 85°C Min[b] | Typ[c] | Max[b] | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Input Voltage Range | $V_{IN}$ | | | Full | 2 | | 6 | V |
| Output Voltage Accuracy | | 1 mA ≤ $I_{OUT}$ ≤ 300 mA | $V_{OUT}$ ≥ 1.8 V | Room | –2.0 | 1 | 2.0 | % |
| | | | | Full | –3.0 | 1 | 3.0 | |
| | | | $V_{OUT}$ = 1.2 V, 1.5 V | Room | –2.5 | 1 | 2.5 | |
| | | | | Full | –3.5 | 1 | 3.5 | |
| Line Regulation ($V_{OUT}$ ≤ 3 V) | $\frac{\Delta V_{OUT} \times 100}{\Delta V_{IN} \times V_{OUT(nom)}}$ | From $V_{IN} = V_{OUT(nom)}$ + 1 V to $V_{OUT(nom)}$ + 2 V | | Full | –0.06 | | 0.18 | %/V |
| Line Regulation (3.0 V < $V_{OUT}$ ≤ 3.6 V) | | | | Full | 0 | | 0.3 | |
| Line Regulation (5-V Version) | | From $V_{IN}$ = 5.5 V to 6 V | | Full | 0 | | 0.4 | |
| Dropout Voltage[d, g] ($V_{OUT(nom)}$ ≥ 2.6 V) | $V_{IN} - V_{OUT}$ | $I_{OUT}$ = 1 mA | | Room | | 1 | | mV |
| | | $I_{OUT}$ = 50 mA | | Room | | 45 | 80 | |
| | | | | Full | | 50 | 90 | |
| | | $I_{OUT}$ = 300 mA | | Room | | 300 | 350 | |
| | | | | Full | | | 415 | |
| Dropout Voltage[d, g] ($V_{OUT(nom)}$ < 2.6 V, $V_{IN}$ ≥ 2 V) | | $I_{OUT}$ = 50 mA | | Room | | 65 | 100 | |
| | | | | Full | | | 120 | |
| | | $I_{OUT}$ = 300 mA | | Room | | 400 | 520 | |
| | | | | Full | | | 570 | |
| Ground Pin Current[e, g] ($V_{OUT(nom)}$ ≤ 3 V) | $I_{GND}$ | $I_{OUT}$ = 0 mA | | Room | | 100 | 150 | µA |
| | | | | Full | | | 180 | |
| | | $I_{OUT}$ = 300 mA | | Room | | 130 | 200 | |
| | | | | Full | | | 330 | |
| Ground Pin Current[e, g] ($V_{OUT(nom)}$ > 3 V) | | $I_{OUT}$ = 0 mA | | Room | | 110 | 170 | |
| | | | | Full | | | 200 | |
| | | $I_{OUT}$ = 300 mA | | Room | | 150 | 225 | |
| | | | | Full | | | 275 | |
| Peak Output current | $I_{O(peak)}$ | $V_{OUT}$ ≥ 0.95 x $V_{OUT(nom)}$. $t_{PW}$ = 2 ms | | Full | 400 | | | mA |
| Output Noise Voltage | $e_N$ | $V_{OUT}$ = 2.6 V, BW = 10 Hz to 100 kHz, 0 mA < $I_{OUT}$ < 150 mA | | Room | | 75 | | µV(rms) |

## SPECIFICATIONS

| Parameter | Symbol | Test Conditions Unless Specified $T_A$ = 25°C, $V_{IN} = V_{OUT(nom)}$ + 1 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 2 µF, $C_{OUT}$ = 2.0 µF, $V_{\overline{SD}}$ = 1.5 V | | Temp[a] | Limits −40 to 85°C Min[b] | Typ[c] | Max[b] | Unit |
|---|---|---|---|---|---|---|---|---|
| Ripple Rejection | $\Delta V_{OUT}/\Delta V_{IN}$ | $I_{OUT}$ = 300 mA | f = 1 kHz | Room | | 60 | | dB |
| | | | f = 10 kHz | Room | | 40 | | |
| | | | f = 100 kHz | Room | | 30 | | |
| Dynamic Line Regulation | $\Delta V_{O(line)}$ | $V_{IN}$ : $V_{OUT(nom)}$ + 1 V to $V_{OUT(nom)}$ + 2 V, $t_r/t_f$ = 2 µs, $I_{OUT}$ = 300 mA | | Room | | 20 | | mV |
| Dynamic Load Regulation | $\Delta V_{O(load)}$ | $I_{OUT}$ : 1 mA to 300 mA, $t_r/t_f$ = 2 µs | | Room | | 25 | | |
| Thermal Shutdown Junction Temperature | $T_{J(S/D)}$ | | | Room | | 150 | | °C |
| Thermal Hysteresis | $T_{HYST}$ | | | Room | | 20 | | |
| Reverse current | $I_R$ | $V_{IN}$ = −6.0 V | | Room | | 1 | | µA |
| Short Circuit Current | $I_{SC}$ | $V_{OUT}$ = 0 V | | Room | | 700 | | mA |
| **Shutdown** | | | | | | | | |
| Shutdown Supply Current | $I_{CC(off)}$ | $V_{\overline{SD}}$ = 0 V | | Room | | 0.1 | 1 | µA |
| $\overline{SD}$ Pin Input Voltage | $V_{\overline{SD}}$ | High = Regulator ON (Rising) | | Full | 1.5 | | $V_{IN}$ | V |
| | | Low = Regulator OFF (Falling) | | Full | | | 0.4 | |
| Auto Discharge Resistance | R_DIS | Si91872 Only | | Room | | 100 | | Ω |
| $\overline{SD}$ Pin Input Current[f] | $I_{IN(\overline{SD})}$ | $V_{\overline{SD}}$ = 1.5 V, $V_{IN}$ = 6 V | | Room | | 0.7 | | µA |
| $\overline{SD}$ Hysteresis | $V_{HYST(\overline{SD})}$ | | | Full | | 150 | | mV |
| $V_{OUT}$ Turn-On Time | $t_{ON}$ | $V_{\overline{SD}}$ (See Figure 1), $I_{LOAD}$ = 100 mA | | Room | | 50 | | µs |
| **ERROR Output** | | | | | | | | |
| $\overline{ERROR}$ High Leakage | $I_{OFF}$ | $\overline{ERROR} \le V_{IN}$. $V_{OUT}$ in Regulation | | Full | | | 1 | µA |
| $\overline{ERROR}$ Low Voltage | $V_{OL}$ | $I_{SINK}$ = 0.5 mA | | Full | | | 0.4 | V |
| $\overline{ERROR}$ Voltage Threshold | $V_{\overline{ERROR}}$ | $V_{OUT}$ Below $V_{OUT(nom)}$[g], $V_{IN} \ge$ 2 V<br>$V_{OUT}$ Falling, $I_{OUT}$ = 1 mA, $V_{OUT(nom)} \ge$ 2 V | | Full | −2 | −4 | −6 | % |
| | | $V_{OUT(nom)}$[g] < 2 V, $V_{IN}$ > 2 V | | Full | | −4 | | |
| $\overline{ERROR}$ Voltage Threshold Hysteresis | $V_{HYST(\overline{ERROR})}$ | | | Room | | 1.5 | | |

Notes
a. Room = 25°C, Full = −40 to 85°C.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 2% below the output voltage measured with a 1-V differential, provided that $V_{IN}$ does not not drop below 2.0 V.
e. Ground current is specified for normal operation as well as “drop-out” operation.
f. The device’s shutdown pin includes a typical 2-MΩ internal pull-down resistor connected to ground.
g. $V_{OUT(nom)}$ is $V_{OUT}$ when measured with a 1-V differential to $V_{IN}$.

## TIMING WAVEFORMS

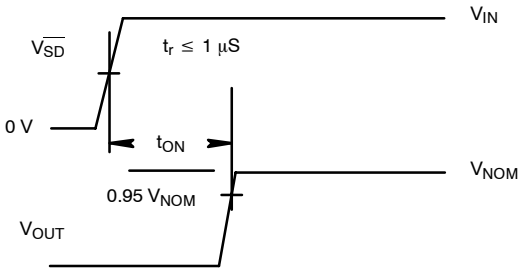



**FIGURE 1.** Timing Diagram for Power-Up

## PIN CONFIGURATION: MLP33-5

**MLP33-5 PowerPAK**

## PIN DESCRIPTION

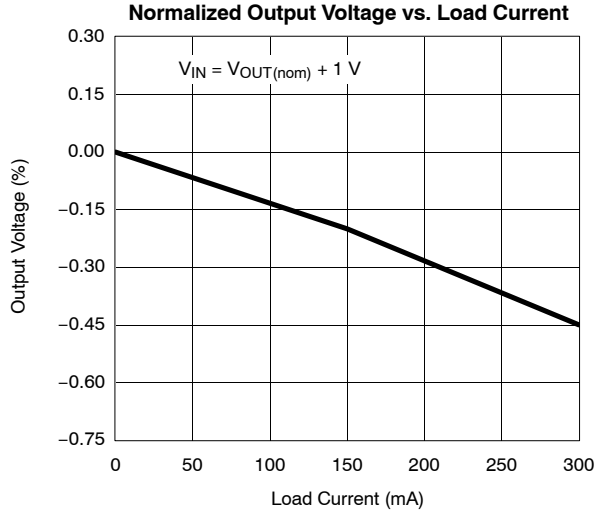
| Pin Number | Name | Function |
|---|---|---|
| 1 | $\overline{SD}$ | By applying less than 0.4 V to this pin, the device will be turned off. Connect this pin to $V_{IN}$ if unused |
| 2 | $\overline{ERROR}$ | The open drain output is an error flag output which goes low when $V_{OUT}$ drops 4% below its nominal voltage. |
| 3 | $V_{IN}$ | Input supply pin. Bypass this pin with a 1-µF ceramic or tantalum capacitor to ground |
| 4 | $V_{OUT}$ | Output voltage. Connect $C_{OUT}$ between this pin and ground. |
| 5 | GND | Ground pin. For better thermal capability, directly connected to large ground plane |

## ORDERING INFORMATION

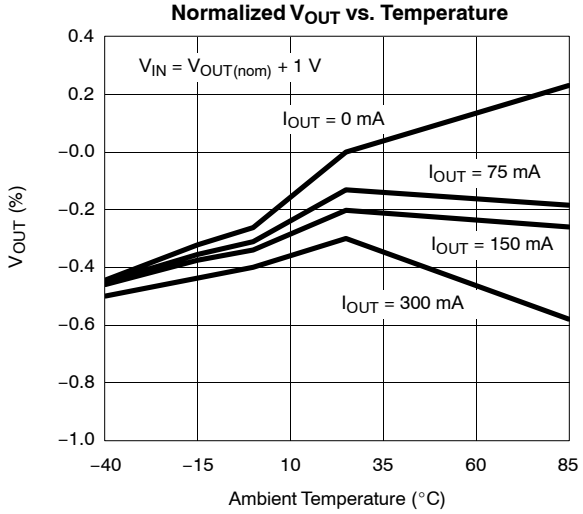
| Standard Part Number | Lead (Pb)-Free Part Number | Marking | Voltage | Temp. Range | Pkg. |
|---|---|---|---|---|---|
| Si91872DMP-12-T1 | Si91872DMP-12-E3 | 7212 | 1.2 | −40 to 85°C | MLP33-5 |
| Si91872DMP-18-T1 | Si91872DMP-18-E3 | 7218 | 1.8 | | |
| Si91872DMP-25-T1 | Si91872DMP-25-E3 | 7225 | 2.5 | | |
| Si91872DMP-26-T1 | Si91872DMP-26-E3 | 7226 | 2.6 | | |
| Si91872DMP-28-T1 | Si91872DMP-28-E3 | 7228 | 2.8 | | |
| Si91872DMP-30-T1 | Si91872DMP-30-E3 | 7230 | 3.0 | | |
| Si91872DMP-33-T1 | Si91872DMP-33-E3 | 7233 | 3.3 | | |
| Si91872DMP-50-T1 | Si91872DMP-50-E3 | 7250 | 5.0 | | |

## TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)

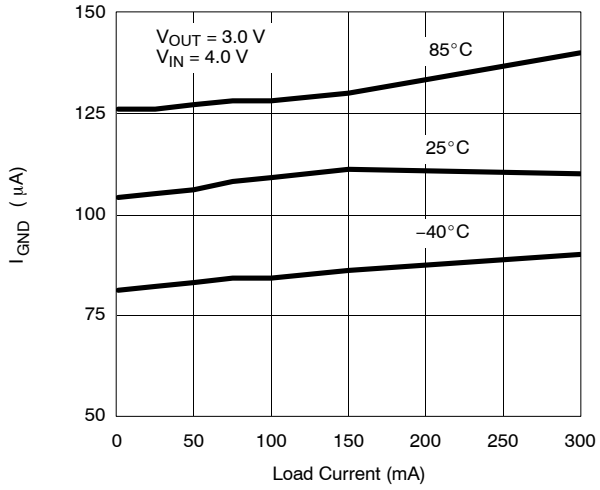
**Normalized Output Voltage vs. Load Current**



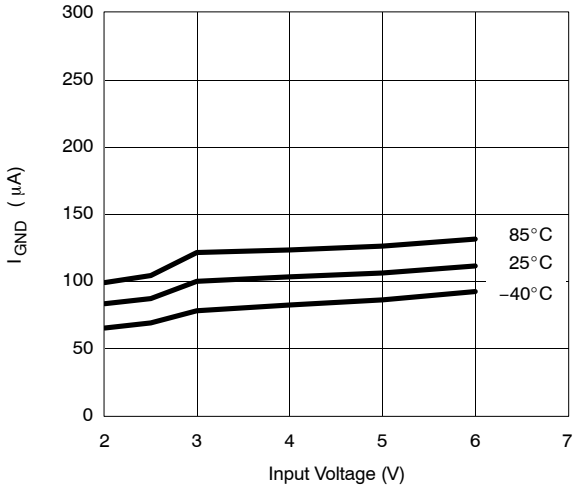

**Normalized $V_{OUT}$ vs. Temperature**



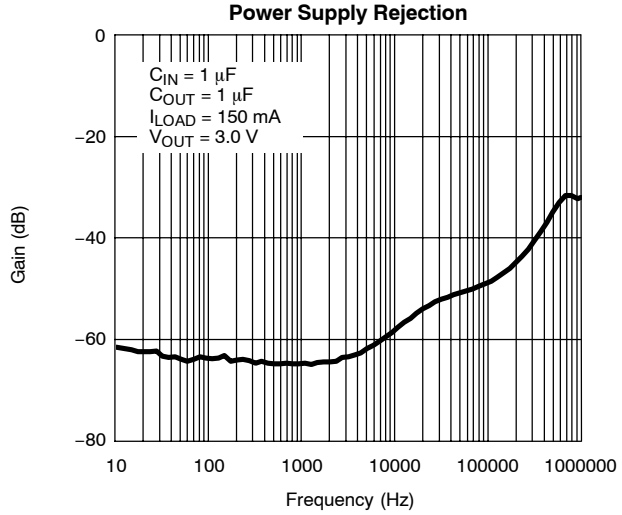

**GND Current vs. Load Current**



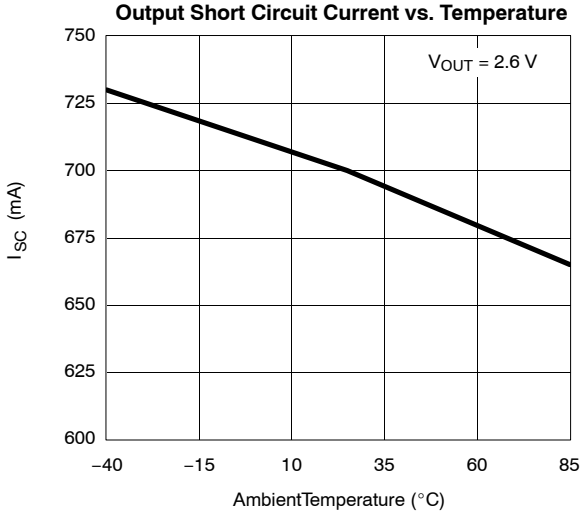

**No Load GND Pin Current vs. Input Voltage**




**Power Supply Rejection**

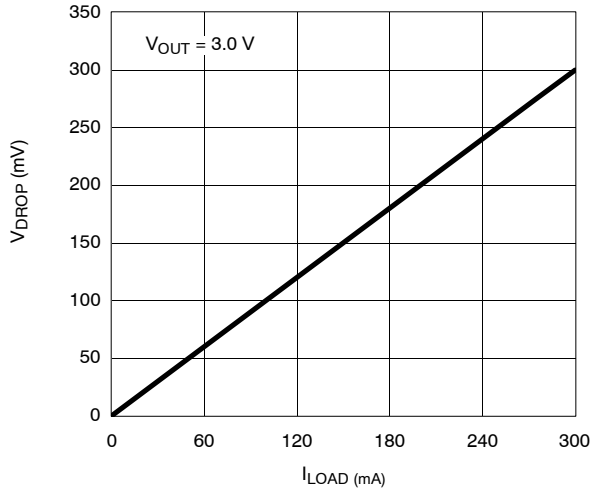



**Output Short Circuit Current vs. Temperature**

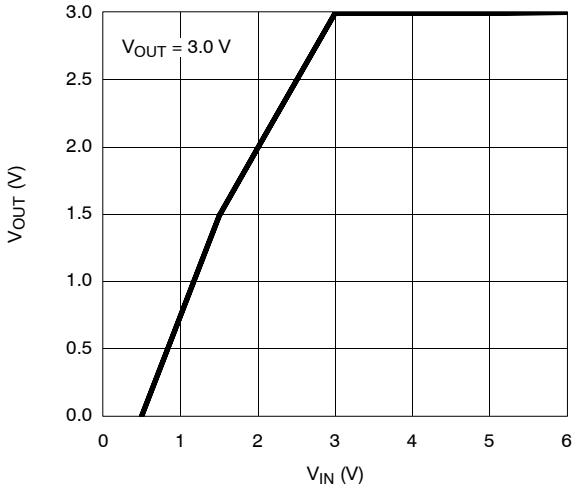


## TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)

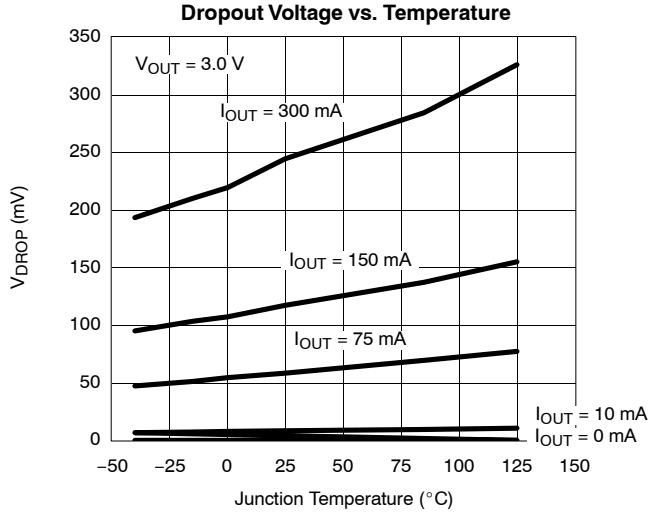
**Dropout Voltage vs. Load Current**



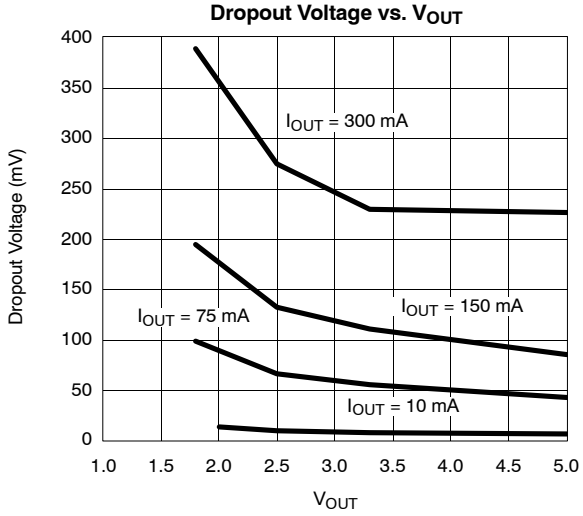

**$V_{IN}$ – $V_{OUT}$ Transfer Characteristic**




**Dropout Voltage vs. Temperature**

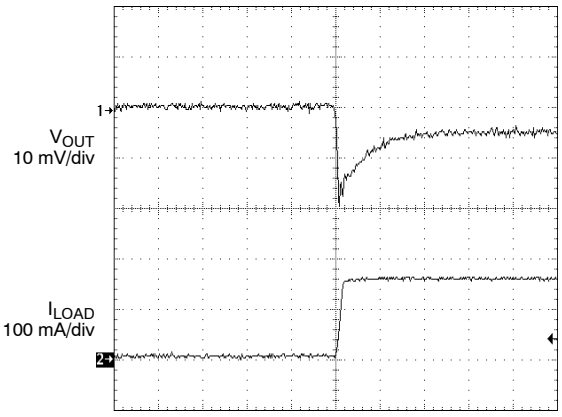



**Dropout Voltage vs. $V_{OUT}$**



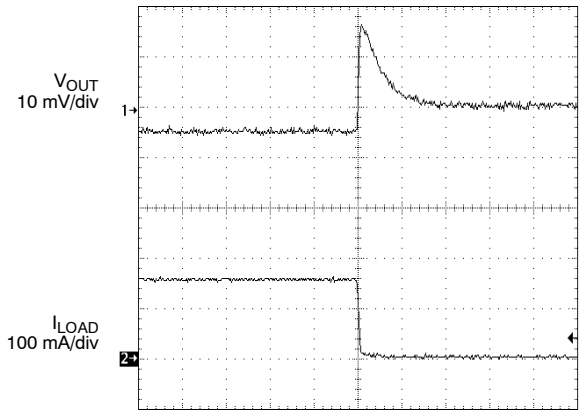
## TYPICAL WAVEFORMS

**Load Transient Response-1**



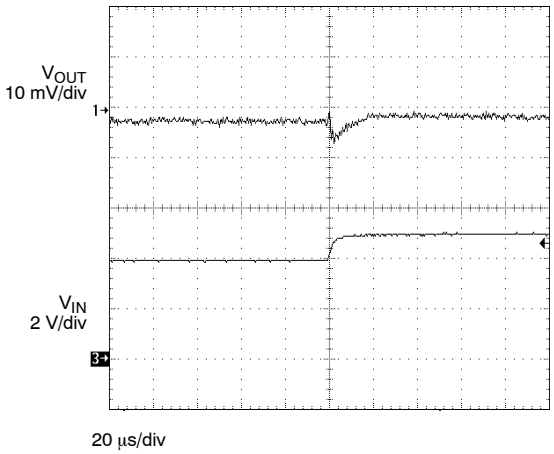

$V_{OUT}$ = 3.0 V
$C_{OUT}$ = 1 µF
$I_{LOAD}$ = 1 to 150 mA
$t_{rise}$ = 2 µsec

**Load Transient Response-2**



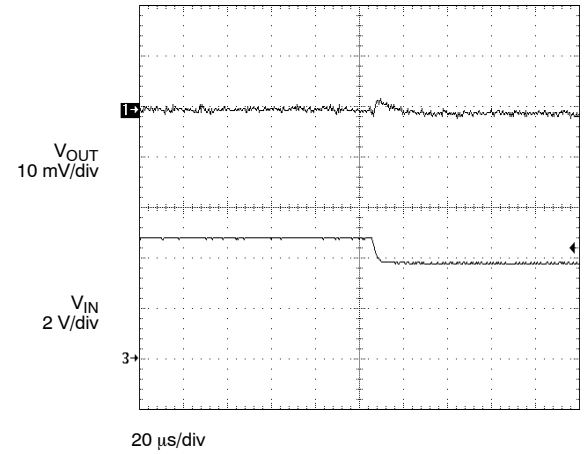

$V_{OUT}$ = 3.0 V
$C_{OUT}$ = 1 µF
$I_{LOAD}$ = 150 to 1 mA
$t_{fall}$ = 2 µsec

**LineTransient Response-1**




$V_{INSTEP}$ = 4 to 5 V
$V_{OUT}$ = 3 V
$C_{OUT}$ = 1 µF
$C_{IN}$ = 1 µF
$I_{LOAD}$ = 150 mA
$t_{rise}$ = 5 µsec

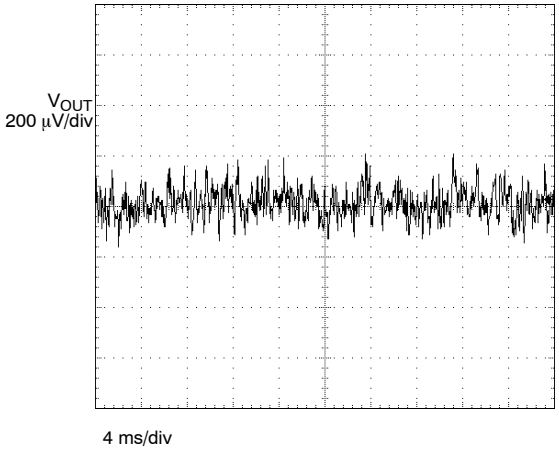
**LineTransient Respons-2**




$V_{INSTEP}$ = 5 to 4 V
$V_{OUT}$ = 3 V
$C_{OUT}$ = 1 µF
$C_{IN}$ = 1 µF
$I_{LOAD}$ = 150 mA
$t_{fall}$ = 5 µsec

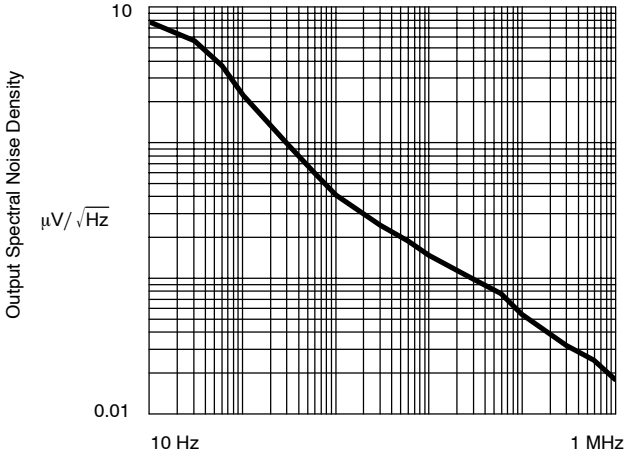
## TYPICAL WAVEFORMS

**Output Noise**



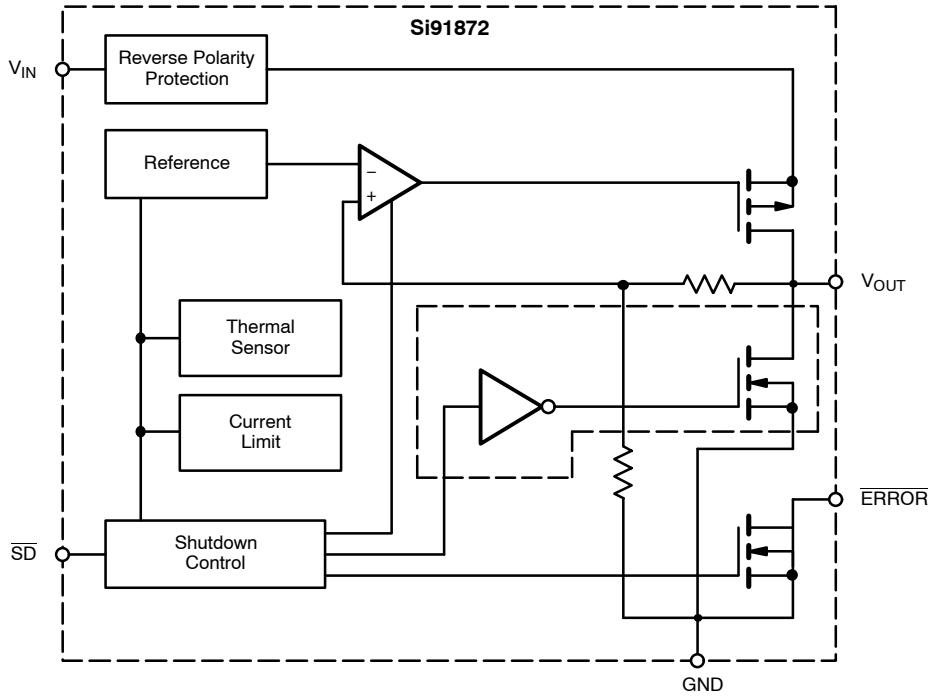

$V_{IN}$ = 4 V
$V_{OUT}$ = 3 V
$I_{OUT}$ = 150 mA
BW = 10 Hz to 100 kHz

**Noise Spectrum**




$V_{IN}$ = 4 V
$V_{OUT}$ = 3 V
$I_{LOAD}$ = 150 mA

## FUNCTIONAL BLOCK DIAGRAM



## DETAILED DESCRIPTION

The Si91872 is a low-noise, low drop-out and low quiescent current linear voltage regulator, packaged in a small footprint MLP33-5 package. The Si91872 can supply loads up to 300 mA. As shown in the block diagram, the circuit consists of a bandgap reference, error amplifier, p-channel pass transistor and feedback resistor string. Additional blocks, not shown in the block diagram, include a precise current limiter, reverse battery and current protection, and thermal sensor.

### Thermal Overload Protection

The thermal overload protection limits the total power dissipation and protects the device from being damaged. When the junction temperature exceeds 150°C, the device turns the p-channel pass transistor off.

### Reverse Battery Protection

The Si91872 has a battery reverse protection circuitry that disconnects the internal circuitry when $V_{IN}$ drops below the GND voltage. There is no current drawn in such an event. When the $\overline{SD}$ pin is hardwired to $V_{IN}$, the user must connect the $\overline{SD}$ pin to $V_{IN}$ via a 100-kΩ resistor if reverse battery protection is desired. Hardwiring the $\overline{SD}$ pin directly to the $V_{IN}$ pin is allowed when reverse battery protection is not desired.

### $\overline{ERROR}$

$\overline{ERROR}$ is an open drain output that goes low when $V_{OUT}$ is less than 4% of its normal value. To obtain a logic level output, connect a pull-up resister from $\overline{ERROR}$ to $V_{OUT}$ or any other voltage equal to or less than $V_{IN}$. $\overline{ERROR}$ pin is high impedance (off) when $\overline{SD}$ pin is low.

### Auto-Discharge

$V_{OUT}$ has an internal 100-Ω (typ.) discharge path to ground when $\overline{SD}$ pin is low for the Si91872.

### Stability

The circuit is stable with only a small output capacitor equal to 6 nF/mA (= 2 µF @ 300 mA). Since the bandwidth of the error amplifier is around 1–3 MHz and the dominant pole is at the output node, the capacitor should be capacitive in this range, i.e., for 150-mA load current, an ESR <0.2 Ω is necessary. Parasitic inductance of about 10 nH can be tolerated.

### Safe Operating Area

The ability of the Si91872 to supply current is ultimately dependent on the junction temperature of the pass device. Junction temperature is in turn dependent on power dissipation in the pass device, the thermal resistance of the package and the circuit board, and the ambient temperature. The power dissipation is defined as

$$P_D = (V_{IN} - V_{OUT}) * I_{OUT}.$$

Junction temperature is defined as

$$T_J = T_A + ((P_D * (R\theta_{JC} + R\theta_{CA})).$$

To calculate the limits of performance, these equations must be rewritten.

Allowable power dissipation is calculated using the equation

$$P_D = (T_J - T_A)/ (R\theta_{JC} + R\theta_{CA})$$

While allowable output current is calculated using the equation

$$I_{OUT} = (T_J - T_A)/ (R\theta_{JC} + R\theta_{CA}) * (V_{IN} - V_{OUT}).$$

Ratings of the Si91872 that must be observed are

$T_{Jmax}$ = 125 °C, $T_{Amax}$ = 85 °C, $(V_{IN} - V_{OUT})_{max}$ = 5.3 V, $R\theta_{JC}$ = 8 °C/W.

The value of $R\theta_{CA}$ is dependent on the PC board used. The value of $R\theta_{CA}$ for the board used in device characterization is approximately 46 °C/W.

Figure 1 shows the performance limits graphically for the Si91872 mounted on the circuit board used for thermal characterization.

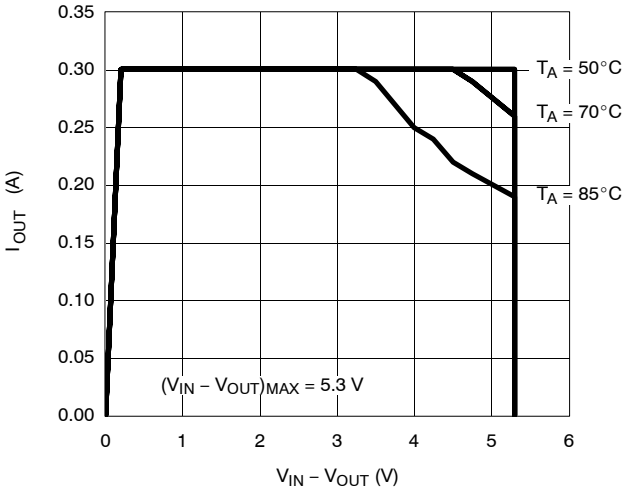



**Figure 1.** Safe Operating Area

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