

# DS4000 Digitally Controlled TCXO

[www.maxim-ic.com](http://www.maxim-ic.com)

## GENERAL DESCRIPTION

The DS4000 digitally controlled temperature-compensated crystal oscillator (DC-TCXO) features a digital temperature sensor, one fixed-frequency temperature-compensated square-wave output ( $F_1$ ), one programmable temperature-compensated square-wave output ( $F_2$ ), and digital communication for frequency tuning (SDA, SCL).

## APPLICATIONS

Reference Oscillators in PLL Circuits  
Global Positioning Systems  
SATCOM  
Telecom  
Wireless Base Stations

## ORDERING INFORMATION

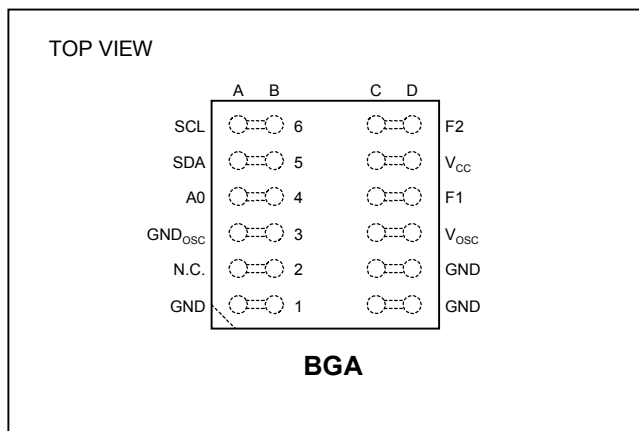
| PART    | TEMP RANGE     | PIN-PACKAGE |
|---------|----------------|-------------|
| DS4000  | 0°C to +70°C   | 24 BGA      |
| DS4000N | -40°C to +85°C | 24 BGA      |

Selector Guide appears end of data sheet.

## FEATURES

- Aging  $\leq 1.0$ ppm (First Year)
- Frequency Stability  $\pm 1.0$ ppm from -40°C to +85°C
- Frequency Versus Supply Stability of  $\pm 1.0$ ppm per Volt
  - Base Frequency is Digitally Tunable by  $\pm 10$ ppm
  - One Fixed-Frequency Output and One (n + 1) or 2(n + 1) Division of the Base Frequency Output
- Temperature Measurements from -40°C to +85°C with 10-Bit/ $\pm 0.25^\circ\text{C}$  Resolution and  $\pm 3^\circ\text{C}$  Accuracy
- 2-Wire Serial Interface

## PIN CONFIGURATION



**Note:** Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: [www.maxim-ic.com/errata](http://www.maxim-ic.com/errata).

## ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground

-0.3V to +6.0V

Storage Temperature Range

-55°C to +85°C

Operating Voltage Range

 $V_{CC} = 5V \pm 5\%$ 

Operating Temperature Range

Commercial

0°C to +70°C

Industrial

-40°C to +85°C

Soldering Temperature

See IPC/JEDEC J-STD-020A (2x max)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

## RECOMMENDED DC OPERATING CONDITIONS

(V<sub>CC</sub> = 5V ±5%, over the operating temperature range.)

| PARAMETER                 | SYMBOL           | CONDITIONS   | MIN  | TYP | MAX                   | UNITS |
|---------------------------|------------------|--------------|------|-----|-----------------------|-------|
| Supply Voltage            | V <sub>CC</sub>  | (Notes 1, 2) | 4.75 | 5.0 | 5.25                  | V     |
| Oscillator Supply Voltage | V <sub>OSC</sub> | (Notes 1, 2) | 4.75 | 5.0 | 5.25                  | V     |
| Input Logic High          | V <sub>IH</sub>  | (Note 1)     | 2.2  |     | V <sub>CC</sub> + 0.3 | V     |
| Input Logic Low           | V <sub>IL</sub>  | (Note 1)     | -0.3 |     | +0.8                  | V     |

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 5V ±5%, over the operating temperature range.)

| PARAMETER                        | SYMBOL             | CONDITIONS   | MIN | TYP | MAX | UNITS |
|----------------------------------|--------------------|--------------|-----|-----|-----|-------|
| Active Supply Current            | I <sub>CC</sub>    | (Notes 3, 4) |     | 1.5 | 2   | mA    |
| Active Oscillator Supply Current | I <sub>OSC</sub>   | (Notes 3, 4) |     | 3.5 | 5.5 | mA    |
| Output Logic High 2.4V           | I <sub>OH</sub>    | (Note 1)     | -1  |     |     | mA    |
| Output Logic Low 0.4V            | I <sub>OL</sub>    | (Note 1)     |     |     | 4   | mA    |
| Input Leakage                    | I <sub>LI</sub>    |              |     |     | 1   | μA    |
| I/O Leakage                      | I <sub>LO</sub>    |              |     |     | 1   | μA    |
| Temperature Conversion Time      | t <sub>CONVT</sub> | (Note 3)     |     | 250 | 300 | ms    |

**Note 1:** All voltages are referenced to ground.

**Note 2:** For ±10% operating range, contact factory.

**Note 3:** Typical values are at +25°C and nominal supplies.

**Note 4:** These parameters are measured with the outputs disabled.

**AC ELECTRICAL CHARACTERISTICS: TCXO**(V<sub>CC</sub> = 5V ±5%, over the operating temperature range.)

| PARAMETER                                                      | SYMBOL                          | CONDITIONS    | MIN  | TYP  | MAX  | UNITS  |
|----------------------------------------------------------------|---------------------------------|---------------|------|------|------|--------|
| Output Frequency                                               | F <sub>1</sub>                  | CMOS (Note 5) | 10   |      | 20   | MHz    |
|                                                                | F <sub>2</sub>                  |               |      |      |      |        |
| Frequency Stability vs. Temperature                            | ΔF/T <sub>A</sub>               |               | -1.0 |      | +1.0 | ppm    |
| Frequency Stability vs. Voltage                                | ΔF/V                            | (Note 6)      |      | ±1.0 |      | ppm/V  |
| Frequency Stability vs. Aging                                  | ΔF/Yr                           |               |      | ±1.0 |      | ppm/Yr |
| F <sub>1</sub> , F <sub>2</sub> Rise and Fall Time, 10% to 90% | t <sub>R</sub> , t <sub>F</sub> |               |      | 4    |      | ns     |
| Max Output Capacitive Load                                     | C <sub>L</sub>                  |               |      |      | 10   | pF     |
| Duty Cycle                                                     | t <sub>W</sub> / t              |               | 40   | 50   | 60   | %      |
| Phase Noise f1 Output (Note 7)                                 | φ <sub>N</sub>                  | 10Hz          |      | -85  |      | dBc/Hz |
|                                                                |                                 | 100Hz         |      | -115 |      |        |
|                                                                |                                 | 1kHz          |      | -129 |      |        |
|                                                                |                                 | 10kHz         |      | -134 |      |        |
|                                                                |                                 | 100kHz        |      | -139 |      |        |

**Note 5:** F<sub>1</sub> is the base frequency as defined by the package markings. F<sub>2</sub> is a programmable frequency output. The output frequency of F<sub>2</sub> is derived from the base frequency, F<sub>1</sub>, by programming the F<sub>2</sub> frequency select register and duty cycle (DC) bit in the TCXO control register. The minimum output frequency is F<sub>1</sub> / (2<sup>8</sup> + 1) with DC = 0 and f<sub>1</sub> / [2 × (2<sup>8</sup> + 1)] with DC = 1.

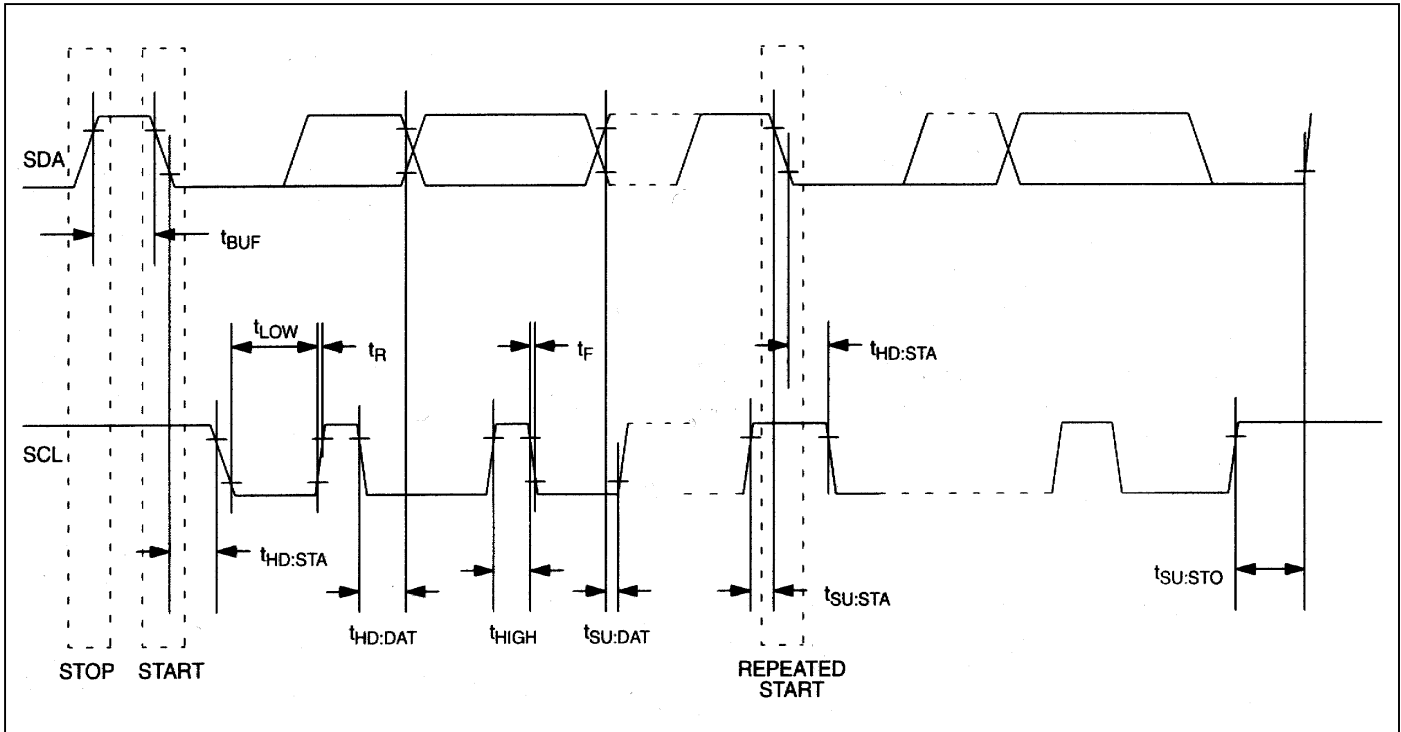
**Note 6:** First year typical.

**Note 7:** 16.384MHz, 5V, +25°C with one of the two outputs enabled.

**AC ELECTRICAL CHARACTERISTICS—2-WIRE SERIAL INTERFACE**(V<sub>CC</sub> = 4.75 to 5.25V, T<sub>A</sub> = -40°C to +85°C)

| PARAMETER                                        | SYMBOL              | CONDITION               | MIN                    | TYP | MAX  | UNITS |
|--------------------------------------------------|---------------------|-------------------------|------------------------|-----|------|-------|
| SCL Clock Frequency                              | f <sub>SCL</sub>    | Fast mode               | 0                      |     | 400  | kHz   |
|                                                  |                     | Standard mode           | 0                      |     | 100  |       |
| Bus Free Time Between a STOP and START Condition | t <sub>BUF</sub>    | Fast mode               | 1.3                    |     |      | μs    |
|                                                  |                     | Standard mode           | 4.7                    |     |      |       |
| Hold Time (Repeated) START Condition             | t <sub>HD:STA</sub> | Fast mode (Note 7)      | 0.6                    |     |      | μs    |
|                                                  |                     | Standard mode (Note 7)  | 4.0                    |     |      |       |
| Low Period of SCL Clock                          | t <sub>LOW</sub>    | Fast mode               | 1.3                    |     |      | μs    |
|                                                  |                     | Standard mode           | 4.7                    |     |      |       |
| High Period of SCL Clock                         | t <sub>HIGH</sub>   | Fast mode               | 0.6                    |     |      | μs    |
|                                                  |                     | Standard mode           | 4.0                    |     |      |       |
| Setup Time for a Repeated START Condition        | t <sub>SU:STA</sub> | Fast mode               | 0.6                    |     |      | μs    |
|                                                  |                     | Standard mode           | 4.7                    |     |      |       |
| Data Hold Time                                   | t <sub>HD:DAT</sub> | Fast mode (Note 8)      | 0                      |     | 0.9  | μs    |
|                                                  |                     | Standard mode (Note 8)  | 0                      |     | 0.9  |       |
| Data Setup Time                                  | t <sub>SU:DAT</sub> | Fast mode (Note 9)      | 100                    |     |      | ns    |
|                                                  |                     | Standard mode (Note 9)  | 250                    |     |      |       |
| Rise Time of Both SDA and SCL                    | t <sub>R</sub>      | Fast mode (Note 9)      | 20 + 0.1C <sub>B</sub> |     | 300  | ns    |
|                                                  |                     | Standard mode (Note 9)  | 20 + 0.1C <sub>B</sub> |     | 1000 |       |
| Fall Time of Both SDA and SCL                    | t <sub>F</sub>      | Fast mode (Note 10)     | 20 + 0.1C <sub>B</sub> |     | 300  | ns    |
|                                                  |                     | Standard mode (Note 10) | 20 + 0.1C <sub>B</sub> |     | 1000 |       |
| Setup Time for STOP Condition                    | t <sub>SU:STO</sub> | Fast mode               | 0.6                    |     |      | μs    |
|                                                  |                     | Standard mode           | 4.0                    |     |      |       |
| Capacitive Load for Each Bus Line                | C <sub>B</sub>      | (Note 10)               |                        |     | 400  | pF    |
| Input Capacitance                                | C <sub>I</sub>      |                         |                        | 5   |      | pF    |

**Note 7:** After this period, the first clock pulse is generated.**Note 8:** The maximum t<sub>HD:DAT</sub> has only to be met if the device does not stretch the LOW period (t<sub>LOW</sub>) of the SCL signal.**Note 9:** A fast-mode device can be used in a standard mode system, but the requirement t<sub>SU:DAT</sub> > 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t<sub>RMAX</sub> + t<sub>SU:DAT</sub> (1000 + 250 = 1250ns) before the SCL line is released.**Note 10:** C<sub>B</sub>: Total capacitance of one bus line in pF.

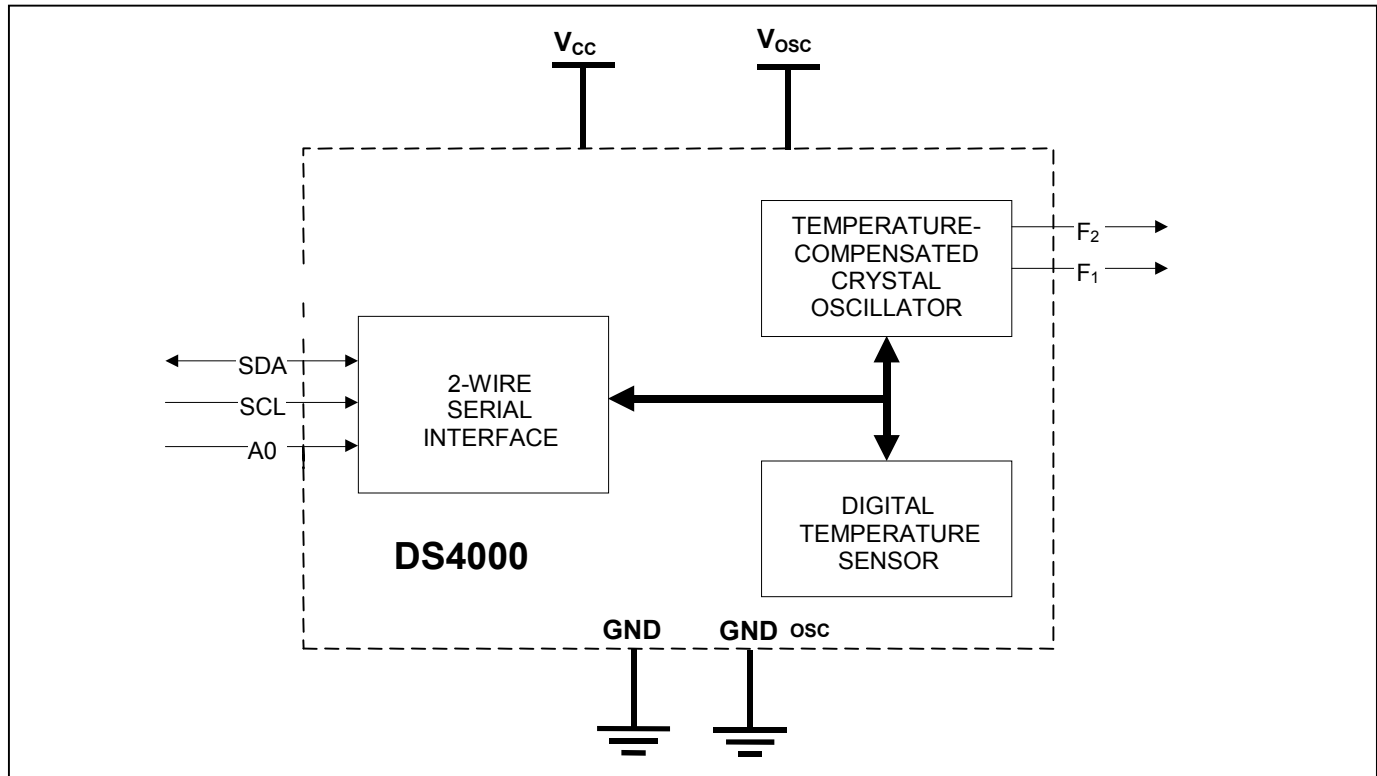
**Figure 1. Timing Diagram****PIN DESCRIPTION**

| PIN                       | NAME               | FUNCTION                                                                                                                                                          |
|---------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1A, 1B, 1C,<br>1D, 2C, 2D | GND                | Ground. DC power is provided to the device on these pins.                                                                                                         |
| 2A, 2B                    | N.C.               | No Connection. (Do not connect to ground.)                                                                                                                        |
| 3A, 3B                    | GND <sub>OSC</sub> | Oscillator Ground. DC power is provided to the oscillator on these pins.                                                                                          |
| 3C, 3D                    | V <sub>OSC</sub>   | Oscillator Power Supply. DC power is provided to the oscillator on these pins.                                                                                    |
| 4A, 4B                    | A <sub>0</sub>     | 2-Wire Slave Address Input. This pin is used to configure the slave address.                                                                                      |
| 4C, 4D                    | F <sub>1</sub>     | DC-TCXO Frequency Output                                                                                                                                          |
| 5A, 5B                    | SDA                | 2-Wire Serial-Data Input/Output. SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open drain and requires an external pullup resistor. |
| 5C, 5D                    | V <sub>CC</sub>    | Power Supply. DC power is provided to the device on these pins.                                                                                                   |
| 6A, 6B                    | SCL                | 2-Wire Serial-Clock Input. SCL is used to synchronize data movement on the serial interface. The SCL pin is open drain and requires an external pullup resistor.  |
| 6C, 6D                    | F <sub>2</sub>     | DC-TCXO Frequency Output                                                                                                                                          |

## DETAILED DESCRIPTION

The DS4000 digitally controlled temperature-compensated crystal oscillator (DC-TCXO) features a digital temperature sensor, one fixed-frequency temperature-compensated square-wave output ( $F_1$ ), one programmable temperature-compensated square-wave output ( $F_2$ ), and digital communication for frequency tuning (SDA, SCL).

**Figure 2. Block Diagram**



## TEMPERATURE-COMPENSATED CRYSTAL OSCILLATOR

The DS4000 can either function as a standalone TCXO or as a digitally controlled TCXO. When used as a standalone TCXO, the only requirements needed to function properly are power, ground, and an output. However, the 2-wire interface must be used to tune (push and pull) the crystal.

The DS4000 is capable of supplying two different outputs,  $F_1$  and  $F_2$ .

- 1)  $F_1$  is the base frequency of the crystal unit inside of the device. The output type is a CMOS square wave.
- 2)  $F_2$  is a programmable frequency output. The frequency select register can program this output to an integer division of the base ( $F_1$ ) frequency. The duty cycle (DC) bit determines if the output is an  $n + 1$  or a  $2(n + 1)$  division of  $F_1$ .

### $F_2$ FREQUENCY SELECT REGISTER (FSR) (5Dh)

| Bit     | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|---------|----|----|----|----|----|----|----|----|
| Name    | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Default | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

$$F_2 = F_1 / (\text{FSR value} + 1); \text{ with DC} = 0$$

$$F_2 = F_1 / [2 \times (\text{FSR value} + 1)]; \text{ with DC} = 1$$

### TCXO CONTROL REGISTER (60h)

| Bit     | 7 | 6 | 5 | 4 | 3              | 2              | 1     | 0  |
|---------|---|---|---|---|----------------|----------------|-------|----|
| Name    | X | X | X | X | $F_2\text{OE}$ | $F_1\text{OE}$ | $F_T$ | DC |
| Default | 0 | 0 | 0 | 0 | 0              | 0              | 0     | 0  |

**DC, Duty Cycle Bit:** If 50% duty cycle is desired, then this bit must be set to logic 1. The default condition at power-up is logic 0.

**$F_T$ :** This bit must be programmed by the user to 0.

**$F_1\text{OE}$ ,  $F_1$  Output Enable Bit:** This bit allows the user to disable/enable the  $F_1$  output.

**$F_2\text{OE}$ ,  $F_2$  Output Enable Bit:** This bit allows the user to disable/enable the  $F_2$  output.

## DIGITAL TUNING THE BASE CRYSTAL FREQUENCY

When using the 2-wire interface for tuning the base frequency, the frequency tuning register is used. The frequency tuning register contains two's complement data. The data is used to add or subtract an offset from the crystal loading register. When the tuning register is programmed with a value, the next temperature-update cycle sums the programmed value with the factory-compensated value. This allows the user/system to digitally control the base frequency by a microcontroller using the 2-wire protocol.

### FREQUENCY TUNING REGISTER (66h)

| Bit     | 7    | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|---------|------|-----|-----|-----|-----|-----|-----|-----|
| Name    | SIGN | FO6 | FO5 | FO4 | FO3 | FO2 | FO1 | FO0 |
| Default | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

**FOS[6:0], Frequency Offset:** These bits are used to tune the base crystal frequency. Each bit represents approximately 0.08ppm and, therefore, for a value of 07FH, pushes or pulls the base frequency by approximately 10.16ppm.

**SIGN, Sign Bit:** This bit is used to determine whether to add or subtract the frequency offset from the crystal loading.

**Table 1. Frequency Tuning Relationship**

| CALCULATED<br>FREQUENCY OFFSET<br>(ppm) | DIGITAL DATA<br>(Binary) | DIGITAL DATA<br>(hex) |
|-----------------------------------------|--------------------------|-----------------------|
| -10.16                                  | 0111 1111                | 7Fh                   |
| -8.00                                   | 0110 0100                | 64h                   |
| -5.28                                   | 0100 0010                | 42h                   |
| -1.84                                   | 0001 0111                | 17h                   |
| -0.08                                   | 0000 0001                | 01h                   |
| 0.0                                     | 0000 0000                | 00h                   |
| +0.08                                   | 1111 1111                | FFh                   |
| +1.84                                   | 1110 1000                | E8h                   |
| +5.28                                   | 1011 0011                | B3h                   |
| +8.00                                   | 1001 1100                | 9Ch                   |
| +10.16                                  | 1000 0000                | 80h                   |



## DIGITAL TEMPERATURE SENSOR

The digital temperature sensor provides 10-bit temperature readings that indicate the temperature of the device. Temperature readings are communicated from the DS4000 over a 2-wire serial interface. No additional components are required. The DS4000 has an external address bit that allows a user to choose the slave address from two possible values.

The factory-calibrated temperature sensor requires no external components. Upon power-up, the DS4000 starts performing temperature conversions with a resolution of 10 bits ( $+0.25^{\circ}\text{C}$  resolution). Following an 8-bit command protocol, temperature data can be read over the 2-wire interface. The host can periodically read the value in the temperature register, which contains the last completed conversion. As conversions are performed in the background, reading the temperature register does not affect the conversion in progress.

## READING TEMPERATURE

The DS4000 measures temperature through the use of an on-chip temperature-measurement technique with an operation range from  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  (commercial) or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (industrial). The device performs continuous conversions with the most recent result being stored in the temperature register. The digital temperature is retrieved from the temperature register using the READ TEMPERATURE command, as described in detail in the following paragraphs.

Table 2 shows the exact relationship of output data to measured temperature. The data is transmitted serially over the 2-wire serial interface, MSB first. The MSB of the temperature register contains the “sign” (S) bit, denoting whether the temperature is positive or negative. For Fahrenheit usage, a lookup table or conversion routine must be used.

### TEMPERATURE/DATA RELATIONSHIP (UNIT = $^{\circ}\text{C}$ )

| MSB (64h) |       |       |       |       |       |       |       |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| BIT 7     | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| S         | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |

| LSB (65h) |          |       |       |       |       |       |       |
|-----------|----------|-------|-------|-------|-------|-------|-------|
| BIT 7     | BIT 6    | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| $2^{-1}$  | $2^{-2}$ | 0     | 0     | 0     | 0     | 0     | 0     |

**Table 2. Temperature/Data Relationship**

| TEMPERATURE<br>( $^{\circ}\text{C}$ ) | DIGITAL OUTPUT<br>(Binary) | DIGITAL OUTPUT<br>(hex) |
|---------------------------------------|----------------------------|-------------------------|
| +85                                   | 0101 0101 0000 0000        | 5500h                   |
| +75                                   | 0100 1011 0000 0000        | 4B00h                   |
| +0.5                                  | 0000 0000 1000 0000        | 0080h                   |
| 0                                     | 0000 0000 0000 0000        | 0000h                   |
| -0.5                                  | 1111 1111 1000 0000        | FF80h                   |
| -20                                   | 1110 1100 0000 0000        | EC00h                   |
| -40                                   | 1101 1000 0000 0000        | D800h                   |

**Note:** Internal power dissipation raises the temperature above the ambient. The delta between ambient and the die temperature depends on power consumption, PC board layout, and airflow.

## READ TEMPERATURE COMMAND

This command reads the last temperature conversion result from the temperature register in the format described in the *Reading Temperature* section. If an application can accept temperature resolutions of  $+1.0^{\circ}\text{C}$ , then the master can read the first data byte and follow with a NACK and STOP. For higher resolution, both bytes must be read.

**Table 3. Command Set**

| INSTRUCTION                        | FUNCTION                                                    | PROTOCOL | 2-WIRE BUS DATA AFTER ISSUING PROTOCOL |
|------------------------------------|-------------------------------------------------------------|----------|----------------------------------------|
| Frequency Select Register (Note 1) | Defines $F_2$ output frequency                              | 5Dh      | Read or write 1 data byte              |
| TCXO Control Register (Note 1)     | Enables/disables $F_1$ and $F_2$ ; sets duty cycle of $F_2$ | 60h      | Read or write 1 data byte              |
| Read Temperature (Note 2)          | Reads 10-bit temperature register                           | 64h      | Read 1 or 2 data bytes                 |
| Frequency Tuning Register (Note 2) | Digitally adds/subtracts an offset from oscillator          | 66h      | Read or write 1 data byte              |

**Note 1:** The slave does not increment the internal address pointer between instructions. The address pointer must be reinitialized after each access.

**Note 2:** If the user only desires 8-bit thermometer readings, the master can read one data byte, and follow with a NACK and STOP. If higher resolution is required, both bytes must be read.

## 2-WIRE SERIAL INTERFACE

The DS4000 supports a bidirectional 2-wire serial bus and data transmission protocol. The bus must be controlled by a master device, which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS4000 operates as a slave on the 2-wire bus. The DS4000 works in a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate), which are defined within the bus specifications. Connections to the bus are made by the open-drain I/O signals SDA and SCL.

The following bus protocol has been defined (Figure 3):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data signal must remain stable whenever the clock signal is HIGH. Changes in the data signal while the clock signal is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

**Bus Not Busy:** Both data and clock signals remain HIGH.

**Start Data Transfer:** A change in the state of the data signal, from HIGH to LOW, while the clock line is HIGH, defines the START condition.

**Stop Data Transfer:** A change in the state of the data signal, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

**Data Valid:** The state of the data signal represents valid data when, after a START condition, the data signal is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

**Acknowledge:** Each receiving device, when addressed, is required to generate an acknowledge after reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the serial data (SDA) signal during the acknowledge clock pulse in such a way that the SDA signal is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end-of-data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data signal HIGH to enable the master to generate the STOP condition.



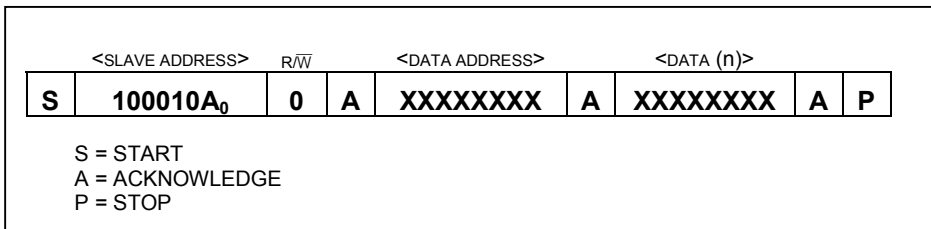
## SLAVE ADDRESS

The slave address is the first byte received following the START condition generated by the master device. The address byte consists of a 7-bit slave address and the  $R/\overline{W}$  direction bit. The DS4000 slave address is set to  $100010A_0$ , where  $A_0$  is externally hardwired to a HIGH or LOW state. This allows design flexibility to set the slave's address to one of two possible address locations. The last bit following the slave address is the direction bit ( $R/\overline{W}$ ) and defines the operation to be performed by the master, transmit data ( $R/\overline{W} = 0$ ), or receive data ( $R/\overline{W} = 1$ ). Following the START condition, the DS4000 monitors the SDA bus by checking the slave address being transmitted. Upon receiving the proper slave address and  $R/\overline{W}$  bit, the slave device outputs an acknowledge signal on the SDA line regardless of the operation mode.

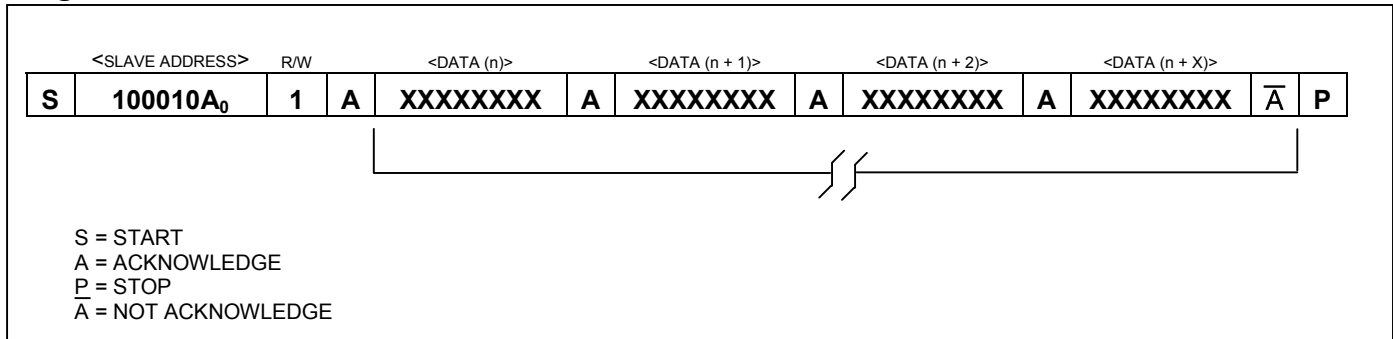
The DS4000 can operate in the following two modes:

- 1) **Slave Receiver Mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by the hardware after reception of the slave address and direction bit (Figure 4).
- 2) **Slave Transmitter Mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS4000 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 5).

**Figure 4. Data Write—Slave Receiver Mode**



**Figure 5. Data Read—Slave Transmitter Mode**



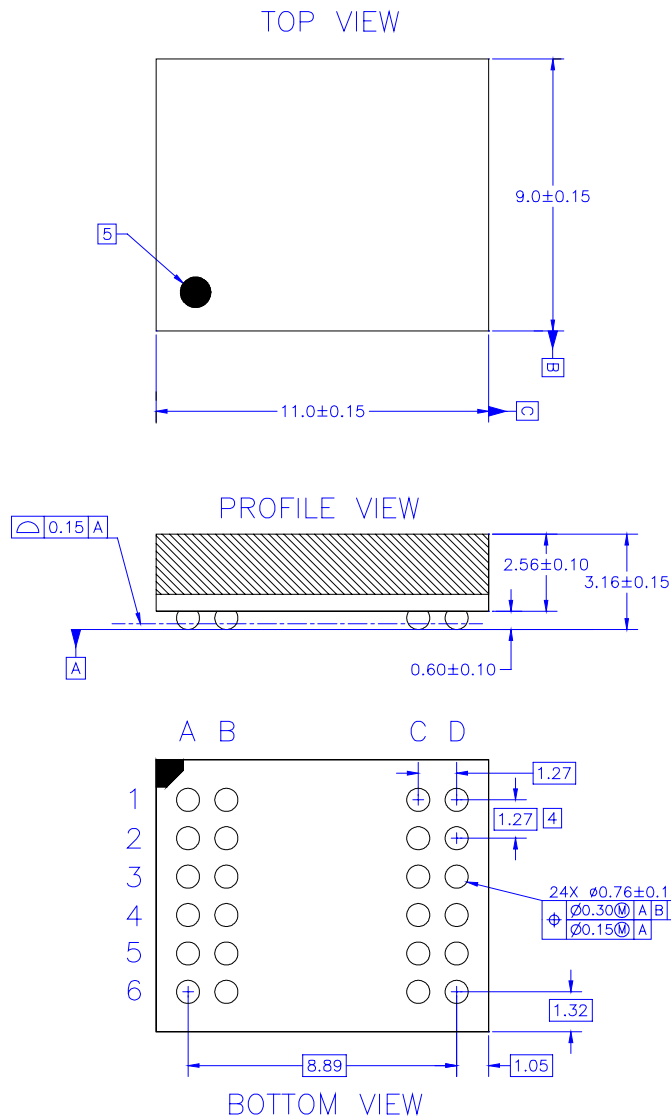
**SELECTOR GUIDE**

| PART           | TEMP RANGE     | PIN-PACKAGE | TOP MARK            | FREQUENCY<br>DESIGNATOR (MHz) |
|----------------|----------------|-------------|---------------------|-------------------------------|
| DS4000A0/WBGA  | 0°C to +70°C   | 24 BGA      | DS4000A0            | 10.00000                      |
| DS4000A0N/WBGA | -40°C to +85°C | 24 BGA      | DS4000A0<br>###XX N | 10.00000                      |
| DS4000CW/WBGA  | 0°C to +70°C   | 24 BGA      | DS4000CW            | 12.80000                      |
| DS4000CWN/WBGA | -40°C to +85°C | 24 BGA      | DS4000CW<br>###XX N | 12.80000                      |
| DS4000D0/WBGA  | 0°C to +70°C   | 24 BGA      | DS4000D0            | 13.00000                      |
| DS4000D0N/WBGA | -40°C to +85°C | 24 BGA      | DS4000D0<br>###XX N | 13.00000                      |
| DS4000EC/WBGA  | 0°C to +70°C   | 24 BGA      | DS4000EC            | 14.31818                      |
| DS4000ECN/WBGA | -40°C to +85°C | 24 BGA      | DS4000EC<br>###XX N | 14.31818                      |
| DS4000G0/WBGA  | 0°C to +70°C   | 24 BGA      | DS4000G0            | 16.00000                      |
| DS4000G0N/WBGA | -40°C to +85°C | 24 BGA      | DS4000G0<br>###XX N | 16.00000                      |
| DS4000GF/WBGA  | 0°C to +70°C   | 24 BGA      | DS4000GF            | 16.38400                      |
| DS4000GFN/WBGA | -40°C to +85°C | 24 BGA      | DS4000GF<br>###XX N | 16.38400                      |
| DS4000GW/WBGA  | 0°C to +70°C   | 24 BGA      | DS4000GW            | 16.80000                      |
| DS4000GWN/WBGA | -40°C to +85°C | 24 BGA      | DS4000GW<br>###XX N | 16.80000                      |
| DS4000KI/WBGA  | 0°C to +70°C   | 24 BGA      | DS4000KI            | 19.44000                      |
| DS4000KIN/WBGA | -40°C to +85°C | 24 BGA      | DS4000KI<br>###XX N | 19.44000                      |

## PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/DallasPackInfo](http://www.maxim-ic.com/DallasPackInfo).)

**NOTE:** THE BGA IS SOLDER-MASKED DEFINED.



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONING AND TOLERANCES PER ASME Y14.5M-1994.

2. DIMENSIONS IN MILLIMETERS.

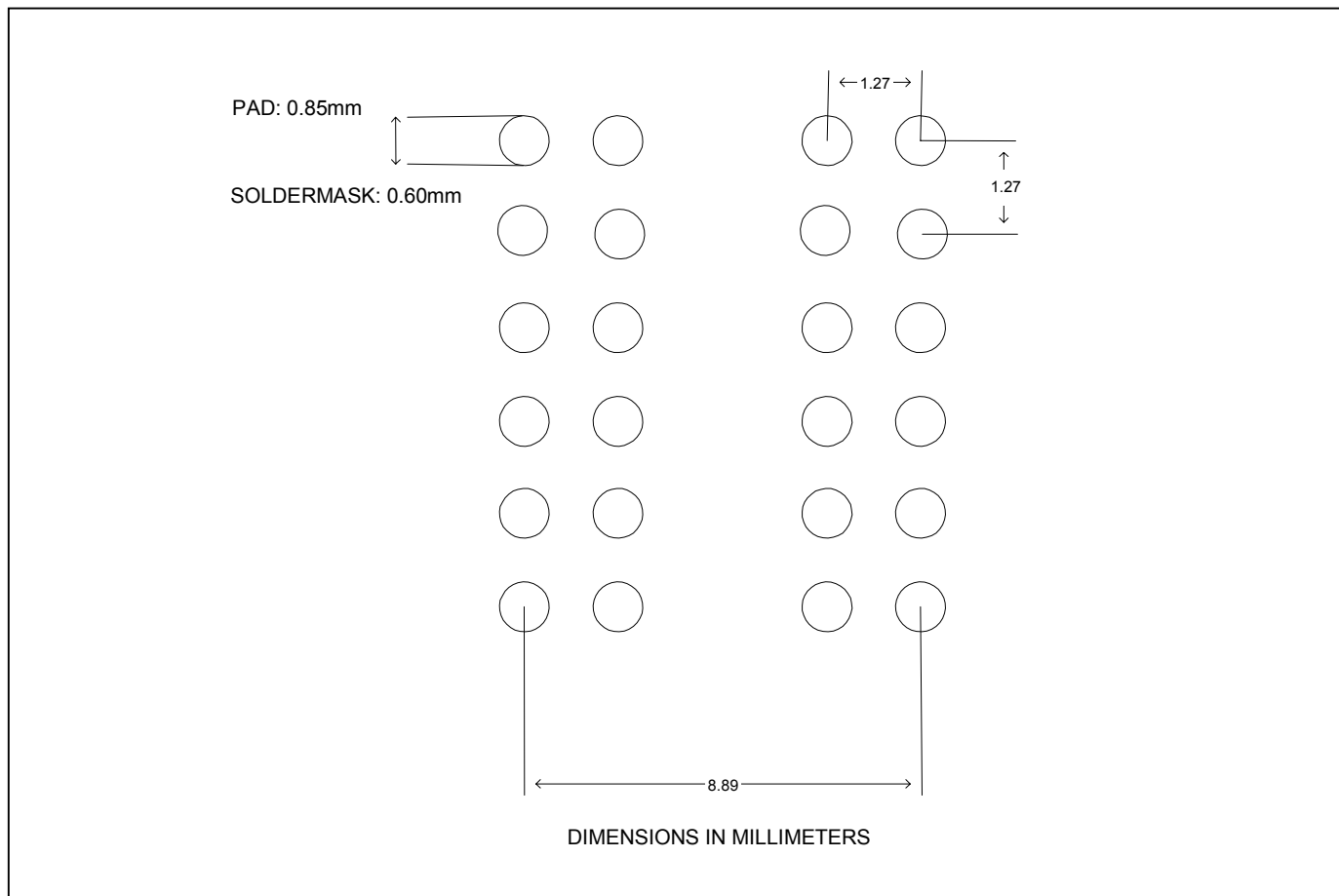
3. DATUM A (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4. BALL DIAMETER IS MEASURED AT ITS MAXIMUM SIZE, PARALLEL TO DATUM A.

5. A1 CORNER IDENTIFIED WITH CONTRASTING INK MARKING, VISIBLE FROM TOP SURFACE, AND IN SOLDERMASK, VISIBLE FROM THE BOTTOM SURFACE.

**PACKAGE INFORMATION (continued)**

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