Features

- High-performance, Low-power 32-bit Atmel® AVR® Microcontroller
  - Compact Single-cycle RISC Instruction Set Including DSP Instructions
  - Read-modify-write Instructions and Atomic Bit Manipulation
  - Performance
    - Up to 64 DMIPS Running at 50 MHz from Flash (1 Flash Wait State)
    - Up to 36 DMIPS Running at 25 MHz from Flash (0 Flash Wait State)
  - Memory Protection Unit (MPU)
    - Secure Access Unit (SAU) providing User-defined Peripheral Protection
- picoPower® Technology for Ultra-low Power Consumption
- Multi-hierarchy Bus System
  - High-performance Data Transfers on Separate Buses for Increased Performance
  - 12 Peripheral DMA Channels Improve Speed for Peripheral Communication
- Internal High-speed Flash
  - 256 Kbytes and 128 Kbytes Versions
  - Single-cycle Access up to 25 MHz
  - FlashVault Technology Allows Pre-programmed Secure Library Support for End User Applications
  - Prefetch Buffer Optimizing Instruction Execution at Maximum Speed
  - 100,000 Write Cycles, 15-year Data Retention Capability
  - Flash Security Locks and User-defined Configuration Area
- Internal High-speed SRAM, Single-cycle Access at Full Speed
  - 32 Kbytes
- Interrupt Controller (INTC)
  - Autovectored Low-latency Interrupt Service with Programmable Priority
- External Interrupt Controller (EIC)
- Peripheral Event System for Direct Peripheral to Peripheral Communication
- System Functions
  - Power and Clock Manager
  - SleepWalking Power Saving Control
  - Internal System RC Oscillator (RCSYS)
  - 32 KHz Oscillator
  - Multipurpose Oscillator, Phase Locked Loop (PLL), and Digital Frequency Locked Loop (DFLL)
- Windowed Watchdog Timer (WDT)
- Asynchronous Timer (AST) with Real-time Clock Capability
  - Counter or Calendar Mode Supported
- Frequency Meter (FREQM) for Accurate Measuring of Clock Frequency
- Six 16-bit Timer/Counter (TC) Channels
  - External Clock Inputs, PWM, Capture, and Various Counting Capabilities
- PWM Channels on All I/O Pins (PWMA)
  - 8-bit PWM with a Source Clock up to 150 MHz
- Four Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
  - Independent Baudrate Generator, Support for SPI
  - Support for Hardware Handshaking
- One Master/Slave Serial Peripheral Interface (SPI) with Chip Select Signals
  - Up to 15 SPI Slaves can be Addressed

32-bit Atmel AVR Microcontroller

AT32UC3L0256 AT32UC3L0128

Summary

32145CS–06/2013

- **Two Master and Two Slave Two-wire Interfaces (TWI), 400 kbit/s I^2C-compatible**
- **One 8-channel Analog-to-digital Converter (ADC) with up to 12 Bits Resolution**
  - **Internal Temperature Sensor**
- **Eight Analog Comparators (AC) with Optional Window Detection**
- **Capacitive Touch (CAT) Module**
  - **Hardware-assisted Atmel® AVR® QTouch® and Atmel® AVR® QMatrix Touch Acquisition**
  - **Supports QTouch and QMatrix Capture from Capacitive Touch Sensors**
- **QTouch Library Support**
  - **Capacitive Touch Buttons, Sliders, and Wheels**
  - **QTouch and QMatrix Acquisition**
- **On-chip Non-intrusive Debug System**
  - **Nexus Class 2+, Runtime Control, Non-intrusive Data and Program Trace**
  - **aWire Single-pin Programming Trace and Debug Interface Muxed with Reset Pin**
  - **NanoTrace Provides Trace Capabilities through JTAG or aWire Interface**
- **48-pin TQFP/QFN/TLLGA (36 GPIO Pins)**
- **Five High-drive I/O Pins**
- **Single 1.62-3.6 V Power Supply**

1. Description

The Atmel® AVR® AT32UC3L0128/256 is a complete system-on-chip microcontroller based on the AVR32 UC RISC processor running at frequencies up to 50MHz. AVR32 UC is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density, and high performance.

The processor implements a Memory Protection Unit (MPU) and a fast and flexible interrupt controller for supporting modern and real-time operating systems. The Secure Access Unit (SAU) is used together with the MPU to provide the required security and integrity.

Higher computation capability is achieved using a rich set of DSP instructions.

The AT32UC3L0128/256 embeds state-of-the-art picoPower technology for ultra-low power consumption. Combined power control techniques are used to bring active current consumption down to 174µA/MHz, and leakage down to 220nA while still retaining a bank of backup registers. The device allows a wide range of trade-offs between functionality and power consumption, giving the user the ability to reach the lowest possible power consumption with the feature set required for the application.

The Peripheral Direct Memory Access (DMA) controller enables data transfers between peripherals and memories without processor involvement. The Peripheral DMA controller drastically reduces processing overhead when transferring continuous and large data streams.

The AT32UC3L0128/256 incorporates on-chip Flash and SRAM memories for secure and fast access. The FlashVault technology allows secure libraries to be programmed into the device. The secure libraries can be executed while the CPU is in Secure State, but not read by non-secure software in the device. The device can thus be shipped to end customers, who will be able to program their own code into the device to access the secure libraries, but without risk of compromising the proprietary secure code.

The External Interrupt Controller (EIC) allows pins to be configured as external interrupts. Each external interrupt has its own interrupt request and can be individually masked.

The Peripheral Event System allows peripherals to receive, react to, and send peripheral events without CPU intervention. Asynchronous interrupts allow advanced peripheral operation in low power sleep modes.

The Power Manager (PM) improves design flexibility and security. The Power Manager supports SleepWalking functionality, by which a module can be selectively activated based on peripheral events, even in sleep modes where the module clock is stopped. Power monitoring is supported by on-chip Power-on Reset (POR), Brown-out Detector (BOD), and Supply Monitor (SM). The device features several oscillators, such as Phase Locked Loop (PLL), Digital Frequency Locked Loop (DFLL), Oscillator 0 (OSC0), and system RC oscillator (RCSYS). Either of these oscillators can be used as source for the system clock. The DFLL is a programmable internal oscillator from 20 to 150MHz. It can be tuned to a high accuracy if an accurate reference clock is running, e.g. the 32KHz crystal oscillator.

The Watchdog Timer (WDT) will reset the device unless it is periodically serviced by the software. This allows the device to recover from a condition that has caused the system to be unstable.

The Asynchronous Timer (AST) combined with the 32KHz crystal oscillator supports powerful real-time clock capabilities, with a maximum timeout of up to 136 years. The AST can operate in counter mode or calendar mode.

The Frequency Meter (FREQM) allows accurate measuring of a clock frequency by comparing it to a known reference clock.

The device includes six identical 16-bit Timer/Counter (TC) channels. Each channel can be independently programmed to perform frequency measurement, event counting, interval measurement, pulse generation, delay timing, and pulse width modulation.

The Pulse Width Modulation controller (PWMA) provides 8-bit PWM channels which can be synchronized and controlled from a common timer. One PWM channel is available for each I/O pin on the device, enabling applications that require multiple PWM outputs, such as LCD backlight control. The PWM channels can operate independently, with duty cycles set individually, or in interlinked mode, with multiple channels changed at the same time.

The AT32UC3L0128/256 also features many communication interfaces, like USART, SPI, and TWI, for communication intensive applications. The USART supports different communication modes, like SPI Mode and LIN Mode.

A general purpose 8-channel ADC is provided, as well as eight analog comparators (AC). The ADC can operate in 10-bit mode at full speed or in enhanced mode at reduced speed, offering up to 12-bit resolution. The ADC also provides an internal temperature sensor input channel. The analog comparators can be paired to detect when the sensing voltage is within or outside the defined reference window.

The Capacitive Touch (CAT) module senses touch on external capacitive touch sensors, using the QTouch technology. Capacitive touch sensors use no external mechanical components, unlike normal push buttons, and therefore demand less maintenance in the user application. The CAT module allows up to 17 touch sensors, or up to 16 by 8 matrix sensors to be interfaced. All touch sensors can be configured to operate autonomously without software interaction, allowing wakeup from sleep modes when activated.

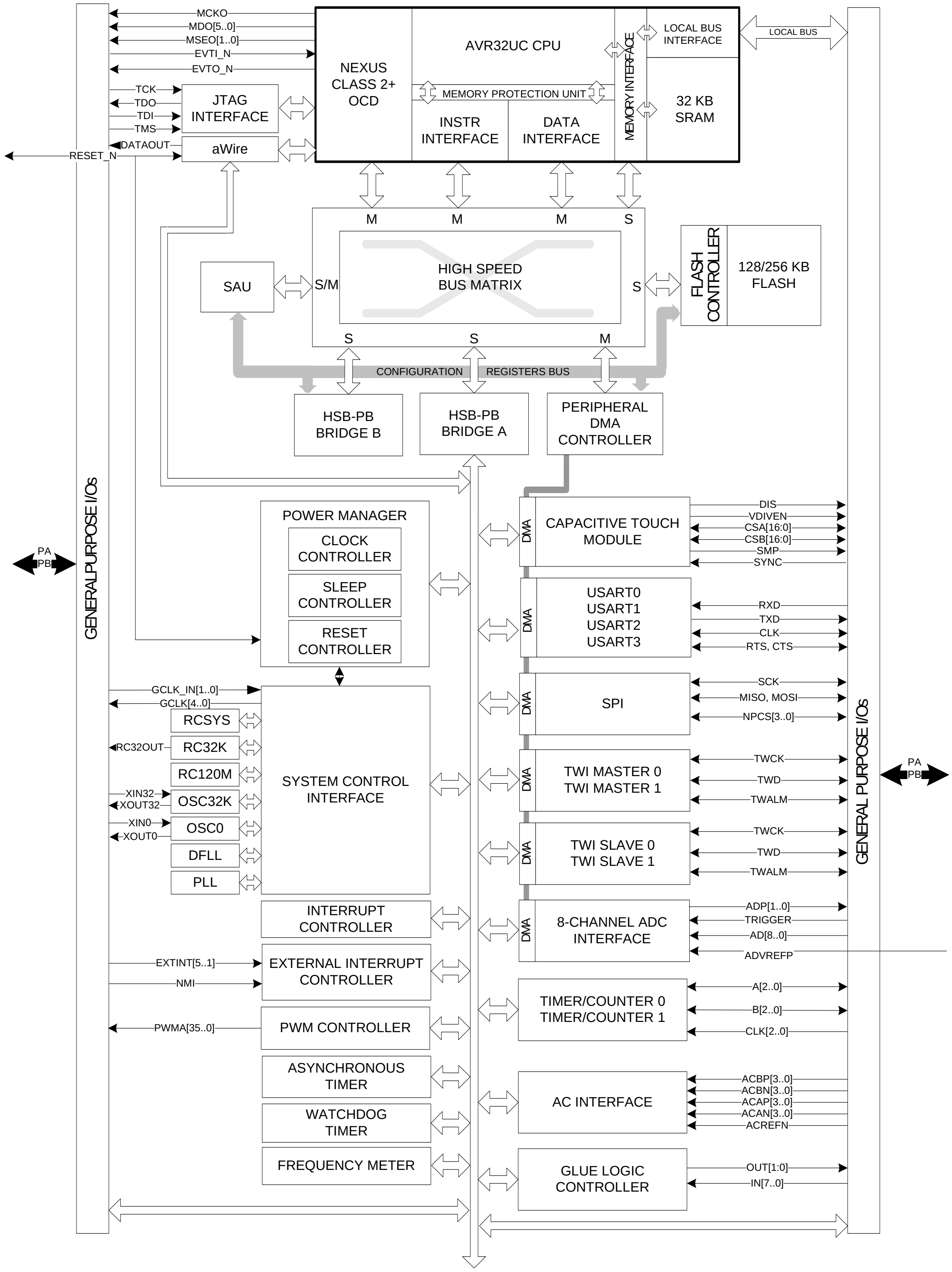
Atmel offers the QTouch library for embedding capacitive touch buttons, sliders, and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys as well as Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop, and debug your own touch applications.

The AT32UC3L0128/256 integrates a class 2+ Nexus 2.0 On-chip Debug (OCD) System, with non-intrusive real-time trace and full-speed read/write memory access, in addition to basic runtime control. The NanoTrace interface enables trace feature for aWire- or JTAG-based debuggers. The single-pin aWire interface allows all features available through the JTAG interface to be accessed through the RESET pin, allowing the JTAG pins to be used for GPIO or peripherals.

2. Overview

2.1 Block Diagram

Figure 2-1. Block Diagram



2.2 Configuration Summary

Table 2-1. Configuration Summary

Feature	AT32UC3L0256	AT32UC3L0128
Flash	256KB	128KB
SRAM	32KB	
GPIO	36	
High-drive pins	5	
External Interrupts	6	
TWI	2	
USART	4	
Peripheral DMA Channels	12	
Peripheral Event System	1	
SPI	1	
Asynchronous Timers	1	
Timer/Counter Channels	6	
PWM channels	36	
Frequency Meter	1	
Watchdog Timer	1	
Power Manager	1	
Secure Access Unit	1	
Glue Logic Controller	1	
Oscillators	Digital Frequency Locked Loop 20-150 MHz (DFLL) Phase Locked Loop 40-240 MHz (PLL) Crystal Oscillator 0.45-16 MHz (OSC0) Crystal Oscillator 32 KHz (OSC32K) RC Oscillator 120MHz (RC120M) RC Oscillator 115 kHz (RCSYS) RC Oscillator 32 kHz (RC32K)	
ADC	8-channel 12-bit	
Temperature Sensor	1	
Analog Comparators	8	
Capacitive Touch Module	1	
JTAG	1	
aWire	1	
Max Frequency	50 MHz	
Packages	TQFP48/QFN48/TLLGA48	

3. Package and Pinout

3.1 Package

The device pins are multiplexed with peripheral functions as described in Section 3.2.1.

Figure 3-1. TQFP48/QFN48 Pinout

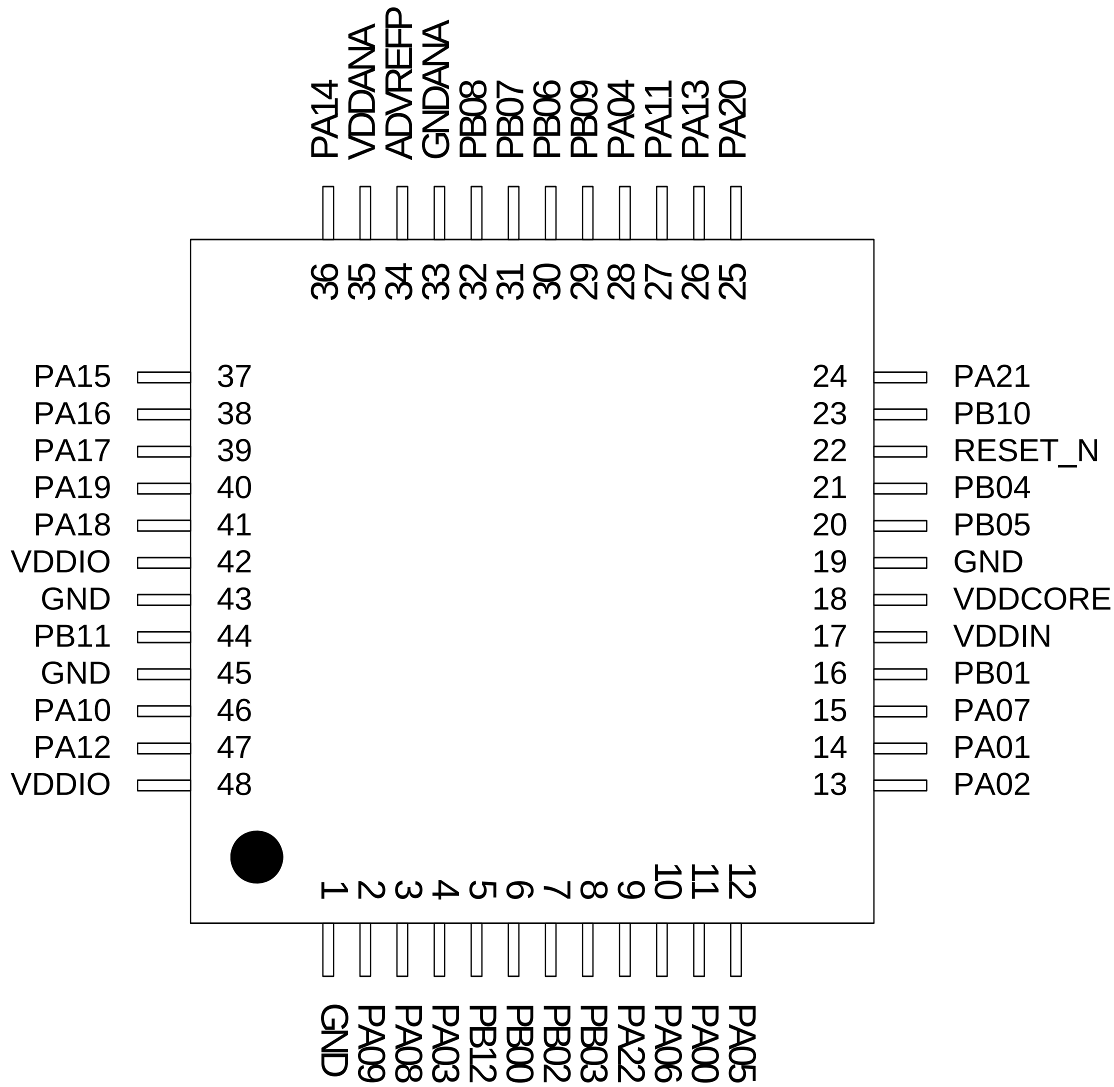
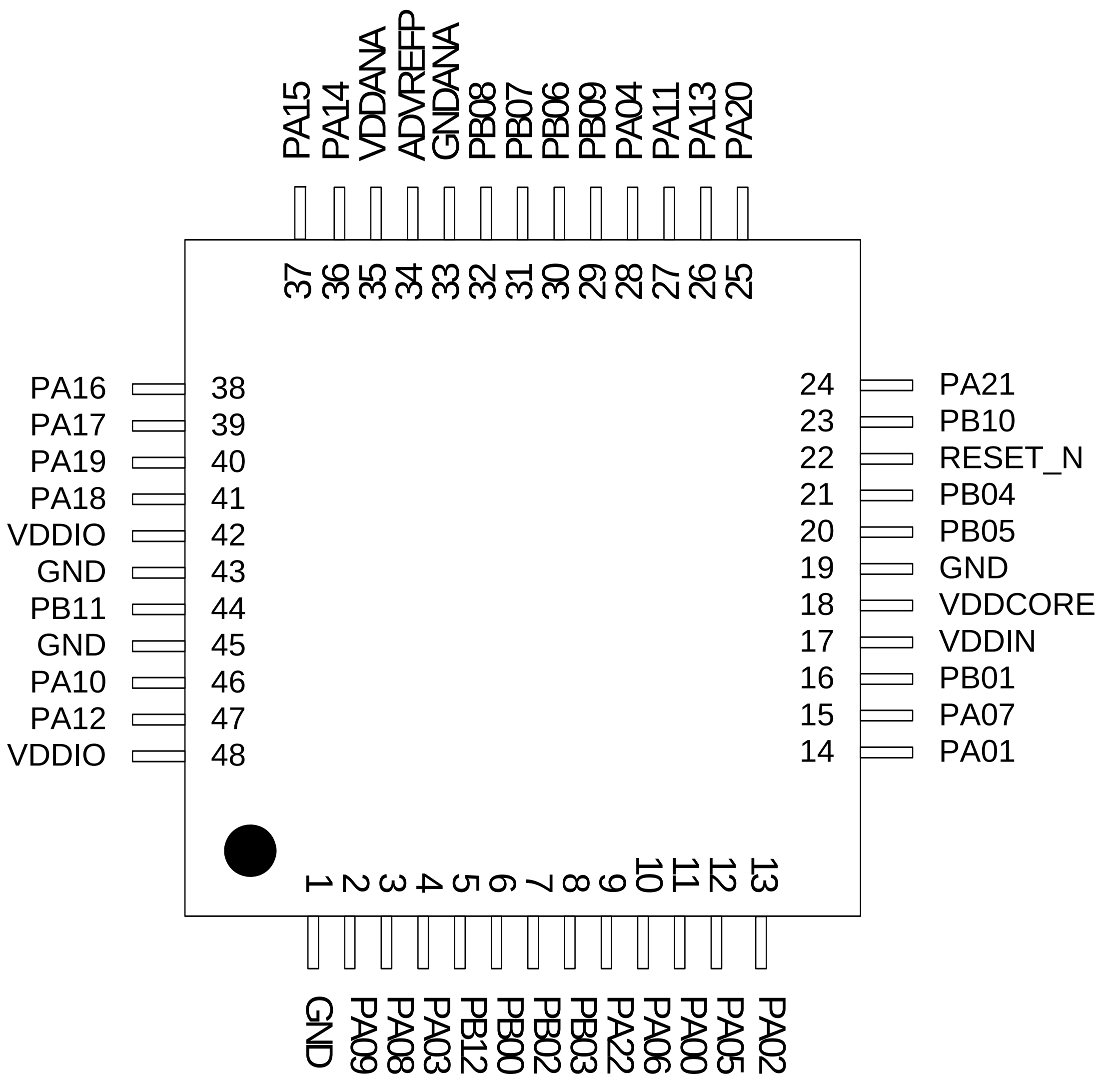


Figure 3-2. TLLGA48 Pinout



3.2 Peripheral Multiplexing on I/O Lines

3.2.1 Multiplexed Signals

Each GPIO line can be assigned to one of the peripheral functions. The following table describes the peripheral signals multiplexed to the GPIO lines.

Table 3-1. GPIO Controller Function Multiplexing

48-pin	PIN	GPIO	Supply	Pin Type	GPIO Function A	B	C	D	E	F	G	H
11	PA00	0	VDDIO	Normal I/O	USART0 TXD	USART1 RTS	SPI NPCS[2]		PWMA PWMA[0]		SCIF GCLK[0]	CAT CSA[2]
14	PA01	1	VDDIO	Normal I/O	USART0 RXD	USART1 CTS	SPI NPCS[3]	USART1 CLK	PWMA PWMA[1]	ACIFB ACAP[0]	TWIMS0 TWALM	CAT CSA[1]

Table 3-1. GPIO Controller Function Multiplexing

13	PA02	2	VDDIO	High-drive I/O	USART0 RTS	ADCIFB TRIGGER	USART2 TXD	TC0 A0	PWMA PWMA[2]	ACIFB ACBP[0]	USART0 CLK	CAT CSA[3]
4	PA03	3	VDDIO	Normal I/O	USART0 CTS	SPI NPCS[1]	USART2 TXD	TC0 B0	PWMA PWMA[3]	ACIFB ACBN[3]	USART0 CLK	CAT CSB[3]
28	PA04	4	VDDIO	Normal I/O	SPI MISO	TWIMS0 TWCK	USART1 RXD	TC0 B1	PWMA PWMA[4]	ACIFB ACBP[1]		CAT CSA[7]
12	PA05	5	VDDIO	Normal I/O (TWI)	SPI MOSI	TWIMS1 TWCK	USART1 TXD	TC0 A1	PWMA PWMA[5]	ACIFB ACBN[0]	TWIMS0 TWD	CAT CSB[7]
10	PA06	6	VDDIO	High-drive I/O, 5V tolerant	SPI SCK	USART2 TXD	USART1 CLK	TC0 B0	PWMA PWMA[6]	EIC EXTINT[2]	SCIF GCLK[1]	CAT CSB[1]
15	PA07	7	VDDIO	Normal I/O (TWI)	SPI NPCS[0]	USART2 RXD	TWIMS1 TWALM	TWIMS0 TWCK	PWMA PWMA[7]	ACIFB ACAN[0]	EIC NMI (EXTINT[0])	CAT CSB[2]
3	PA08	8	VDDIO	High-drive I/O	USART1 TXD	SPI NPCS[2]	TC0 A2	ADCIFB ADP[0]	PWMA PWMA[8]			CAT CSA[4]
2	PA09	9	VDDIO	High-drive I/O	USART1 RXD	SPI NPCS[3]	TC0 B2	ADCIFB ADP[1]	PWMA PWMA[9]	SCIF GCLK[2]	EIC EXTINT[1]	CAT CSB[4]
46	PA10	10	VDDIO	Normal I/O	TWIMS0 TWD		TC0 A0		PWMA PWMA[10]	ACIFB ACAP[1]	SCIF GCLK[2]	CAT CSA[5]
27	PA11	11	VDDIN	Normal I/O					PWMA PWMA[11]			
47	PA12	12	VDDIO	Normal I/O		USART2 CLK	TC0 CLK1	CAT SMP	PWMA PWMA[12]	ACIFB ACAN[1]	SCIF GCLK[3]	CAT CSB[5]
26	PA13	13	VDDIN	Normal I/O	GLOC OUT[0]	GLOC IN[7]	TC0 A0	SCIF GCLK[2]	PWMA PWMA[13]	CAT SMP	EIC EXTINT[2]	CAT CSA[0]
36	PA14	14	VDDIO	Normal I/O	ADCIFB AD[0]	TC0 CLK2	USART2 RTS	CAT SMP	PWMA PWMA[14]		SCIF GCLK[4]	CAT CSA[6]
37	PA15	15	VDDIO	Normal I/O	ADCIFB AD[1]	TC0 CLK1		GLOC IN[6]	PWMA PWMA[15]	CAT SYNC	EIC EXTINT[3]	CAT CSB[6]
38	PA16	16	VDDIO	Normal I/O	ADCIFB AD[2]	TC0 CLK0		GLOC IN[5]	PWMA PWMA[16]	ACIFB ACREFN	EIC EXTINT[4]	CAT CSA[8]
39	PA17	17	VDDIO	Normal I/O (TWI)		TC0 A1	USART2 CTS	TWIMS1 TWD	PWMA PWMA[17]	CAT SMP	CAT DIS	CAT CSB[8]
41	PA18	18	VDDIO	Normal I/O	ADCIFB AD[4]	TC0 B1		GLOC IN[4]	PWMA PWMA[18]	CAT SYNC	EIC EXTINT[5]	CAT CSB[0]
40	PA19	19	VDDIO	Normal I/O	ADCIFB AD[5]		TC0 A2	TWIMS1 TWALM	PWMA PWMA[19]	SCIF GCLK_IN[0]	CAT SYNC	CAT CSA[10]
25	PA20	20	VDDIN	Normal I/O	USART2 TXD		TC0 A1	GLOC IN[3]	PWMA PWMA[20]	SCIF RC32OUT		CAT CSA[12]
24	PA21	21	VDDIN	Normal I/O (TWI, 5V tolerant, SMBus)	USART2 RXD	TWIMS0 TWD	TC0 B1	ADCIFB TRIGGER	PWMA PWMA[21]	PWMA PWMAOD[21]	SCIF GCLK[0]	CAT SMP
9	PA22	22	VDDIO	Normal I/O	USART0 CTS	USART2 CLK	TC0 B2	CAT SMP	PWMA PWMA[22]	ACIFB ACBN[2]		CAT CSB[10]
6	PB00	32	VDDIO	Normal I/O	USART3 TXD	ADCIFB ADP[0]	SPI NPCS[0]	TC0 A1	PWMA PWMA[23]	ACIFB ACAP[2]	TC1 A0	CAT CSA[9]
16	PB01	33	VDDIO	High-drive I/O	USART3 RXD	ADCIFB ADP[1]	SPI SCK	TC0 B1	PWMA PWMA[24]		TC1 A1	CAT CSB[9]
7	PB02	34	VDDIO	Normal I/O	USART3 RTS	USART3 CLK	SPI MISO	TC0 A2	PWMA PWMA[25]	ACIFB ACAN[2]	SCIF GCLK[1]	CAT CSB[11]

Table 3-1. GPIO Controller Function Multiplexing

8	PB03	35	VDDIO	Normal I/O	USART3 CTS	USART3 CLK	SPI MOSI	TC0 B2	PWMA PWMA[26]	ACIFB ACBP[2]	TC1 A2	CAT CSA[11]
21	PB04	36	VDDIN	Normal I/O (TWI, 5V tolerant, SMBus)	TC1 A0	USART1 RTS	USART1 CLK	TWIMS0 TWALM	PWMA PWMA[27]	PWMA PWMAOD[27]	TWIMS1 TWCK	CAT CSA[14]
20	PB05	37	VDDIN	Normal I/O (TWI, 5V tolerant, SMBus)	TC1 B0	USART1 CTS	USART1 CLK	TWIMS0 TWCK	PWMA PWMA[28]	PWMA PWMAOD[28]	SCIF GCLK[3]	CAT CSB[14]
30	PB06	38	VDDIO	Normal I/O	TC1 A1	USART3 TXD	ADCIFB AD[6]	GLOC IN[2]	PWMA PWMA[29]	ACIFB ACAN[3]	EIC NMI (EXTINT[0])	CAT CSB[13]
31	PB07	39	VDDIO	Normal I/O	TC1 B1	USART3 RXD	ADCIFB AD[7]	GLOC IN[1]	PWMA PWMA[30]	ACIFB ACAP[3]	EIC EXTINT[1]	CAT CSA[13]
32	PB08	40	VDDIO	Normal I/O	TC1 A2	USART3 RTS	ADCIFB AD[8]	GLOC IN[0]	PWMA PWMA[31]	CAT SYNC	EIC EXTINT[2]	CAT CSB[12]
29	PB09	41	VDDIO	Normal I/O	TC1 B2	USART3 CTS	USART3 CLK		PWMA PWMA[32]	ACIFB ACBN[1]	EIC EXTINT[3]	CAT CSB[15]
23	PB10	42	VDDIN	Normal I/O	TC1 CLK0	USART1 TXD	USART3 CLK	GLOC OUT[1]	PWMA PWMA[33]	SCIF GCLK_IN[1]	EIC EXTINT[4]	CAT CSB[16]
44	PB11	43	VDDIO	Normal I/O	TC1 CLK1	USART1 RXD		ADCIFB TRIGGER	PWMA PWMA[34]	CAT VDIVEN	EIC EXTINT[5]	CAT CSA[16]
5	PB12	44	VDDIO	Normal I/O	TC1 CLK2		TWIMS1 TWALM	CAT SYNC	PWMA PWMA[35]	ACIFB ACBP[3]	SCIF GCLK[4]	CAT CSA[15]

See Section 3.3 for a description of the various peripheral signals.

Refer to "Electrical Characteristics" on page 791 for a description of the electrical properties of the pin types used.

3.2.2 TWI, 5V Tolerant, and SMBUS Pins

Some normal I/O pins offer TWI, 5V tolerance, and SMBUS features. These features are only available when either of the TWI functions or the PWMAOD function in the PWMA are selected for these pins.

Refer to the "TWI Pin Characteristics(1)" on page 798 for a description of the electrical properties of the TWI, 5V tolerance, and SMBUS pins.

3.2.3 Peripheral Functions

Each GPIO line can be assigned to one of several peripheral functions. The following table describes how the various peripheral functions are selected. The last listed function has priority in case multiple functions are enabled on the same pin.

Table 3-2. Peripheral Functions

Function	Description
GPIO Controller Function multiplexing	GPIO and GPIO peripheral selection A to H
Nexus OCD AUX port connections	OCD trace system
aWire DATAOUT	aWire output in two-pin mode
JTAG port connections	JTAG debug port
Oscillators	OSC0, OSC32

3.2.4 JTAG Port Connections

If the JTAG is enabled, the JTAG will take control over a number of pins, irrespectively of the I/O Controller configuration.

Table 3-3. JTAG Pinout

48-pin	Pin name	JTAG pin
11	PA00	TCK
14	PA01	TMS
13	PA02	TDO
4	PA03	TDI

3.2.5 Nexus OCD AUX Port Connections

If the OCD trace system is enabled, the trace system will take control over a number of pins, irrespectively of the I/O Controller configuration. Two different OCD trace pin mappings are possible, depending on the configuration of the OCD AXS register. For details, see the AVR32 UC Technical Reference Manual.

Table 3-4. Nexus OCD AUX Port Connections

Pin	AXS=1	AXS=0
EVTI_N	PA05	PB08
MDO[5]	PA10	PB00
MDO[4]	PA18	PB04
MDO[3]	PA17	PB05
MDO[2]	PA16	PB03
MDO[1]	PA15	PB02
MDO[0]	PA14	PB09

Table 3-4. Nexus OCD AUX Port Connections

Pin	AXS=1	AXS=0
EVTO_N	PA04	PA04
MCKO	PA06	PB01
MSEO[1]	PA07	PB11
MSEO[0]	PA11	PB12

3.2.6 Oscillator Pinout

The oscillators are not mapped to the normal GPIO functions and their muxings are controlled by registers in the System Control Interface (SCIF). Please refer to the SCIF chapter for more information about this.

Table 3-5. Oscillator Pinout

48-pin	Pin Name	Oscillator Pin
3	PA08	XIN0
46	PA10	XIN32
26	PA13	XIN32_2
2	PA09	XOUT0
47	PA12	XOUT32
25	PA20	XOUT32_2

3.2.7 Other Functions

The functions listed in Table 3-6 are not mapped to the normal GPIO functions. The aWire DATA pin will only be active after the aWire is enabled. The aWire DATAOUT pin will only be active after the aWire is enabled and the 2_PIN_MODE command has been sent. The WAKE_N pin is always enabled. Please refer to Section 6.1.4 on page 40 for constraints on the WAKE_N pin.

Table 3-6. Other Functions

48-pin	Pin	Function
27	PA11	WAKE_N
22	RESET_N	aWire DATA
11	PA00	aWire DATAOUT

3.3 Signal Descriptions

The following table gives details on signal names classified by peripheral.

Table 3-7. Signal Descriptions List

Signal Name	Function	Type	Active Level	Comments
Analog Comparator Interface - ACIFB				
ACAN3 - ACAN0	Negative inputs for comparators "A"	Analog		
ACAP3 - ACAP0	Positive inputs for comparators "A"	Analog		
ACBN3 - ACBN0	Negative inputs for comparators "B"	Analog		
ACBP3 - ACBP0	Positive inputs for comparators "B"	Analog		
ACREFN	Common negative reference	Analog		
ADC Interface - ADCIFB				
AD8 - AD0	Analog Signal	Analog		
ADP1 - ADP0	Drive Pin for resistive touch screen	Output		
TRIGGER	External trigger	Input		
aWire - AW				
DATA	aWire data	I/O		
DATAOUT	aWire data output for 2-pin mode	I/O		
Capacitive Touch Module - CAT				
CSA16 - CSA0	Capacitive Sense A	I/O		
CSB16 - CSB0	Capacitive Sense B	I/O		
DIS	Discharge current control	Analog		
SMP	SMP signal	Output		
SYNC	Synchronize signal	Input		
VDIVEN	Voltage divider enable	Output		
External Interrupt Controller - EIC				
NMI (EXTINT0)	Non-Maskable Interrupt	Input		
EXTINT5 - EXTINT1	External interrupt	Input		
Glue Logic Controller - GLOC				
IN7 - IN0	Inputs to lookup tables	Input		
OUT1 - OUT0	Outputs from lookup tables	Output		
JTAG module - JTAG				
TCK	Test Clock	Input		
TDI	Test Data In	Input		
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		

Table 3-7. Signal Descriptions List

Power Manager - PM				
RESET_N	Reset	Input	Low	
Pulse Width Modulation Controller - PWMA				
PWMA35 - PWMA0	PWMA channel waveforms	Output		
PWMAOD35 - PWMAOD0	PWMA channel waveforms, open drain mode	Output		Not all channels support open drain mode
System Control Interface - SCIF				
GCLK4 - GCLK0	Generic Clock Output	Output		
GCLK_IN1 - GCLK_IN0	Generic Clock Input	Input		
RC32OUT	RC32K output at startup	Output		
XIN0	Crystal 0 Input	Analog/ Digital		
XIN32	Crystal 32 Input (primary location)	Analog/ Digital		
XIN32_2	Crystal 32 Input (secondary location)	Analog/ Digital		
XOUT0	Crystal 0 Output	Analog		
XOUT32	Crystal 32 Output (primary location)	Analog		
XOUT32_2	Crystal 32 Output (secondary location)	Analog		
Serial Peripheral Interface - SPI				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
NPCS3 - NPCS0	SPI Peripheral Chip Select	I/O	Low	
SCK	Clock	I/O		
Timer/Counter - TC0, TC1				
A0	Channel 0 Line A	I/O		
A1	Channel 1 Line A	I/O		
A2	Channel 2 Line A	I/O		
B0	Channel 0 Line B	I/O		
B1	Channel 1 Line B	I/O		
B2	Channel 2 Line B	I/O		
CLK0	Channel 0 External Clock Input	Input		
CLK1	Channel 1 External Clock Input	Input		
CLK2	Channel 2 External Clock Input	Input		
Two-wire Interface - TWIMS0, TWIMS1				
TWALM	SMBus SMBALERT	I/O	Low	
TWCK	Two-wire Serial Clock	I/O		
TWD	Two-wire Serial Data	I/O		

Table 3-7. Signal Descriptions List

Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2, USART3				
CLK	Clock	I/O		
CTS	Clear To Send	Input	Low	
RTS	Request To Send	Output	Low	
RXD	Receive Data	Input		
TXD	Transmit Data	Output		

Note: 1. ADCIFB: AD3 does not exist.

Table 3-8. Signal Description List, Continued

Signal Name	Function	Type	Active Level	Comments
Power				
VDDCORE	Core Power Supply / Voltage Regulator Output	Power Input/Output		1.62V to 1.98V
VDDIO	I/O Power Supply	Power Input		1.62V to 3.6V. VDDIO should always be equal to or lower than VDDIN.
VDDANA	Analog Power Supply	Power Input		1.62V to 1.98V
ADVREFP	Analog Reference Voltage	Power Input		1.62V to 1.98V
VDDIN	Voltage Regulator Input	Power Input		1.62V to 3.6V (1)
GNDANA	Analog Ground	Ground		
GND	Ground	Ground		
Auxiliary Port - AUX				
MCKO	Trace Data Output Clock	Output		
MDO5 - MDO0	Trace Data Output	Output		
MSEO1 - MSEO0	Trace Frame Control	Output		
EVTI_N	Event In	Input	Low	
EVTO_N	Event Out	Output	Low	
General Purpose I/O pin				
PA22 - PA00	Parallel I/O Controller I/O Port 0	I/O		
PB12 - PB00	Parallel I/O Controller I/O Port 1	I/O		

1. See Section 6.1 on page 36

3.4 I/O Line Considerations

3.4.1 JTAG Pins

The JTAG is enabled if TCK is low while the RESET_N pin is released. The TCK, TMS, and TDI pins have pull-up resistors when JTAG is enabled. The TCK pin always has pull-up enabled during reset. The TDO pin is an output, driven at VDDIO, and has no pull-up resistor. The JTAG pins can be used as GPIO pins and multiplexed with peripherals when the JTAG is disabled. Please refer to Section 3.2.4 on page 11 for the JTAG port connections.

3.4.2 PA00

Note that PA00 is multiplexed with TCK. PA00 GPIO function must only be used as output in the application.

3.4.3 RESET_N Pin

The RESET_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIN. As the product integrates a power-on reset detector, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

The RESET_N pin is also used for the aWire debug protocol. When the pin is used for debugging, it must not be driven by external circuitry.

3.4.4 TWI Pins PA21/PB04/PB05

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with spike filtering. When used as GPIO pins or used for other peripherals, the pins have the same characteristics as other GPIO pins. Selected pins are also SMBus compliant (refer to Section 3.2.1 on page 8). As required by the SMBus specification, these pins provide no leakage path to ground when the AT32UC3L0128/256 is powered down. This allows other devices on the SMBus to continue communicating even though the AT32UC3L0128/256 is not powered.

After reset a TWI function is selected on these pins instead of the GPIO. Please refer to the GPIO Module Configuration chapter for details.

3.4.5 TWI Pins PA05/PA07/PA17

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with spike filtering. When used as GPIO pins or used for other peripherals, the pins have the same characteristics as other GPIO pins.

After reset a TWI function is selected on these pins instead of the GPIO. Please refer to the GPIO Module Configuration chapter for details.

3.4.6 GPIO Pins

All the I/O lines integrate a pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the GPIO Controllers. After reset, I/O lines default as inputs with pull-up resistors disabled, except PA00 which has the pull-up resistor enabled. PA20 selects SCIF-RC32OUT (GPIO Function F) as default enabled after reset.

3.4.7 High-drive Pins

The five pins PA02, PA06, PA08, PA09, and PB01 have high-drive output capabilities. Refer to Section 32. on page 791 for electrical characteristics.

3.4.8 RC32OUT Pin

3.4.8.1 Clock output at startup

After power-up, the clock generated by the 32kHz RC oscillator (RC32K) will be output on PA20, even when the device is still reset by the Power-On Reset Circuitry. This clock can be used by the system to start other devices or to clock a switching regulator to rise the power supply voltage up to an acceptable value.

The clock will be available on PA20, but will be disabled if one of the following conditions are true:

- PA20 is configured to use a GPIO function other than F (SCIF-RC32OUT)
- PA20 is configured as a General Purpose Input/Output (GPIO)
- The bit FRC32 in the Power Manager PPCR register is written to zero (refer to the Power Manager chapter)

The maximum amplitude of the clock signal will be defined by VDDIN.

Once the RC32K output on PA20 is disabled it can never be enabled again.

3.4.8.2 XOUT32_2 function

PA20 selects RC32OUT as default enabled after reset. This function is not automatically disabled when the user enables the XOUT32_2 function on PA20. This disturbs the oscillator and may result in the wrong frequency. To avoid this, RC32OUT must be disabled when XOUT32_2 is enabled.

3.4.9 ADC Input Pins

These pins are regular I/O pins powered from the VDDIO. However, when these pins are used for ADC inputs, the voltage applied to the pin must not exceed 1.98V. Internal circuitry ensures that the pin cannot be used as an analog input pin when the I/O drives to VDD. When the pins are not used for ADC inputs, the pins may be driven to the full I/O voltage range.

4. Mechanical Characteristics

4.1 Thermal Considerations

4.1.1 Thermal Data

Table 4-1 summarizes the thermal resistance data depending on the package.

Table 4-1. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP48	54.4	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP48	15.7	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	QFN48	26.0	°C/W
θ_{JC}	Junction-to-case thermal resistance		QFN48	1.6	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TLLGA48	25.4	°C/W
θ_{JC}	Junction-to-case thermal resistance		TLLGA48	12.7	

4.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

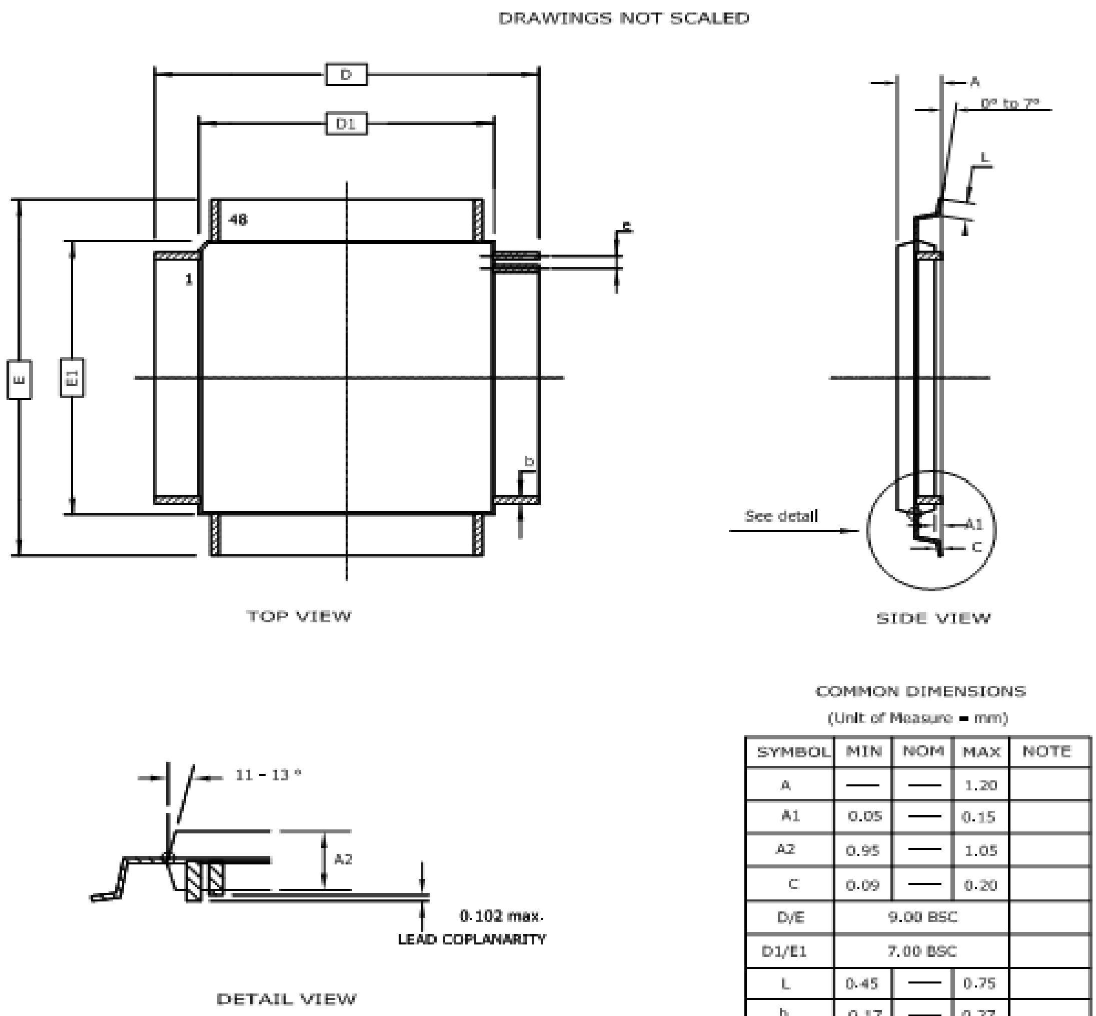
where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 4-1.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 4-1.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in Section 32.4 on page 792.
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

4.2 Package Drawings

Figure 4-1. TQFP-48 Package Drawing



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.95	—	1.05	
C	0.09	—	0.20	
D/E	9.00 BSC			
D1/E1	7.00 BSC			
L	0.45	—	0.75	
b	0.17	—	0.27	
e	0.50 BSC			

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

10/04/2011

Table 4-2. Device and Package Maximum Weight

140	mg

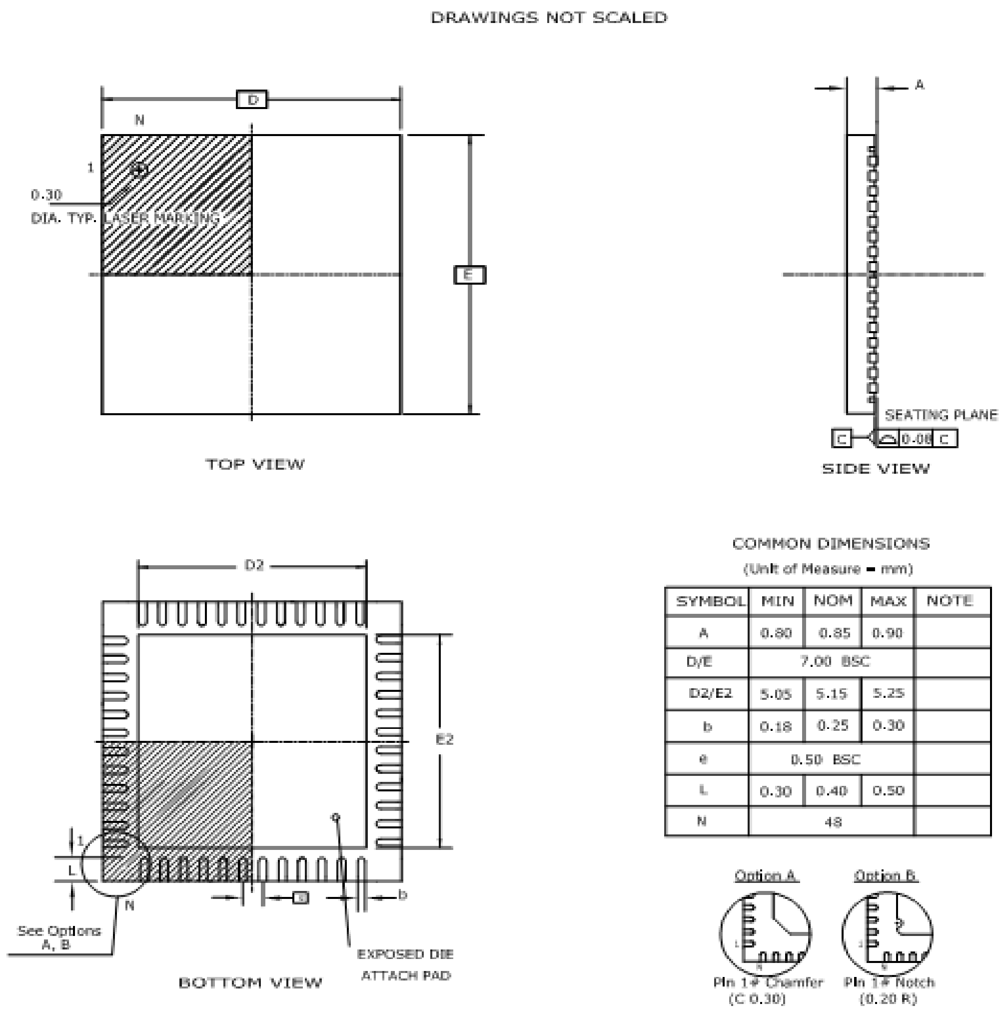
Table 4-3. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 4-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 4-2. QFN-48 Package Drawing



SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
D/E	7.00 BSC			
D2/E2	5.05	5.15	5.25	
b	0.18	0.25	0.30	
e	0.50 BSC			
L	0.30	0.40	0.50	
N	48			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VKKD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

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Note: The exposed pad is not connected to anything internally, but should be soldered to ground to increase board level reliability.

Table 4-5. Device and Package Maximum Weight

140	mg

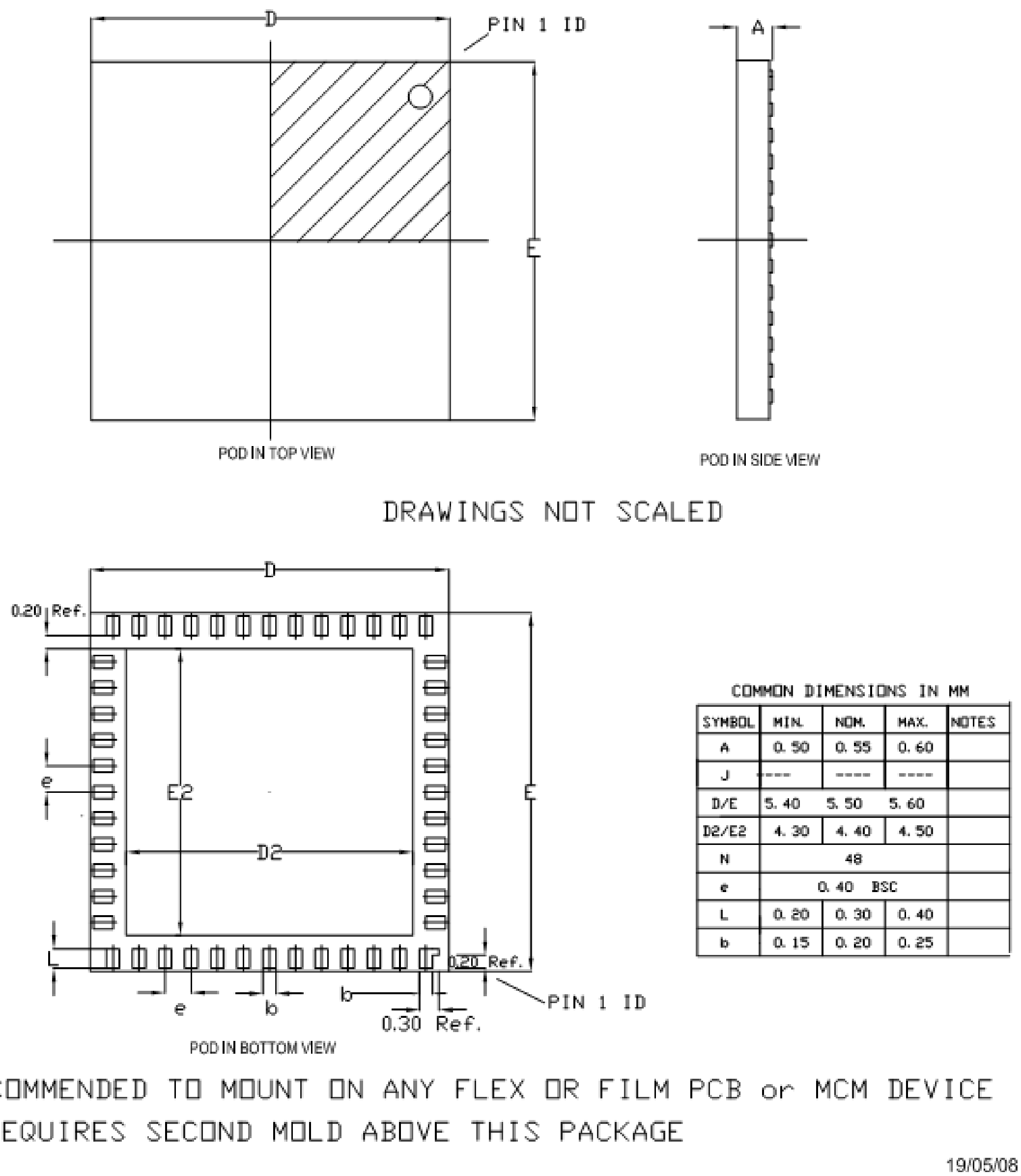
Table 4-6. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 4-7. Package Reference

JEDEC Drawing Reference	M0-220
JESD97 Classification	E3

Figure 4-3. TLLGA-48 Package Drawing



SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.50	0.55	0.60	
J	----	----	----	
D/E	5.40	5.50	5.60	
D2/E2	4.30	4.40	4.50	
N		48		
e		0.40 BSC		
L	0.20	0.30	0.40	
b	0.15	0.20	0.25	

Table 4-8. Device and Package Maximum Weight

39.3	mg

Table 4-9. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 4-10. Package Reference

JEDEC Drawing Reference	N/A
JESD97 Classification	E4

4.3 Soldering Profile

Table 4-11 gives the recommended soldering profile from J-STD-20.

Table 4-11. Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150 s
Time within 5°C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

A maximum of three reflow passes is allowed per component.

5. Ordering Information

Table 5-1. Ordering Information

Device	Ordering Code	Carrier Type	Package	Package Type	Temperature Operating Range
AT32UC3L0256	AT32UC3L0256-AUTES	ES	TQFP 48	JESD97 Classification E3	Industrial (-40°C to 85°C)
	AT32UC3L0256-AUT	Tray			
	AT32UC3L0256-AUR	Tape & Reel			
	AT32UC3L0256-ZAUTES	ES	QFN 48		
	AT32UC3L0256-ZAUT	Tray			
	AT32UC3L0256-ZAUR	Tape & Reel			
	AT32UC3L0256-D3HES	ES	TLLGA 48	JESD97 Classification E4	
	AT32UC3L0256-D3HT	Tray			
	AT32UC3L0256-D3HR	Tape & Reel			
AT32UC3L0128	AT32UC3L0128-AUT	Tray	TQFP 48	JESD97 Classification E3	
	AT32UC3L0128-AUR	Tape & Reel			
	AT32UC3L0128-ZAUT	Tray	QFN 48		
	AT32UC3L0128-ZAUR	Tape & Reel			
	AT32UC3L0128-D3HT	Tray	TLLGA 48	JESD97 Classification E4	
	AT32UC3L0128-D3HR	Tape & Reel			

6. Errata

6.1 Rev. C

6.1.1 SCIF

1. **The RC32K output on PA20 is not always permanently disabled**
The RC32K output on PA20 may sometimes re-appear.
Fix/Workaround
Before using RC32K for other purposes, the following procedure has to be followed in order to properly disable it:
- Run the CPU on RCSYS
- Disable the output to PA20 by writing a zero to PM.PPCR.RC32OUT
- Enable RC32K by writing a one to SCIF.RC32KCR.EN, and wait for this bit to be read as one
- Disable RC32K by writing a zero to SCIF.RC32KCR.EN, and wait for this bit to be read as zero.

2. **PLLCOUNT value larger than zero can cause PLLEN glitch**
Initializing the PLLCOUNT with a value greater than zero creates a glitch on the PLLEN signal during asynchronous wake up.
Fix/Workaround
The lock-masking mechanism for the PLL should not be used.
The PLLCOUNT field of the PLL Control Register should always be written to zero.

3. **Writing 0x5A5A5A5A to the SCIF memory range will enable the SCIF UNLOCK feature**
The SCIF UNLOCK feature will be enabled if the value 0x5A5A5A5A is written to any location in the SCIF memory range.
Fix/Workaround
None.

6.1.2 SPI

1. **SPI data transfer hangs with CSR0.CSAAT==1 and MR.MODFDIS==0**
When CSR0.CSAAT==1 and mode fault detection is enabled (MR.MODFDIS==0), the SPI module will not start a data transfer.
Fix/Workaround
Disable mode fault detection by writing a one to MR.MODFDIS.

2. **Disabling SPI has no effect on the SR.TDRE bit**
Disabling SPI has no effect on the SR.TDRE bit whereas the write data command is filtered when SPI is disabled. Writing to TDR when SPI is disabled will not clear SR.TDRE. If SPI is disabled during a PDCA transfer, the PDCA will continue to write data to TDR until its buffer is empty, and this data will be lost.
Fix/Workaround
Disable the PDCA, add two NOPs, and disable the SPI. To continue the transfer, enable the SPI and PDCA.

3. **SPI disable does not work in SLAVE mode**
SPI disable does not work in SLAVE mode.
Fix/Workaround
Read the last received data, then perform a software reset by writing a one to the Software Reset bit in the Control Register (CR.SWRST).

4. **SPI bad serial clock generation on 2nd chip_select when SCBR=1, CPOL=1, and NCPHA=0**
When multiple chip selects (CS) are in use, if one of the baudrates equal 1 while one (CSRn.SCBR=1) of the others do not equal 1, and CSRn.CPOL=1 and CSRn.NCPHA=0, then an additional pulse will be generated on SCK.
Fix/Workaround
When multiple CS are in use, if one of the baudrates equals 1, the others must also equal 1 if CSRn.CPOL=1 and CSRn.NCPHA=0.

5. **SPI mode fault detection enable causes incorrect behavior**
When mode fault detection is enabled (MR.MODFDIS==0), the SPI module may not operate properly.
Fix/Workaround
Always disable mode fault detection before using the SPI by writing a one to MR.MODFDIS.

6. **SPI RDR.PCS is not correct**
The PCS (Peripheral Chip Select) field in the SPI RDR (Receive Data Register) does not correctly indicate the value on the NPCS pins at the end of a transfer.
Fix/Workaround
Do not use the PCS field of the SPI RDR.

6.1.3 TWI

1. **SMBALERT bit may be set after reset**
The SMBus Alert (SMBALERT) bit in the Status Register (SR) might be erroneously set after system reset.
Fix/Workaround
After system reset, clear the SR.SMBALERT bit before commencing any TWI transfer.

2. **Clearing the NAK bit before the BTF bit is set locks up the TWI bus**
When the TWIS is in transmit mode, clearing the NAK Received (NAK) bit of the Status Register (SR) before the end of the Acknowledge/Not Acknowledge cycle will cause the TWIS to attempt to continue transmitting data, thus locking up the bus.
Fix/Workaround
Clear SR.NAK only after the Byte Transfer Finished (BTF) bit of the same register has been set.

6.1.4 TC

1. **Channel chaining skips first pulse for upper channel**
When chaining two channels using the Block Mode Register, the first pulse of the clock between the channels is skipped.
Fix/Workaround
Configure the lower channel with RA = 0x1 and RC = 0x2 to produce a dummy clock cycle for the upper channel. After the dummy cycle has been generated, indicated by the SR.CPCS bit, reconfigure the RA and RC registers for the lower channel with the real values.

6.1.5 CAT

1. **CAT QMatrix sense capacitors discharged prematurely**
At the end of a QMatrix burst charging sequence that uses different burst count values for different Y lines, the Y lines may be incorrectly grounded for up to n-1 periods of the periph-

eral bus clock, where n is the ratio of the PB clock frequency to the GCLK_CAT frequency. This results in premature loss of charge from the sense capacitors and thus increased variability of the acquired count values.
Fix/Workaround
Enable the 1 kOhm drive resistors on all implemented QMatrix Y lines (CSA 1, 3, 5, 7, 9, 11, 13, and/or 15) by writing ones to the corresponding odd bits of the CSARES register.

2. **Autonomous CAT acquisition must be longer than AST source clock period**
When using the AST to trigger CAT autonomous touch acquisition in sleep modes where the CAT bus clock is turned off, the CAT will start several acquisitions if the period of the AST source clock is larger than one CAT acquisition. One AST clock period after the AST trigger, the CAT clock will automatically stop and the CAT acquisition can be stopped prematurely, ruining the result.
Fix/Workaround
Always ensure that the ATCFG1.max field is set so that the duration of the autonomous touch acquisition is greater than one clock period of the AST source clock.

6.1.6 aWire

1. **aWire MEMORY_SPEED_REQUEST command does not return correct CV**
The aWire MEMORY_SPEED_REQUEST command does not return a CV corresponding to the formula in the aWire Debug Interface chapter.
Fix/Workaround
Issue a dummy read to address 0x100000000 before issuing the MEMORY_SPEED_REQUEST command and use this formula instead:

$$f_{sab} = \frac{7f_{aw}}{CV-3}$$

6.1.7 Flash

1. **Corrupted data in flash may happen after flash page write operations**
After a flash page write operation from an external in situ programmer, reading (data read or code fetch) in flash may fail. This may lead to an exception or to others errors derived from this corrupted read access.
Fix/Workaround
Before any flash page write operation, each write in the page buffer must preceded by a write in the page buffer with 0xFFFF_FFFF content at any address in the page.

6.2 Rev. B

6.2.1 SCIF

1. **The RC32K output on PA20 is not always permanently disabled**
The RC32K output on PA20 may sometimes re-appear.
Fix/Workaround
Before using RC32K for other purposes, the following procedure has to be followed in order to properly disable it:
- Run the CPU on RCSYS
- Disable the output to PA20 by writing a zero to PM.PPCR.RC32OUT
- Enable RC32K by writing a one to SCIF.RC32KCR.EN, and wait for this bit to be read as one

- Disable RC32K by writing a zero to SCIF.RC32KCR.EN, and wait for this bit to be read as zero.

2. **PLLCOUNT value larger than zero can cause PLLEN glitch**
Initializing the PLLCOUNT with a value greater than zero creates a glitch on the PLLEN signal during asynchronous wake up.
Fix/Workaround
The lock-masking mechanism for the PLL should not be used.
The PLLCOUNT field of the PLL Control Register should always be written to zero.

3. **Writing 0x5A5A5A5A to the SCIF memory range will enable the SCIF UNLOCK feature**
The SCIF UNLOCK feature will be enabled if the value 0x5A5A5A5A is written to any location in the SCIF memory range.
Fix/Workaround
None.

6.2.2 WDT

1. **WDT Control Register does not have synchronization feedback**
When writing to the Timeout Prescale Select (PSEL), Time Ban Prescale Select (TBAN), Enable (EN), or WDT Mode (MODE) fieldss of the WDT Control Register (CTRL), a synchronizer is started to propagate the values to the WDT clcok domain. This synchronization takes a finite amount of time, but only the status of the synchronization of the EN bit is reflected back to the user. Writing to the synchronized fields during synchronization can lead to undefined behavior.
Fix/Workaround
-When writing to the affected fields, the user must ensure a wait corresponding to 2 clock cycles of both the WDT peripheral bus clock and the selected WDT clock source.
-When doing writes that changes the EN bit, the EN bit can be read back until it reflects the written value.

6.2.3 SPI

1. **SPI data transfer hangs with CSR0.CSAAT==1 and MR.MODFDIS==0**
When CSR0.CSAAT==1 and mode fault detection is enabled (MR.MODFDIS==0), the SPI module will not start a data transfer.
Fix/Workaround
Disable mode fault detection by writing a one to MR.MODFDIS.

2. **Disabling SPI has no effect on the SR.TDRE bit**
Disabling SPI has no effect on the SR.TDRE bit whereas the write data command is filtered when SPI is disabled. Writing to TDR when SPI is disabled will not clear SR.TDRE. If SPI is disabled during a PDCA transfer, the PDCA will continue to write data to TDR until its buffer is empty, and this data will be lost.
Fix/Workaround
Disable the PDCA, add two NOPs, and disable the SPI. To continue the transfer, enable the SPI and PDCA.

3. **SPI disable does not work in SLAVE mode**
SPI disable does not work in SLAVE mode.
Fix/Workaround
Read the last received data, then perform a software reset by writing a one to the Software Reset bit in the Control Register (CR.SWRST).

4. **SPI bad serial clock generation on 2nd chip_select when SCBR=1, CPOL=1, and NCPHA=0**
   When multiple chip selects (CS) are in use, if one of the baudrates equal 1 while one (CSRn.SCBR=1) of the others do not equal 1, and CSRn.CPOL=1 and CSRn.NCPHA=0, then an additional pulse will be generated on SCK.
   Fix/Workaround
   When multiple CS are in use, if one of the baudrates equals 1, the others must also equal 1 if CSRn.CPOL=1 and CSRn.NCPHA=0.

5. **SPI mode fault detection enable causes incorrect behavior**
   When mode fault detection is enabled (MR.MODFDIS==0), the SPI module may not operate properly.
   Fix/Workaround
   Always disable mode fault detection before using the SPI by writing a one to MR.MODFDIS.

6. **SPI RDR.PCS is not correct**
   The PCS (Peripheral Chip Select) field in the SPI RDR (Receive Data Register) does not correctly indicate the value on the NPCS pins at the end of a transfer.
   Fix/Workaround
   Do not use the PCS field of the SPI RDR.

6.2.4 TWI

1. **TWIS may not wake the device from sleep mode**
   If the CPU is put to a sleep mode (except Idle and Frozen) directly after a TWI Start condition, the CPU may not wake upon a TWIS address match. The request is NACKed.
   Fix/Workaround
   When using the TWI address match to wake the device from sleep, do not switch to sleep modes deeper than Frozen. Another solution is to enable asynchronous EIC wake on the TWIS clock (TWCK) or TWIS data (TWD) pins, in order to wake the system up on bus events.

2. **SMBALERT bit may be set after reset**
   The SMBus Alert (SMBALERT) bit in the Status Register (SR) might be erroneously set after system reset.
   Fix/Workaround
   After system reset, clear the SR.SMBALERT bit before commencing any TWI transfer.

3. **Clearing the NAK bit before the BTF bit is set locks up the TWI bus**
   When the TWIS is in transmit mode, clearing the NAK Received (NAK) bit of the Status Register (SR) before the end of the Acknowledge/Not Acknowledge cycle will cause the TWIS to attempt to continue transmitting data, thus locking up the bus.
   Fix/Workaround
   Clear SR.NAK only after the Byte Transfer Finished (BTF) bit of the same register has been set.

6.2.5 PWMA

1. **The SR.READY bit cannot be cleared by writing to SCR.READY**
   The Ready bit in the Status Register will not be cleared when writing a one to the corresponding bit in the Status Clear register. The Ready bit will be cleared when the Busy bit is set.
   Fix/Workaround

Disable the Ready interrupt in the interrupt handler when receiving the interrupt. When an operation that triggers the Busy/Ready bit is started, wait until the ready bit is low in the Status Register before enabling the interrupt.

6.2.6 TC

1. **Channel chaining skips first pulse for upper channel**
   When chaining two channels using the Block Mode Register, the first pulse of the clock between the channels is skipped.
   Fix/Workaround
   Configure the lower channel with RA = 0x1 and RC = 0x2 to produce a dummy clock cycle for the upper channel. After the dummy cycle has been generated, indicated by the SR.CPCS bit, reconfigure the RA and RC registers for the lower channel with the real values.

6.2.7 CAT

1. **CAT QMatrix sense capacitors discharged prematurely**
   At the end of a QMatrix burst charging sequence that uses different burst count values for different Y lines, the Y lines may be incorrectly grounded for up to n-1 periods of the peripheral bus clock, where n is the ratio of the PB clock frequency to the GCLK_CAT frequency. This results in premature loss of charge from the sense capacitors and thus increased variability of the acquired count values.
   Fix/Workaround
   Enable the 1kOhm drive resistors on all implemented QMatrix Y lines (CSA 1, 3, 5, 7, 9, 11, 13, and/or 15) by writing ones to the corresponding odd bits of the CSARES register.

2. **Autonomous CAT acquisition must be longer than AST source clock period**
   When using the AST to trigger CAT autonomous touch acquisition in sleep modes where the CAT bus clock is turned off, the CAT will start several acquisitions if the period of the AST source clock is larger than one CAT acquisition. One AST clock period after the AST trigger, the CAT clock will automatically stop and the CAT acquisition can be stopped prematurely, ruining the result.
   Fix/Workaround
   Always ensure that the ATCFG1.max field is set so that the duration of the autonomous touch acquisition is greater than one clock period of the AST source clock.

3. **CAT consumes unnecessary power when disabled or when autonomous touch not used**
   A CAT prescaler controlled by the ATCFG0.DIV field will be active even when the CAT module is disabled or when the autonomous touch feature is not used, thereby causing unnecessary power consumption.
   Fix/Workaround
   If the CAT module is not used, disable the CLK_CAT clock in the PM module. If the CAT module is used but the autonomous touch feature is not used, the power consumption of the CAT module may be reduced by writing 0xFFFF to the ATCFG0.DIV field.

6.2.8 aWire

1. **aWire MEMORY_SPEED_REQUEST command does not return correct CV**
   The aWire MEMORY_SPEED_REQUEST command does not return a CV corresponding to the formula in the aWire Debug Interface chapter.
   Fix/Workaround

Issue a dummy read to address 0x100000000 before issuing the MEMORY_SPEED_REQUEST command and use this formula instead:

$$f_{sab} = \frac{7f_{aw}}{CV-3}$$

6.2.9 Flash

1. **Corrupted data in flash may happen after flash page write operations**
   After a flash page write operation from an external in situ programmer, reading (data read or code fetch) in flash may fail. This may lead to an exception or to others errors derived from this corrupted read access.
   Fix/Workaround
   Before any flash page write operation, each write in the page buffer must preceded by a write in the page buffer with 0xFFFF_FFFF content at any address in the page.

6.3 Rev. A

6.3.1 Device

1. **JTAGID is wrong**
   The JTAGID is 0x021DF03F.
   Fix/Workaround
   None.

6.3.2 FLASHCDW

1. **General-purpose fuse programming does not work**
   The general-purpose fuses cannot be programmed and are stuck at 1. Please refer to the Fuse Settings chapter in the FLASHCDW for more information about what functions are affected.
   Fix/Workaround
   None.

2. **Set Security Bit command does not work**
   The Set Security Bit (SSB) command of the FLASHCDW does not work. The device cannot be locked from external JTAG, aWire, or other debug accesses.
   Fix/Workaround
   None.

3. **Flash programming time is longer than specified**

The flash programming time is now:

Table 6-1. Flash Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{FPP}	Page programming time	f_{CLK_HSB}= 50MHz		7.5		ms
T_{FPE}	Page erase time			7.5		
T_{FFP}	Fuse programming time			1		
T_{FEA}	Full chip erase time (EA)			9		
T_{FCE}	JTAG chip erase time (CHIP_ERASE)	f_{CLK_HSB}= 115kHz		250		

Fix/Workaround
None.

4. **Power Manager**

5. **Clock Failure Detector (CFD) can be issued while turning off the CFD**
While turning off the CFD, the CFD bit in the Status Register (SR) can be set. This will change the main clock source to RCSYS.
Fix/Workaround
Solution 1: Enable CFD interrupt. If CFD interrupt is issues after turning off the CFD, switch back to original main clock source.
Solution 2: Only turn off the CFD while running the main clock on RCSYS.

6. **Sleepwalking in idle and frozen sleep mode will mask all other PB clocks**
If the CPU is in idle or frozen sleep mode and a module is in a state that triggers sleep walking, all PB clocks will be masked except the PB clock to the sleepwalking module.
Fix/Workaround
Mask all clock requests in the PM.PPCR register before going into idle or frozen mode.

2. **Unused PB clocks are running**
Three unused PBA clocks are enabled by default and will cause increased active power consumption.
Fix/Workaround
Disable the clocks by writing zeroes to bits [27:25] in the PBA clock mask register.

6.3.3 SCIF

1. **The RC32K output on PA20 is not always permanently disabled**
The RC32K output on PA20 may sometimes re-appear.
Fix/Workaround
Before using RC32K for other purposes, the following procedure has to be followed in order to properly disable it:
- Run the CPU on RCSYS
- Disable the output to PA20 by writing a zero to PM.PPCR.RC32OUT
- Enable RC32K by writing a one to SCIF.RC32KCR.EN, and wait for this bit to be read as one
- Disable RC32K by writing a zero to SCIF.RC32KCR.EN, and wait for this bit to be read as zero.

2. **PLL lock might not clear after disable**

Under certain circumstances, the lock signal from the Phase Locked Loop (PLL) oscillator may not go back to zero after the PLL oscillator has been disabled. This can cause the propagation of clock signals with the wrong frequency to parts of the system that use the PLL clock.

Fix/Workaround

PLL must be turned off before entering STOP, DEEPSTOP or STATIC sleep modes. If PLL has been turned off, a delay of 30us must be observed after the PLL has been enabled again before the SCIF.PLL0LOCK bit can be used as a valid indication that the PLL is locked.

3. **PLLCOUNT value larger than zero can cause PLLEN glitch**

Initializing the PLLCOUNT with a value greater than zero creates a glitch on the PLLEN signal during asynchronous wake up.

Fix/Workaround

The lock-masking mechanism for the PLL should not be used.
The PLLCOUNT field of the PLL Control Register should always be written to zero.

4. **RCSYS is not calibrated**

The RCSYS is not calibrated and will run faster than 115.2kHz. Frequencies around 150kHz can be expected.

Fix/Workaround

If a known clock source is available the RCSYS can be runtime calibrated by using the frequency meter (FREQM) and tuning the RCSYS by writing to the RCCR register in SCIF.

5. **Writing 0x5A5A5A5A to the SCIF memory range will enable the SCIF UNLOCK feature**

The SCIF UNLOCK feature will be enabled if the value 0x5A5A5A5A is written to any location in the SCIF memory range.

Fix/Workaround

None.

6.3.4 WDT

1. **Clearing the Watchdog Timer (WDT) counter in second half of timeout period will issue a Watchdog reset**

If the WDT counter is cleared in the second half of the timeout period, the WDT will immediately issue a Watchdog reset.

Fix/Workaround

Use twice as long timeout period as needed and clear the WDT counter within the first half of the timeout period. If the WDT counter is cleared after the first half of the timeout period, you will get a Watchdog reset immediately. If the WDT counter is not cleared at all, the time before the reset will be twice as long as needed.

2. **WDT Control Register does not have synchronization feedback**

When writing to the Timeout Prescale Select (PSEL), Time Ban Prescale Select (TBAN), Enable (EN), or WDT Mode (MODE) fieldss of the WDT Control Register (CTRL), a synchronizer is started to propagate the values to the WDT clcok domain. This synchronization takes a finite amount of time, but only the status of the synchronization of the EN bit is reflected back to the user. Writing to the synchronized fields during synchronization can lead to undefined behavior.

Fix/Workaround

-When writing to the affected fields, the user must ensure a wait corresponding to 2 clock cycles of both the WDT peripheral bus clock and the selected WDT clock source.
-When doing writes that changes the EN bit, the EN bit can be read back until it reflects the written value.

6.3.5 GPIO

1. **Clearing Interrupt flags can mask other interrupts**
   When clearing interrupt flags in a GPIO port, interrupts on other pins of that port, happening in the same clock cycle will not be registered.
   Fix/Workaround
   Read the PVR register of the port before and after clearing the interrupt to see if any pin change has happened while clearing the interrupt. If any change occurred in the PVR between the reads, they must be treated as an interrupt.

6.3.6 SPI

1. **SPI data transfer hangs with CSR0.CSAAT==1 and MR.MODFDIS==0**
   When CSR0.CSAAT==1 and mode fault detection is enabled (MR.MODFDIS==0), the SPI module will not start a data transfer.
   Fix/Workaround
   Disable mode fault detection by writing a one to MR.MODFDIS.

2. **Disabling SPI has no effect on the SR.TDRE bit**
   Disabling SPI has no effect on the SR.TDRE bit whereas the write data command is filtered when SPI is disabled. Writing to TDR when SPI is disabled will not clear SR.TDRE. If SPI is disabled during a PDCA transfer, the PDCA will continue to write data to TDR until its buffer is empty, and this data will be lost.
   Fix/Workaround
   Disable the PDCA, add two NOPs, and disable the SPI. To continue the transfer, enable the SPI and PDCA.

3. **SPI disable does not work in SLAVE mode**
   SPI disable does not work in SLAVE mode.
   Fix/Workaround
   Read the last received data, then perform a software reset by writing a one to the Software Reset bit in the Control Register (CR.SWRST).

4. **SPI bad serial clock generation on 2nd chip_select when SCBR=1, CPOL=1, and NCPHA=0**
   When multiple chip selects (CS) are in use, if one of the baudrates equal 1 while one (CSRn.SCBR=1) of the others do not equal 1, and CSRn.CPOL=1 and CSRn.NCPHA=0, then an additional pulse will be generated on SCK.
   Fix/Workaround
   When multiple CS are in use, if one of the baudrates equals 1, the others must also equal 1 if CSRn.CPOL=1 and CSRn.NCPHA=0.

5. **SPI mode fault detection enable causes incorrect behavior**
   When mode fault detection is enabled (MR.MODFDIS==0), the SPI module may not operate properly.
   Fix/Workaround
   Always disable mode fault detection before using the SPI by writing a one to MR.MODFDIS.

6. **SPI RDR.PCS is not correct**
   The PCS (Peripheral Chip Select) field in the SPI RDR (Receive Data Register) does not correctly indicate the value on the NPCS pins at the end of a transfer.
   Fix/Workaround
   Do not use the PCS field of the SPI RDR.

6.3.7 TWI

1. **TWIS may not wake the device from sleep mode**
If the CPU is put to a sleep mode (except Idle and Frozen) directly after a TWI Start condition, the CPU may not wake upon a TWIS address match. The request is NACKed.
Fix/Workaround
When using the TWI address match to wake the device from sleep, do not switch to sleep modes deeper than Frozen. Another solution is to enable asynchronous EIC wake on the TWIS clock (TWCK) or TWIS data (TWD) pins, in order to wake the system up on bus events.

2. **SMBALERT bit may be set after reset**
The SMBus Alert (SMBALERT) bit in the Status Register (SR) might be erroneously set after system reset.
Fix/Workaround
After system reset, clear the SR.SMBALERT bit before commencing any TWI transfer.

3. **Clearing the NAK bit before the BTF bit is set locks up the TWI bus**
When the TWIS is in transmit mode, clearing the NAK Received (NAK) bit of the Status Register (SR) before the end of the Acknowledge/Not Acknowledge cycle will cause the TWIS to attempt to continue transmitting data, thus locking up the bus.
Fix/Workaround
Clear SR.NAK only after the Byte Transfer Finished (BTF) bit of the same register has been set.

4. **TWIS stretch on Address match error**
When the TWIS stretches TWCK due to a slave address match, it also holds TWD low for the same duration if it is to be receiving data. When TWIS releases TWCK, it releases TWD at the same time. This can cause a TWI timing violation.
Fix/Workaround
None.

5. **TWIM TWALM polarity is wrong**
The TWALM signal in the TWIM is active high instead of active low.
Fix/Workaround
Use an external inverter to invert the signal going into the TWIM. When using both TWIM and TWIS on the same pins, the TWALM cannot be used.

6.3.8 PWMA

1. **The SR.READY bit cannot be cleared by writing to SCR.READY**
The Ready bit in the Status Register will not be cleared when writing a one to the corresponding bit in the Status Clear register. The Ready bit will be cleared when the Busy bit is set.
Fix/Workaround
Disable the Ready interrupt in the interrupt handler when receiving the interrupt. When an operation that triggers the Busy/Ready bit is started, wait until the ready bit is low in the Status Register before enabling the interrupt.

6.3.9 TC

1. **Channel chaining skips first pulse for upper channel**
When chaining two channels using the Block Mode Register, the first pulse of the clock between the channels is skipped.

Fix/Workaround

Configure the lower channel with RA = 0x1 and RC = 0x2 to produce a dummy clock cycle for the upper channel. After the dummy cycle has been generated, indicated by the SR.CPCS bit, reconfigure the RA and RC registers for the lower channel with the real values.

6.3.10 ADCIFB

1. **ADCIFB DMA transfer does not work with divided PBA clock**

   DMA requests from the ADCIFB will not be performed when the PBA clock is slower than the HSB clock.

   Fix/Workaround

   Do not use divided PBA clock when the PDCA transfers from the ADCIFB.

6.3.11 CAT

1. **CAT QMatrix sense capacitors discharged prematurely**

   At the end of a QMatrix burst charging sequence that uses different burst count values for different Y lines, the Y lines may be incorrectly grounded for up to n-1 periods of the peripheral bus clock, where n is the ratio of the PB clock frequency to the GCLK_CAT frequency. This results in premature loss of charge from the sense capacitors and thus increased variability of the acquired count values.

   Fix/Workaround

   Enable the 1kOhm drive resistors on all implemented QMatrix Y lines (CSA 1, 3, 5, 7, 9, 11, 13, and/or 15) by writing ones to the corresponding odd bits of the CSARES register.

2. **Autonomous CAT acquisition must be longer than AST source clock period**

   When using the AST to trigger CAT autonomous touch acquisition in sleep modes where the CAT bus clock is turned off, the CAT will start several acquisitions if the period of the AST source clock is larger than one CAT acquisition. One AST clock period after the AST trigger, the CAT clock will automatically stop and the CAT acquisition can be stopped prematurely, ruining the result.

   Fix/Workaround

   Always ensure that the ATCFG1.max field is set so that the duration of the autonomous touch acquisition is greater than one clock period of the AST source clock.

3. **CAT consumes unnecessary power when disabled or when autonomous touch not used**

   A CAT prescaler controlled by the ATCFG0.DIV field will be active even when the CAT module is disabled or when the autonomous touch feature is not used, thereby causing unnecessary power consumption.

   Fix/Workaround

   If the CAT module is not used, disable the CLK_CAT clock in the PM module. If the CAT module is used but the autonomous touch feature is not used, the power consumption of the CAT module may be reduced by writing 0xFFFF to the ATCFG0.DIV field.

4. **CAT module does not terminate QTouch burst on detect**

   The CAT module does not terminate a QTouch burst when the detection voltage is reached on the sense capacitor. This can cause the sense capacitor to be charged more than necessary. Depending on the dielectric absorption characteristics of the capacitor, this can lead to unstable measurements.

   Fix/Workaround

   Use the minimum possible value for the MAX field in the ATCFG1, TG0CFG1, and TG1CFG1 registers.

6.3.12 aWire

1. **aWire MEMORY_SPEED_REQUEST command does not return correct CV**
   The aWire MEMORY_SPEED_REQUEST command does not return a CV corresponding to the formula in the aWire Debug Interface chapter.
   Fix/Workaround
   Issue a dummy read to address 0x100000000 before issuing the MEMORY_SPEED_REQUEST command and use this formula instead:

$$f_{sab} = \frac{7f_{aw}}{CV-3}$$

6.3.13 Flash

1. **Corrupted data in flash may happen after flash page write operations**
   After a flash page write operation from an external in situ programmer, reading (data read or code fetch) in flash may fail. This may lead to an exception or to others errors derived from this corrupted read access.
   Fix/Workaround
   Before any flash page write operation, each write in the page buffer must preceded by a write in the page buffer with 0xFFFF_FFFF content at any address in the page.

6.3.14 I/O Pins

1. **PA05 is not 3.3V tolerant.**
   PA05 should be grounded on the PCB and left unused if VDDIO is above 1.8V.
   Fix/Workaround
   None.

2. **No pull-up on pins that are not bonded**
   PB13 to PB27 are not bonded on UC3L0256/128, but has no pull-up and can cause current consumption on VDDIO/VDDIN if left undriven.
   Fix/Workaround
   Enable pull-ups on PB13 to PB27 by writing 0x0FFFE000 to the PUERS1 register in the GPIO.

3. **PA17 has low ESD tolerance**
   PA17 only tolerates 500V ESD pulses (Human Body Model).
   Fix/Workaround
   Care must be taken during manufacturing and PCB design.

7. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

7.1 Rev. C – 06/2013

1. Updated the datasheet with new Atmel blue logo and the last page.
2. Added Flash errata.

7.2 Rev. B – 01/2012

1. Description: DFLL frequency is 20 to 150MHz, not 40 to 150MHz.
2. Description: “One touch sensor can be configured to operate autonomously...” replaced by “All touch sensors can be configured to operate autonomously...”.
3. Block Diagram: GCLK_IN is input, not output, and is 2 bits wide (GCLK_IN[1..0]). CAT SMP corrected from I/O to output. SPI NPCS corrected from output to I/O.
4. Package and Pinout: PRND signal removed from Signal Descriptions List table and GPIO Controller Function Multiplexing table.
5. Supply and Startup Considerations: In 1.8V single supply mode figure, the input voltage is 1.62-1.98V, not 1.98-3.6V. “On system start-up, the DFLL is disabled” is replaced by “On system start-up, all high-speed clocks are disabled”.
6. ADCIFB: PRND signal removed from block diagram.
7. Electrical Characteristics: Added PLL source clock in the Clock Frequencies table in the Maximum Clock Frequencies section. Removed 64-pin package information from I/O Pin Characteristics tables and Digital Clock Characteristics table.
8. Electrical Characteristics: Removed USB Transceiver Characteristics, as the device contains no USB.
9. Mechanical Characteristics: Added notes to package drawings.
10. Summary: Removed Programming and Debugging chapter, added Processor and Architecture chapter.
11. Datasheet Revision History: Corrected release date for datasheet rev. A; the correct date is 12/2011.

7.3 Rev. A – 12/2011

1. Initial revision.

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