

16-bit bus transceiver (3-State)

74ABT16245B
74ABTH16245B

FEATURES

- 16-bit bidirectional bus interface
- Power-up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Output capability: +64 mA / -32 mA
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- Live insertion/extraction permitted
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- 74ABTH16245B incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
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DESCRIPTION

The 74ABT16245B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16245B device is a dual octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features two Output Enable ($1\overline{OE}$, $2\overline{OE}$) inputs for easy cascading and two Direction ($1DIR$, $2DIR$) inputs for direction control.

Two options are available, 74ABT16245B which does not have the bus hold feature and the 74ABTH16245B which incorporates the bus hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25\text{ }^{\circ}\text{C}$; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	$C_L = 50\text{ pF}$; $V_{CC} = 5\text{ V}$	2.0 2.3	ns
C_{IN}	Input capacitance	$V_I = 0\text{ V}$ or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	$V_O = 0\text{ V}$ or V_{CC} ; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{ V}$	500	μA
I_{CCL}		Output Low; $V_{CC} = 5.5\text{ V}$	10	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	PART NUMBER	DWG NUMBER
48-Pin Plastic SSOP Type III	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	74ABT16245BDL	SOT370-1
48-Pin Plastic TSSOP Type II	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	74ABT16245BDGG	SOT362-1
48-Pin Plastic SSOP Type III	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	74ABTH16245BDL	SOT370-1

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FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
nOE	nDIR	nAx	nBx
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

H = HIGH voltage level

L = LOW voltage level

X = Don't care

Z = High impedance "off" scale

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		−0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0 V	−18	mA
V _I	DC input voltage ³		−1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0 V	−50	mA
V _{OUT}	DC output voltage ³	output in Off or HIGH state	−0.5 to +5.5	V
I _{OUT}	DC output current	output in LOW state	128	mA
		output in HIGH state	−64	
T _{stg}	Storage temperature range		−65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	HIGH-level input voltage	2.0		V
V _{IL}	LOW-level Input voltage		0.8	V
I _{OH}	HIGH-level output current		−32	mA
I _{OL}	LOW-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _{amb}	Operating free-air temperature range	−40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T _{amb} = +25 °C			T _{amb} = −40 °C to +85 °C		
				Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5 V; I _{IK} = −18 mA			−0.9	−1.2		−1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5 V; I _{OH} = −3 mA; V _I = V _{IL} or V _{IH}		2.5	2.9		2.5		V
		V _{CC} = 5.0 V; I _{OH} = −3 mA; V _I = V _{IL} or V _{IH}		3.0	3.4		3.0		V
		V _{CC} = 4.5 V; I _{OH} = −32 mA; V _I = V _{IL} or V _{IH}		2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5 V; I _{OL} = 64 mA; V _I = V _{IL} or V _{IH}			0.42	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5 V; V _I = GND or 5.5 V	Control pins		±0.01	±1.0		±1.0	μA
I _{HOLD}	Bus hold current A and B inputs 74ABTH16245B	V _{CC} = 4.5 V; V _I = 0.8 V		50			50		μA
		V _{CC} = 5.5 V; V _I = 2.0 V		−75			−75		
		V _{CC} = 5.5 V; V _I = 0 to 5.5 V		±500					
I _{OFF}	Power-off leakage current	V _{CC} = 0.0 V; V _O or V _I ≤ 4.5 V			±5.0	±100		±100	μA
I _{PU} /I _{PD}	Power-up/down 3-State output current	V _{CC} = 2.0 V; V _O = 0.5 V; V _I = GND or V _{CC} ; V _{OE} = Don't care			±5.0	±50		±50	μA
I _{IH} +I _{OZH}	3-State output HIGH current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = V _{IL} or V _{IH}			0.1	10		10	μA
I _{IL} +I _{OZL}	3-State output LOW current	V _{CC} = 5.5 V; V _O = 0.0 V; V _I = V _{IL} or V _{IH}			0.1	10		10	μA
I _{CEX}	Output high leakage current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC}			5.0	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5 V; V _O = 2.5 V		−50	−92	−180	−50	−180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5 V; Outputs High, V _I = GND or V _{CC}			0.30	0.70		0.70	mA
I _{CCL}		V _{CC} = 5.5 V; Outputs Low, V _I = GND or V _{CC}			10	19		19	mA
I _{CCZ}		V _{CC} = 5.5 V; Outputs 3-State; V _I = GND or V _{CC}			0.30	0.70		0.70	mA
ΔI _{CC}	Additional supply current per input pin ²	Outputs enabled, one data input at 3.4 V, other inputs at V _{CC} or GND; V _{CC} = 5.5 V			400	700		700	μA
		Outputs disabled, one data input at 3.4 V, other inputs at V _{CC} or GND; V _{CC} = 5.5 V			100	250		250	μA
		Control pins, outputs disabled, one enable input at 3.4 V, other inputs at V _{CC} or GND; V _{CC} = 5.5 V			400	700		700	μA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4 V .
- This is the bus hold overdrive current required to force the input to the opposite logic state.

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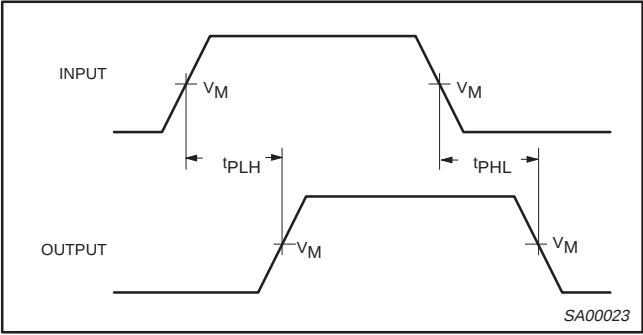
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

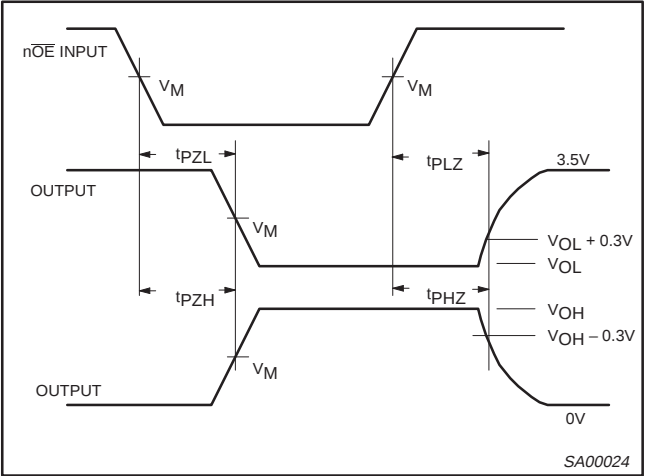
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25 °C V _{CC} = +5.0 V			T _{amb} = −40 °C to +85 °C V _{CC} = +5.0 V ±0.5 V		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.0 1.0	2.0 2.3	3.2 3.5	1.0 1.0	3.5 4.0	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.0 1.7	3.1 4.0	4.4 5.2	1.0 1.7	5.1 6.1	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.7 1.5	3.5 3.2	4.9 4.4	1.7 1.5	5.4 5.0	ns

AC WAVEFORMS

$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



Waveform 1. Input to Output Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

