

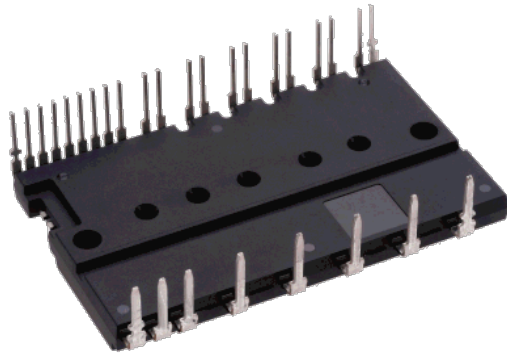
< Dual-In-Line Package Intelligent Power Module >

# PSS20S71F6

TRANSFER MOLDING TYPE

INSULATED TYPE

## OUTLINE



## MAIN FUNCTION AND RATINGS

- 3 phase DC/AC inverter
- 600V / 20A (CSTBT)
- N-side IGBT open emitter
- Built-in bootstrap diodes with current limiting resistor

## APPLICATION

- AC 100~240Vrms(DC voltage:400V or below) class low power motor control

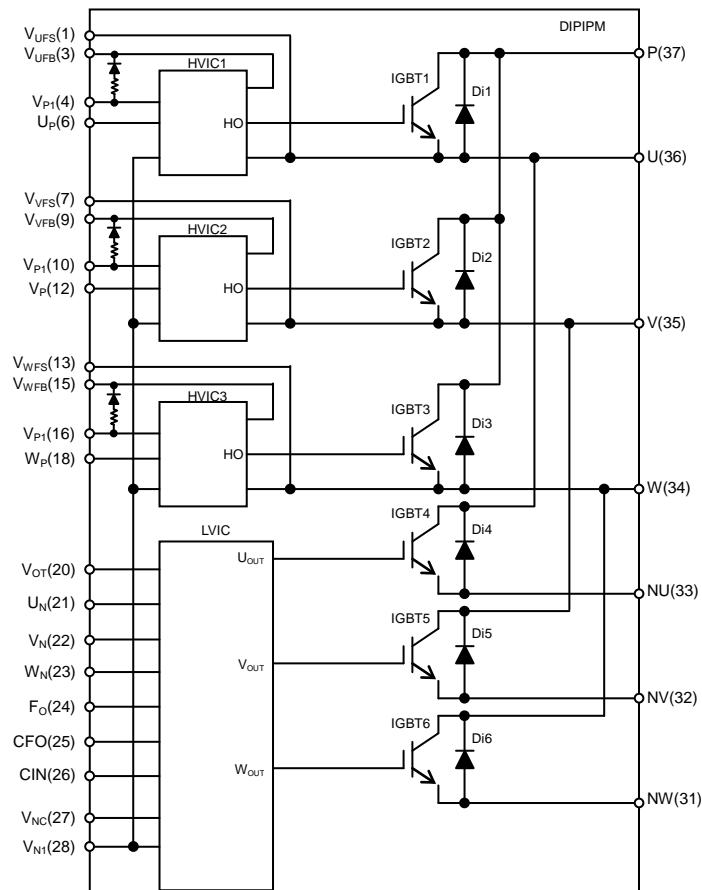
## TYPE NAME

PSS20S71F6	With temperature output function
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## INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC),
- Fault signaling : Corresponding to SC fault (N-side IGBT), UV fault (N-side supply)
- Temperature output : Outputting LVIC temperature by analog signal
- Input interface : 3, 5V line, Schmitt trigger receiver circuit (High Active)
- UL Recognized : UL1557 File E80276

## INTERNAL CIRCUIT



**MAXIMUM RATINGS** ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)**INVERTER PART**

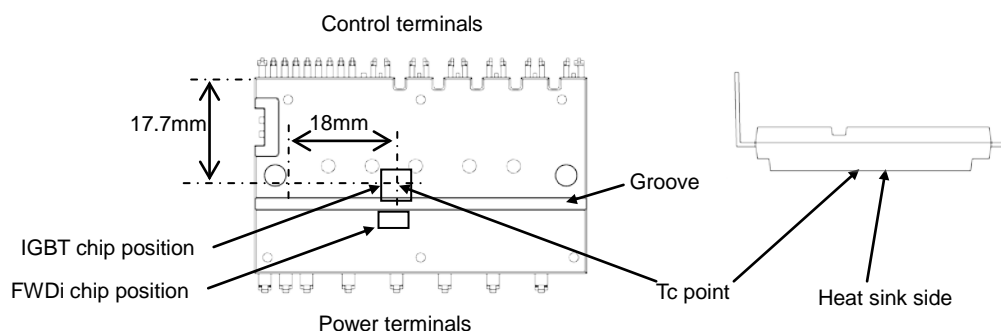
Symbol	Parameter	Condition	Ratings	Unit
$V_{CC}$	Supply voltage	Applied between P-NU, NV, NW	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU, NV, NW	500	V
$V_{CES}$	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	$T_C = 25^\circ\text{C}$	20	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_C = 25^\circ\text{C}$ , less than 1ms	40	A
$P_C$	Collector dissipation	$T_C = 25^\circ\text{C}$ , per 1 chip	76.9	W
$T_j$	Junction temperature		-20~+150	$^\circ\text{C}$

**CONTROL (PROTECTION) PART**

Symbol	Parameter	Condition	Ratings	Unit
$V_D$	Control supply voltage	Applied between $V_{P1}-V_{NC}$ , $V_{N1}-V_{NC}$	20	V
$V_{DB}$	Control supply voltage	Applied between $V_{UFB}-V_{UFS}$ , $V_{VFB}-V_{VFS}$ , $V_{WFB}-V_{WFS}$	20	V
$V_{IN}$	Input voltage	Applied between $U_P$ , $V_P$ , $W_P$ , $U_N$ , $V_N$ , $W_N-V_{NC}$	-0.5~ $V_D+0.5$	V
$V_{FO}$	Fault output supply voltage	Applied between $F_O-V_{NC}$	-0.5~ $V_D+0.5$	V
$I_{FO}$	Fault output current	Sink current at $F_O$ terminal	1	mA
$V_{SC}$	Current sensing input voltage	Applied between $CIN-V_{NC}$	-0.5~ $V_D+0.5$	V

**TOTAL SYSTEM**

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(Prot)}$	Self protection supply voltage limit (Short circuit protection capability)	$V_D = 13.5\sim 16.5\text{V}$ , Inverter Part $T_j = 125^\circ\text{C}$ , non-repetitive, less than 2 $\mu\text{s}$	400	V
$T_C$	Module case operation temperature	Measurement point of $T_C$ is provided in Fig.1	-20~+100	$^\circ\text{C}$
$T_{stg}$	Storage temperature		-40~+125	$^\circ\text{C}$
$V_{iso}$	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	$V_{rms}$

Fig. 1:  $T_C$  MEASUREMENT POINT**THERMAL RESISTANCE**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 1)	Inverter IGBT part (per 1/6 module)	-	-	1.3	K/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	-	-	3.0	K/W

Note 1: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100 $\mu\text{m}$ ~+200 $\mu\text{m}$  on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink  $R_{th(c-f)}$  is determined by the thickness and the thermal conductivity of the applied grease. For reference,  $R_{th(c-f)}$  is about 0.3K/W (per 1/6 module, grease thickness: 20 $\mu\text{m}$ , thermal conductivity: 1.0W/m $\cdot$ k).

**ELECTRICAL CHARACTERISTICS** ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D=V_{DB} = 15V, V_{IN}= 5V$	$I_C= 20A, T_j= 25^{\circ}C$	-	1.40	1.90	V
			$I_C= 20A, T_j= 125^{\circ}C$	-	1.50	2.00	
$V_{EC}$	FWDi forward voltage	$V_{IN}= 0V, -I_C= 20A$		-	1.50	2.00	V
$t_{on}$	Switching times	$V_{CC}= 300V, V_D= V_{DB}= 15V$ $I_C= 20A, T_j= 125^{\circ}C, V_{IN}= 0\leftrightarrow 5V$ Inductive Load (upper-lower arm)		0.95	1.55	2.15	$\mu s$
$t_{C(on)}$				-	0.50	0.80	$\mu s$
$t_{off}$				-	1.75	2.35	$\mu s$
$t_{C(off)}$				-	0.40	0.60	$\mu s$
$t_{rr}$				-	0.30	-	$\mu s$
$I_{CES}$	Collector-emitter cut-off current	$V_{CE}=V_{CES}$	$T_j= 25^{\circ}C$	-	-	1	mA
			$T_j= 125^{\circ}C$	-	-	10	

**CONTROL (PROTECTION) PART**

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I <sub>D</sub>	Circuit current	Total of V <sub>P1</sub> -V <sub>NC</sub> , V <sub>N1</sub> -V <sub>NC</sub>	V <sub>D</sub> =15V, V <sub>IN</sub> =0V	-	-	6.00	mA
			V <sub>D</sub> =15V, V <sub>IN</sub> =5V	-	-	6.00	
I <sub>DB</sub>		Each part of V <sub>UFB</sub> - V <sub>UFS</sub> , V <sub>VFB</sub> - V <sub>VFS</sub> , V <sub>WFB</sub> - V <sub>WFS</sub>	V <sub>D</sub> =V <sub>DB</sub> =15V, V <sub>IN</sub> =0V	-	-	0.55	
			V <sub>D</sub> =V <sub>DB</sub> =15V, V <sub>IN</sub> =5V	-	-	0.55	
V <sub>SC(ref)</sub>	Short circuit trip level	V <sub>D</sub> = 15V (Note 2)		0.45	0.48	0.51	V
UV <sub>DBt</sub>	P-side Control supply under-voltage protection(UV)	T <sub>j</sub> ≤125°C	Trip level	10.0	-	12.0	V
UV <sub>DBr</sub>			Reset level	10.5	-	12.5	V
UV <sub>Dt</sub>	N-side Control supply under-voltage protection(UV)		Trip level	10.3	-	12.5	V
UV <sub>Dr</sub>			Reset level	10.8	-	13.0	V
V <sub>OT</sub>	Temperature Output	Pull down R=5kΩ (Note 3)	LVIC Temperature=90°C	2.51	2.64	2.76	V
V <sub>FOH</sub>	Fault output voltage	V <sub>SC</sub> = 0V, F <sub>O</sub> terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V <sub>FOL</sub>		V <sub>SC</sub> = 1V, I <sub>FO</sub> = 1mA		-	-	0.95	V
t <sub>FO</sub>	Fault output pulse width	C <sub>FO</sub> =22nF (Note 4)		1.6	2.4	-	ms
I <sub>IN</sub>	Input current	V <sub>IN</sub> = 5V		0.70	1.00	1.50	mA
V <sub>th(on)</sub>	ON threshold voltage	Applied between U <sub>P</sub> , V <sub>P</sub> , W <sub>P</sub> , U <sub>N</sub> , V <sub>N</sub> , W <sub>N</sub> -V <sub>NC</sub>		-	2.10	2.60	V
V <sub>th(off)</sub>	OFF threshold voltage			0.80	1.30	-	
V <sub>th(hys)</sub>	ON/OFF threshold hysteresis voltage			0.35	0.80	-	
V <sub>F</sub>	Bootstrap Di forward voltage	I <sub>F</sub> =10mA including voltage drop by limiting resistor (Note 5)		0.5	0.9	1.3	V
R	Built-in limiting resistance	Included in bootstrap Di		16	20	24	Ω

Note 2 : SC protection works only for N-side IGBT. Please select the external shunt resistance such that the SC trip-level is less than 2.0 times of the current rating.

3 : DIPIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM. Temperature of LVIC vs. VOT output characteristics is described in Fig. 3.

4 : Fault signal  $F_O$  outputs when SC or UV protection works.  $F_O$  pulse width is different for each protection modes. At SC failure,  $F_O$  pulse width is a fixed width which is specified by the capacitor connected to  $C_{FO}$  terminal. ( $C_{FO}=9.1 \times 10^{-6} \times t_{FO} [F]$ ), but at UV failure,  $F_O$  outputs continuously until recovering from UV state. (But minimum  $F_O$  pulse width is the specified time by  $C_{FO}$ .)

5 : The characteristics of bootstrap Di is described in Fig.2.

Fig. 2 Characteristics of bootstrap Di  $V_F$ - $I_F$  curve (@ $T_a=25^\circ\text{C}$ ) including voltage drop by limiting resistor (Right chart is enlarged chart.)

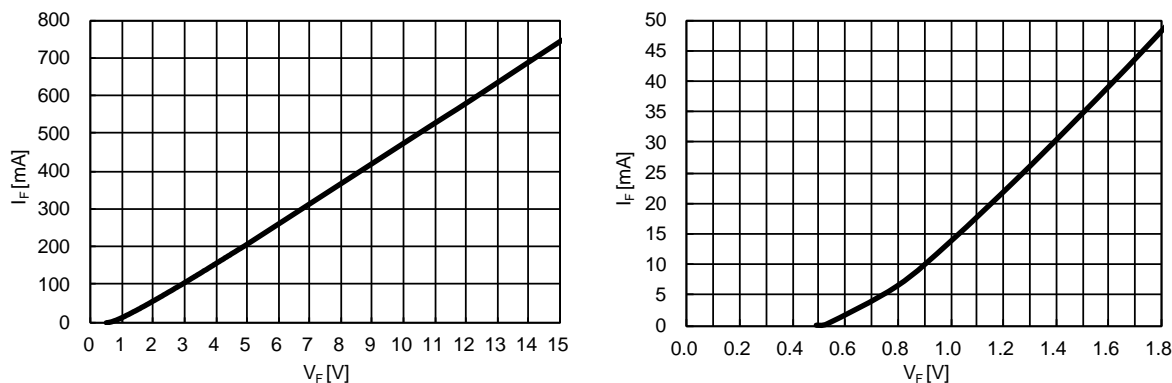


Fig. 3 Temperature of LVIC vs.  $V_{OT}$  output characteristics

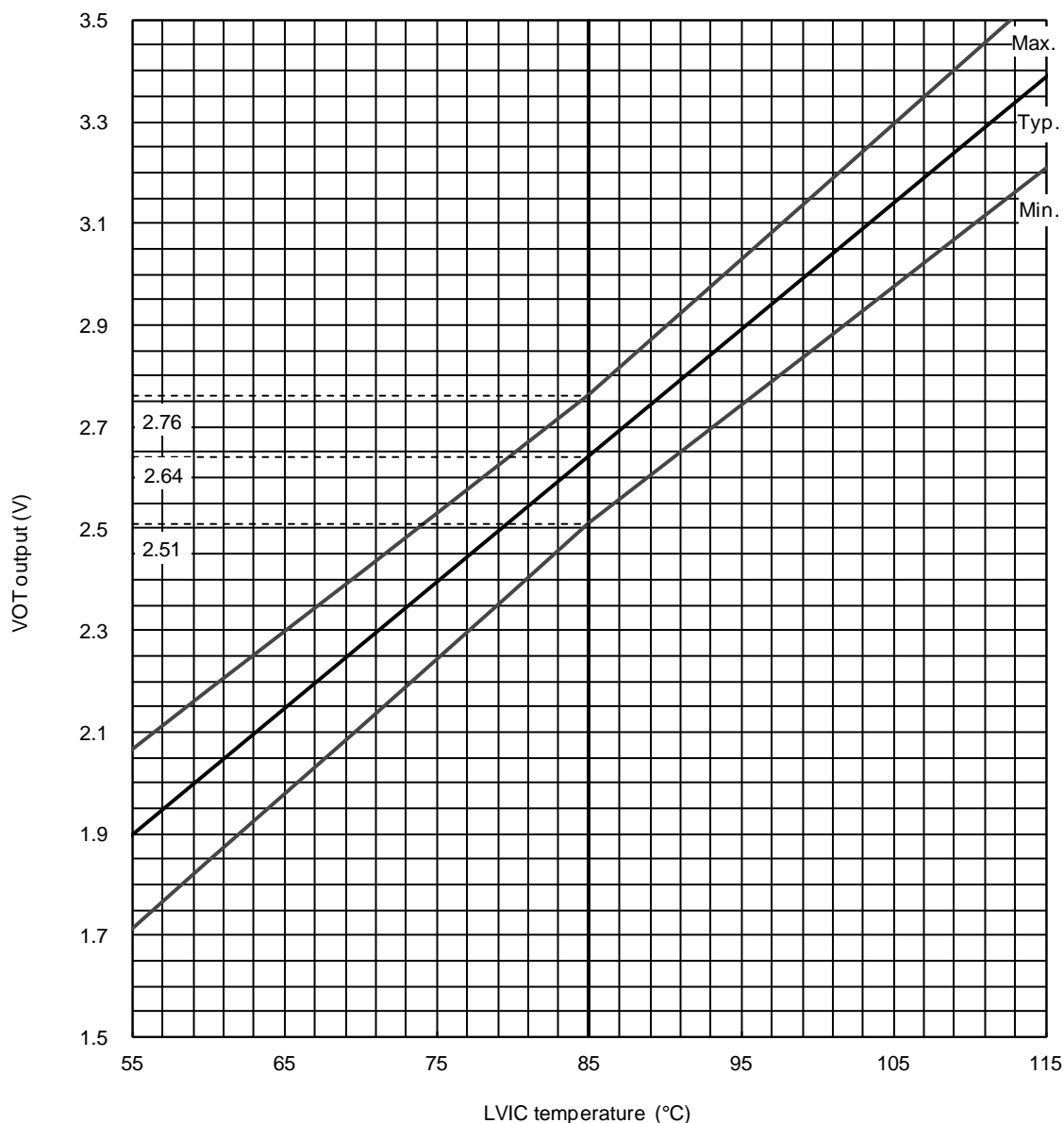
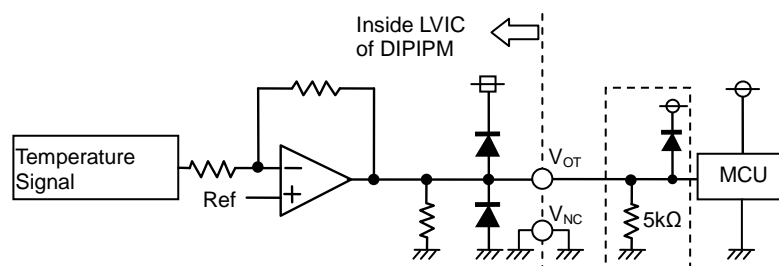


Fig. 4  $V_{OT}$  output circuit



- (1) It is recommended to insert 5kΩ (5.1kΩ is recommended) pull down resistor for getting linear output characteristics at low temperature below room temperature. When the pull down resistor is inserted between  $V_{OT}$  and  $V_{NC}$ (control GND), the extra circuit current, which is calculated approximately by  $V_{OT}$  output voltage divided by pull down resistance, flows as LVIC circuit current continuously. In the case of using  $V_{OT}$  for detecting high temperature over room temperature only, it is unnecessary to insert the pull down resistor.
- (2) In the case of using  $V_{OT}$  with low voltage controller like 3.3V MCU,  $V_{OT}$  output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and  $V_{OT}$  output for preventing over voltage destruction.
- (3) In the case of not using  $V_{OT}$ , leave  $V_{OT}$  output NC (No Connection).

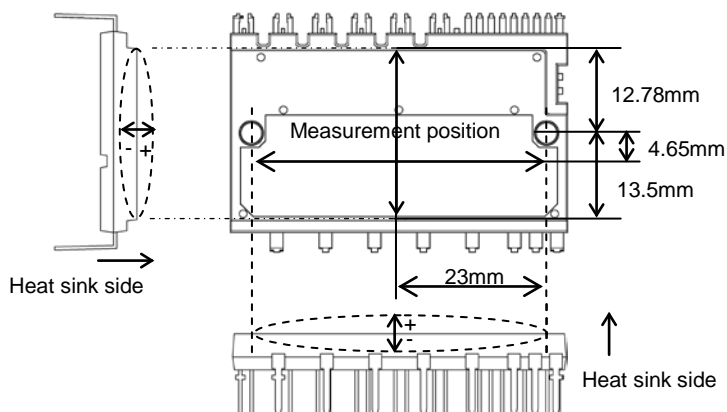
Refer the application note for this product about the usage of  $V_{OT}$ .

**MECHANICAL CHARACTERISTICS AND RATINGS**

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 6)	Recommended 0.78N·m	0.59	0.78	0.98	N·m
Terminal pulling strength	Load 9.8N	EIAJ-ED-4701	10	-	-	s
Terminal bending strength	Load 4.9N, 90deg. bend	EIAJ-ED-4701	2	-	-	times
Weight			-	21	-	g
Heat-sink flatness		(Note 7)	-50	-	100	μm

Note 6: Plain washers (ISO 7089~7094) are recommended.

Note 7: Measurement point of heat sink flatness

**RECOMMENDED OPERATION CONDITIONS**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CC}$	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V
$V_D$	Control supply voltage	Applied between $V_{P1}$ - $V_{NC}$ , $V_{N1}$ - $V_{NC}$	13.5	15.0	16.5	V
$V_{DB}$	Control supply voltage	Applied between $V_{UEB}$ - $V_{UFS}$ , $V_{VFB}$ - $V_{VFS}$ , $V_{WFB}$ - $V_{WFS}$	13.0	15.0	18.5	V
$\Delta V_D$ , $\Delta V_{DB}$	Control supply variation		-1	-	+1	V/μs
$t_{dead}$	Arm shoot-through blocking time	For each input signal	1.5	-	-	μs
$f_{PWM}$	PWM input frequency	$T_C \leq 100^\circ\text{C}$ , $T_J \leq 125^\circ\text{C}$	-	-	20	kHz
$I_o$	Allowable r.m.s. current	$V_{CC} = 300\text{V}$ , $V_D = 15\text{V}$ , P.F = 0.8, Sinusoidal PWM $T_C \leq 100^\circ\text{C}$ , $T_J \leq 125^\circ\text{C}$ (Note8)	$f_{PWM} = 5\text{kHz}$		14.0	Arms
			$f_{PWM} = 15\text{kHz}$		13.0	
PWIN(on)		(Note 9)	0.7	-	-	μs
PWIN(off)	Minimum input pulse width	200V ≤ $V_{CC}$ ≤ 350V, 13.5V ≤ $V_D$ ≤ 16.5V, 13.0V ≤ $V_{DB}$ ≤ 18.5V, -20°C ≤ $T_C$ ≤ 100°C, N-line wiring inductance less than 10nH (Note 10)	Below rated current		1.4	
			Between rated current and 1.7 times of rated current		2.5	
			Between 1.7 times and 2.0 times of rated current		3.0	
$V_{NC}$	$V_{NC}$ variation	Between $V_{NC}$ -NU, NV, NW (including surge)	-5.0	-	+5.0	V
$T_J$	Junction temperature		-20	-	+125	°C

Note 8: Allowable r.m.s. current depends on the actual application conditions.

9: DIPIM might not make response if the input signal pulse width is less than PWIN(on)

10: IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off). Please refer below about delayed response.

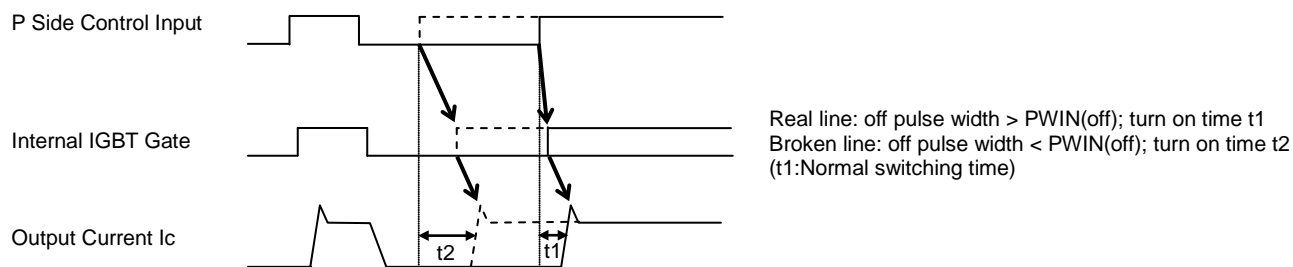
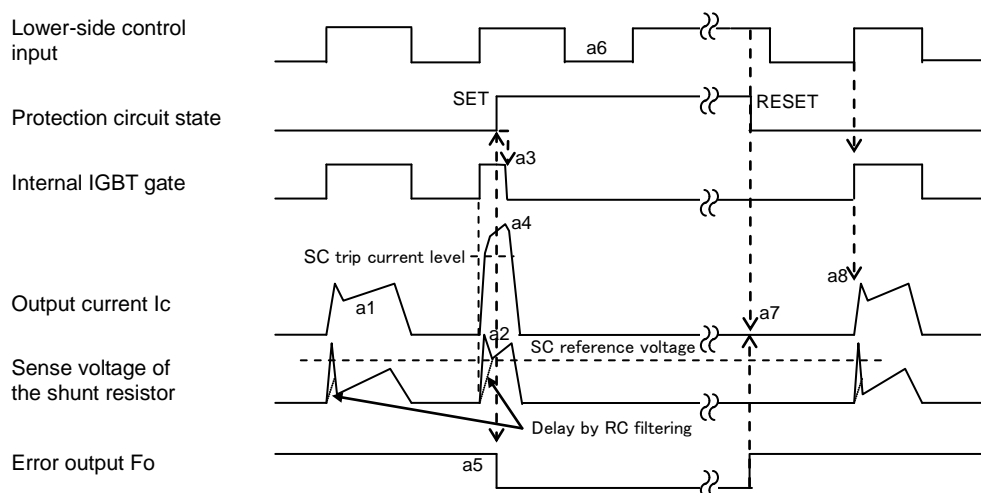
**Delayed Response against Shorter Input Off Signal than PWIN(off) (P-side only)**

Fig. 5 Timing Charts of The DIPIPM Protective Functions

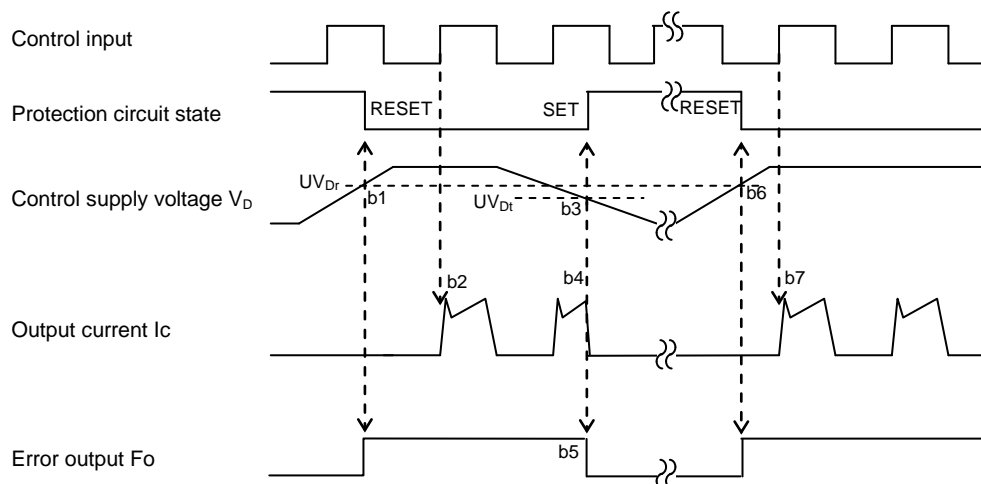
[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

- a1. Normal operation: IGBT ON and outputs current.
- a2. Short circuit current detection (SC trigger)  
(It is recommended to set RC time constant 1.5~2.0 $\mu$ s so that IGBT shut down within 2.0 $\mu$ s when SC.)
- a3. All N-side IGBT's gates are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5.  $F_o$  outputs. The pulse width of the  $F_o$  signal is set by the external capacitor  $C_{FO}$ .
- a6. Input = "L": IGBT OFF
- a7.  $F_o$  finishes output, but IGBTs don't turn on until inputting next ON signal (L $\rightarrow$ H).
- (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a8. Normal operation: IGBT ON and outputs current.



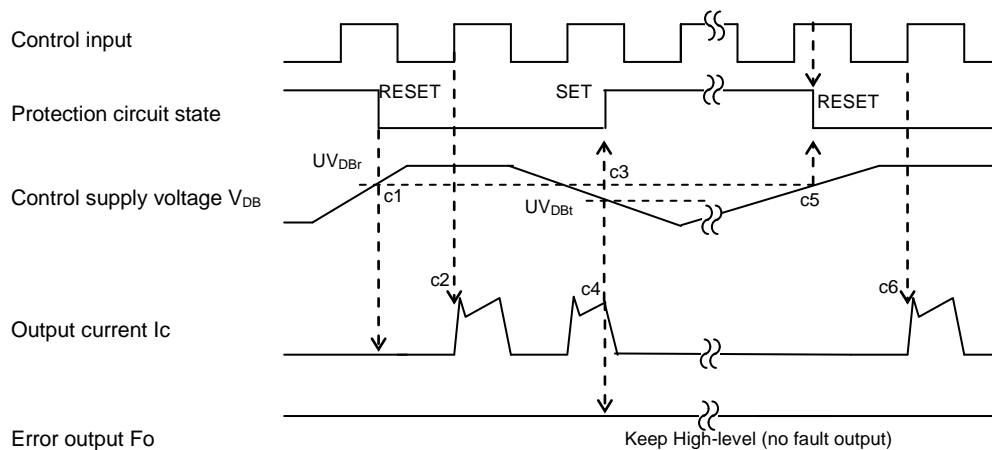
[B] Under-Voltage Protection (N-side,  $UV_D$ )

- b1. Control supply voltage  $V_D$  exceeds under voltage reset level ( $UV_{Dr}$ ), but IGBT turns ON by next ON signal (L $\rightarrow$ H).  
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- b2. Normal operation: IGBT ON and outputs current.
- b3.  $V_D$  level drops to under voltage trip level. ( $UV_{Dt}$ ).
- b4. All N-side IGBTs turn OFF in spite of control input condition.
- b5.  $F_o$  outputs for the period set by the capacitance  $C_{FO}$ , but output is extended during  $V_D$  keeps below  $UV_{Dr}$ .
- b6.  $V_D$  level reaches  $UV_{Dr}$ .
- b7. Normal operation: IGBT ON and outputs current.



[C] Under-Voltage Protection (P-side,  $UV_{DB}$ )

- c1. Control supply voltage  $V_{DB}$  rises. After the voltage reaches under voltage reset level  $UV_{DBr}$ , IGBT turns on by next ON signal (L→H).
- c2. Normal operation: IGBT ON and outputs current.
- c3.  $V_{DB}$  level drops to under voltage trip level ( $UV_{DBt}$ ).
- c4. IGBT of the correspond phase only turns OFF in spite of control input signal level, but there is no  $F_o$  signal output.
- c5.  $V_{DB}$  level reaches  $UV_{DBr}$ .
- c6. Normal operation: IGBT ON and outputs current.



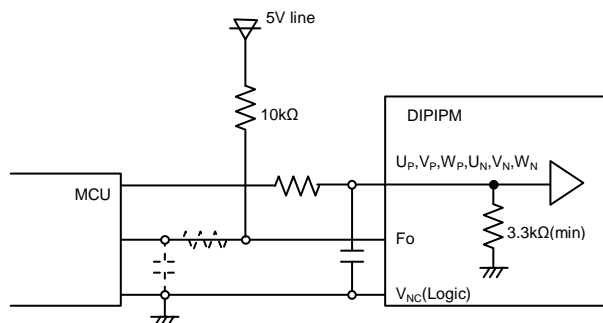
## TRANSFER MOLDING TYPE INSULATED TYPE

The schematic diagram illustrates a 3-phase motor driver circuit. It features an MCU (Microcontroller Unit) on the left, which interfaces with three HVIC (High Voltage Integrated Circuit) blocks and one LVIC (Low Voltage Integrated Circuit) block. The HVIC blocks are connected to the motor's three phases (U, V, W) via IGBTs (IGBT1, IGBT2, IGBT3) and diodes (Di1, Di2, Di3). The LVIC block is connected to the motor's neutral point (N) via IGBTs (IGBT4, IGBT5, IGBT6) and diodes (Di4, Di5, Di6). The motor (M) is connected to the output of the HVIC and LVIC blocks. The circuit includes various input and output pins, such as V<sub>UFB</sub>(3), V<sub>UFS</sub>(1), V<sub>P1</sub>(4), U<sub>P</sub>(6), V<sub>P</sub>(12), W<sub>P</sub>(18), V<sub>Or</sub>(20), U<sub>N</sub>(21), V<sub>N</sub>(22), W<sub>N</sub>(23), F<sub>O</sub>(24), C<sub>FO</sub>(25), V<sub>N1</sub>(28), and V<sub>NC</sub>(27). The circuit also includes a shunt resistor (R1) and a capacitor (C4) for current sensing and filtering. Annotations highlight potential issues: 'Long GND wiring here might generate noise to input signal and cause IGBT malfunction.' points to the ground connection of the MCU; 'Long wiring here might cause SC level fluctuation and malfunction.' points to the wiring between the LVIC and the motor; and 'Long wiring here might cause short circuit failure' points to the wiring between the motor and the power supply.

- 8



Fig. 7 MCU I/O Interface Circuit

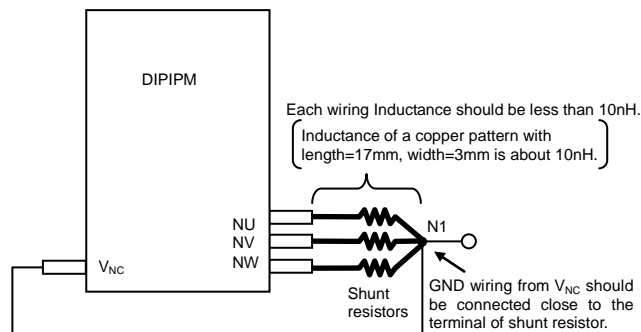
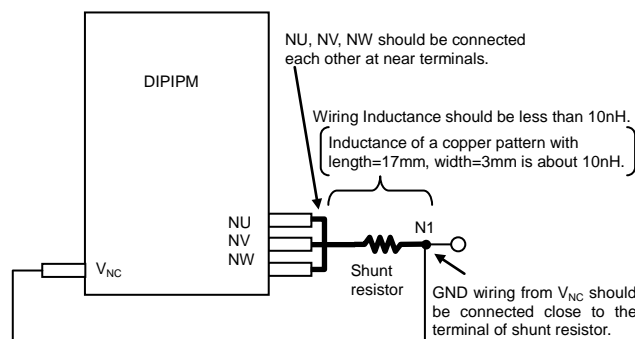


Note)

Design for input RC filter depends on PWM control scheme used in the application and wiring impedance of the printed circuit board. DIPIPM input signal interface integrates a minimum 3.3kΩ pull-down resistor. Therefore, when inserting RC filter, it is necessary to satisfy turn-on threshold voltage requirement.

Fo output is open drain type. It should be pulled up to control power supply (e.g. 5V, 15V) with a resistor that makes Fo sink current  $I_{F_O}$  1mA or less. In the case of pulled up to 5V supply, 10kΩ (5kΩ or more) is recommended.

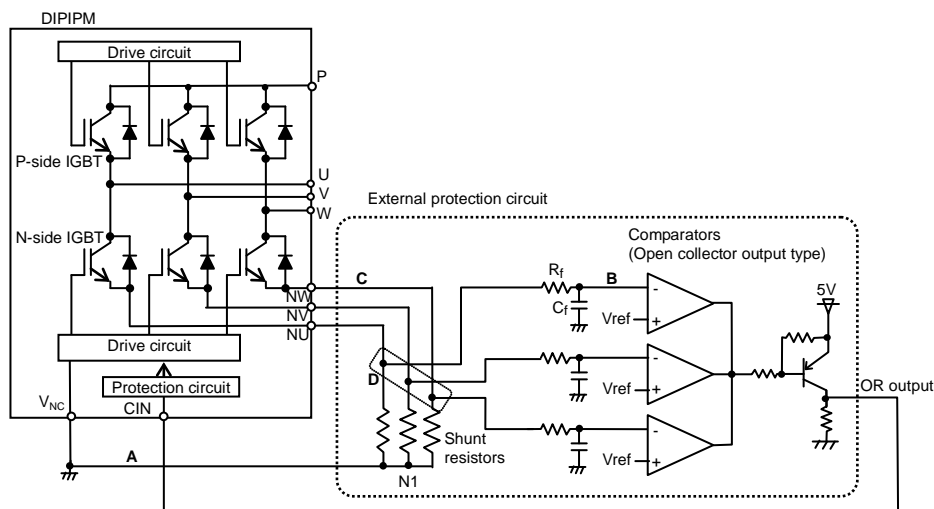
Fig. 8 Pattern Wiring Around the Shunt Resistor



Low inductance shunt resistor like surface mounted (SMD) type is recommended.

Fig. 9 Pattern Wiring Around the Shunt Resistor (for the case of open emitter)

When DIPIPM is operated with three shunt resistors, voltage of each shunt resistor cannot be input to CIN terminal directly. In that case, it is necessary to use the external protection circuit as below.



- (1) It is necessary to set the time constant  $R_f C_f$  of external comparator input so that IGBT stops within 2μs when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
- (2) It is recommended for the threshold voltage  $V_{ref}$  to set to the same rating of short circuit trip level ( $V_{sc(ref)}$ : typ. 0.48V).
- (3) Select the external shunt resistance so that SC trip-level is less than specified value ( $\approx 2.0$  times of rating current).
- (4) To avoid malfunction, the wiring A, B, C should be as short as possible.
- (5) The point D at which the wiring to comparator is divided should be close to the terminal of shunt resistor.
- (6) OR output high level when protection works should be over 0.51V ( $\approx$  maximum  $V_{sc(ref)}$  rating).
- (7) GND of Comparator, GND of  $V_{ref}$  circuit and  $C_f$  should be not connected to power GND but to control GND wiring.

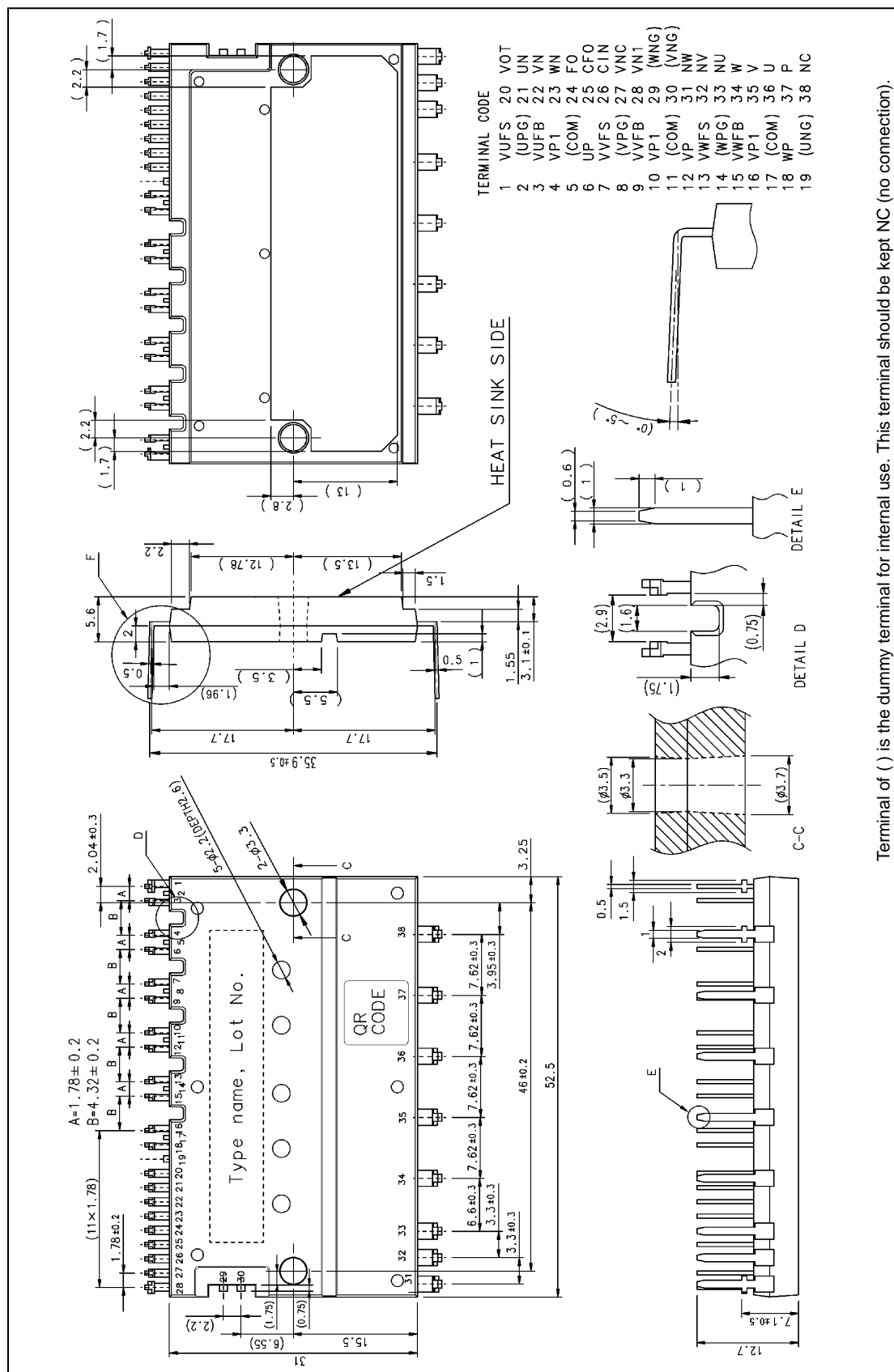
# PSS20S71F6

TRANSFER MOLDING TYPE

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Fig. 10 Package Outlines

Dimensions in mm



Terminal of ( ) is the dummy terminal for internal use. This terminal should be kept NC (no connection).

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# PSS20S71F6

TRANSFER MOLDING TYPE

INSULATED TYPE

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## Revision Record

Rev.	Date	Page	Revised contents
1	10/15/2013	-	New
2	12/25/2013	5	Revise misdescription (Condition of Terminal pulling strength and Terminal bending strength)
3	2/12/2014	1	[INTERNAL CIRCUIT] Revise misdescription of terminal name(VUFS,VUFB, VVFS, VVFB,VWFS,VWFB)
		10	Fig.10 Annotation is added.

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