

Serial-in Parallel-out LED Driver

24ch Constant Current LED Driver IC with 2-line Serial Interface

BD2808MUV-M
General Description

BD2808MUV-M is 24ch Constant current sink LED Driver with a high output voltage capability.
This device is optimized for driving RGB LEDs featuring a 6bit Current DAC for each color.
8bit PWM control is integrated for each channel.
Small VQFN48MCV070 package.

Key Specifications

■ Input Voltage Range:	3.0V to 5.5V
■ Output Voltage Range:	20V (Max)
■ DC Output Current (per ch):	50mA (Max)
■ Operating Temperature Range:	-40°C to +105°C

Package

VQFN48MCV070

 W (Typ) x D (Typ) x H (Max)
 7.00mm x 7.00mm x 1.00mm

Features

- AEC-Q100 Qualified (Note 1)
- 2-Line Serial Control + Enable Signal
- VQFN48 Package
- 24 channel constant current LED driver (max 50mA / channel)
- Independent PWM control for each channel
- 6 bit current DAC for RGB
- Protection features
- Equipped with PWM phase shift function to reduce EMI

(Note1: Grade 2)

Applications

- Instrument Cluster
- LED status indicators
- Instrument backlighting
- LED Interior illumination

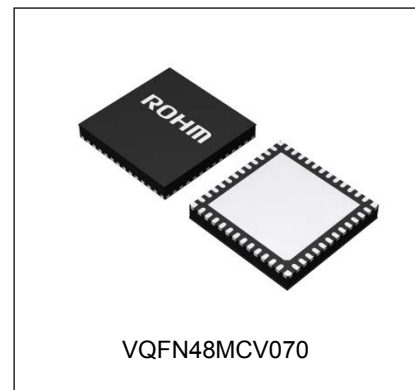
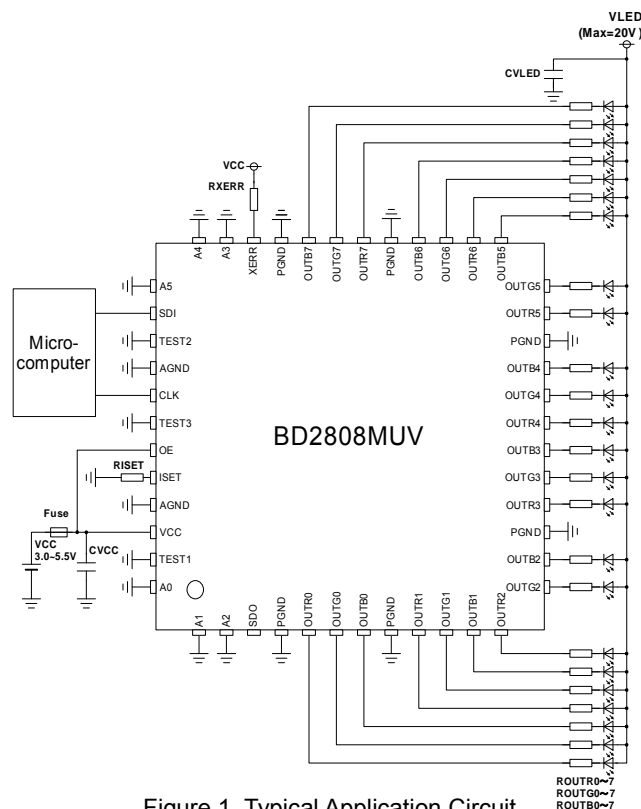

Typical Application Circuit


Figure 1. Typical Application Circuit

Product structure: Silicon monolithic integrated circuit. This product has no designed protection against radioactive rays.

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Pin Configuration

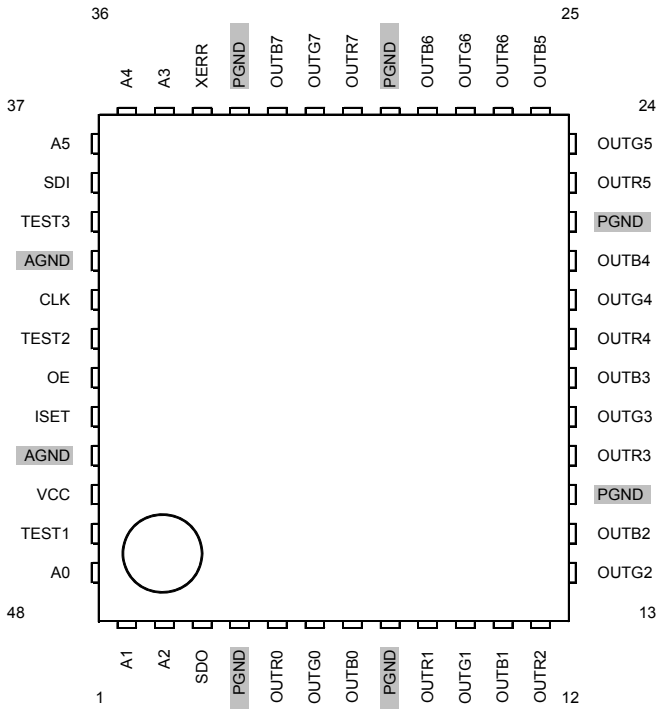


Figure 2. Pin Configuration

Pin Descriptions

Pin No.	Pin Name	Functions
1	A1	Device-address bit
2	A2	Device-address bit
3	SDO	Serial data output
4	PGND	Ground
5	OUTR0	R0 constant-current output
6	OUTG0	G0 constant-current output
7	OUTB0	B0 constant-current output
8	PGND	Ground
9	OUTR1	R1 constant-current output
10	OUTG1	G1 constant-current output
11	OUTB1	B1 constant-current output
12	OUTR2	R2 constant-current output
13	OUTG2	G2 constant-current output
14	OUTB2	B2 constant-current output
15	PGND	Ground
16	OUTR3	R3 constant-current output
17	OUTG3	G3 constant-current output
18	OUTB3	B3 constant-current output
19	OUTR4	R4 constant-current output
20	OUTG4	G4 constant-current output
21	OUTB4	B4 constant-current output
22	PGND	Ground
23	OUTR5	R5 constant-current output
24	OUTG5	G5 constant-current output
25	OUTB5	B5 constant-current output
26	OUTR6	R6 constant-current output
27	OUTG6	G6 constant-current output
28	OUTB6	B6 constant-current output
29	PGND	Ground
30	OUTR7	R7 constant-current output
31	OUTG7	G7 constant-current output
32	OUTB7	B7 constant-current output
33	PGND	Ground
34	XERR	Error output
35	A3	Device-address bit
36	A4	Device-address bit
37	A5	Device-address MSB
38	SDI	Serial data input
39	TEST3	Test terminal
40	AGND	Analog Ground
41	CLK	Serial data clock input
42	TEST2	Test terminal
43	OE	Output enable
44	ISET	Constant-current value setting
45	AGND	Analog Ground
46	VCC	Power supply
47	TEST1	Test terminal
48	A0	Device-address LSB

Block Diagram

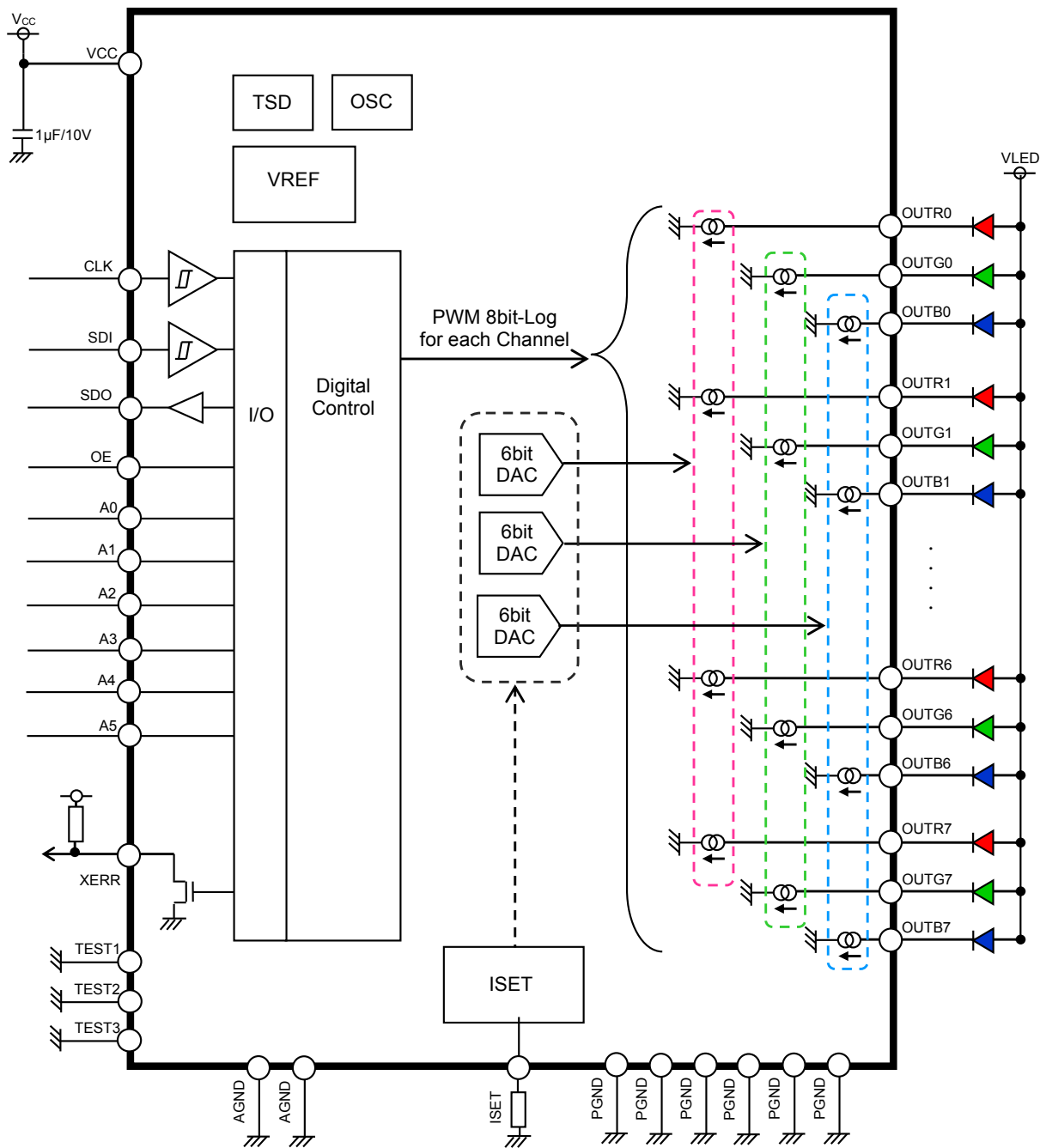


Figure 3. Block Diagram

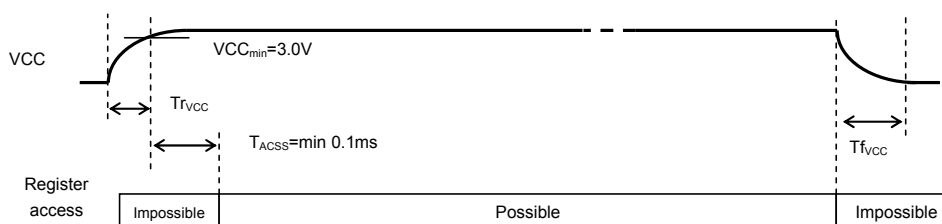
Description of Blocks

(1) Power Supply Start-up

The rise and fall time of a power supply can be from 10us to 1s.

Allow at least 0.1ms after V_{CC} exceeds $V_{UVLO\text{Rise}}$ UVLO before commencing communication.

Input pin voltages must not exceed V_{CC} or LED flicker may occur at start-up.



(2) LED Driver operation

Maximum LED current can be set by selecting the value of R_{ISET} .

The following formula gives the required value of R_{ISET} .

$$I_{LED_max}[mA] = 40 \times 64 / R_{ISET}[k\Omega] \quad (\text{Typ})$$

(3) Reset

Power on reset occurs when V_{CC} voltage falls below $V_{UVLO\text{Fall}}$.

Software reset is by command. If reset occurs, all registers are cleared (set to 0)

(4) Protection function (XERR output)

When thermal shutdown, channel open, or ISET terminal short to ground are detected, the XERR terminal is pulled LOW. All protection functions incorporate noise rejection. The XERR terminal output is low only during detection. (Latch and intentional delay time are not provided.) These signals are also written into a register. The flag returns to "0" only when the register is read.

The thermal shutdown operates at 175°C typically with 10°C of hysteresis, release therefore occurring at 165°C typically. All the channels of are turned OFF automatically when thermal shut down operates.

When the R_{ISET} is out of range $R_{ISET\text{SHT}}$, a short to ground function prevents large current from flowing into the LEDs. All channels of LED driver are turned OFF automatically.

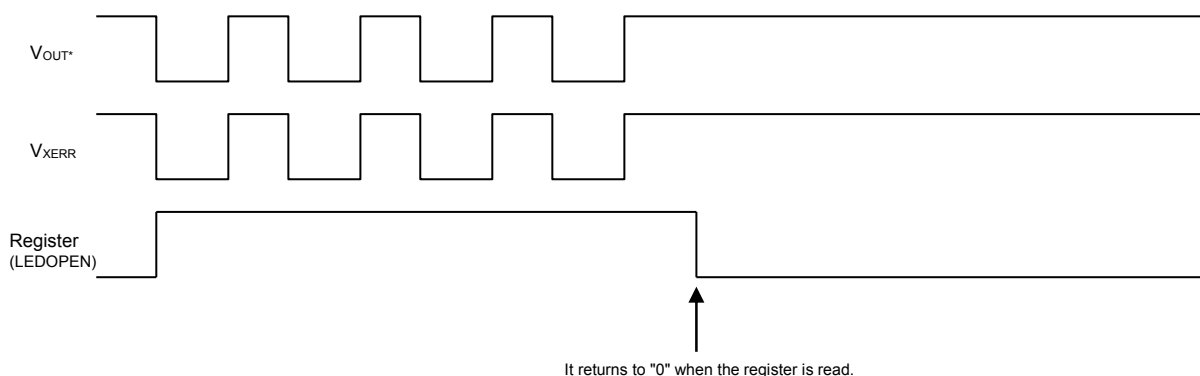
A Channel OPEN is detected when $V_{LED} < V_{LOD}$.

The individual channel is turned OFF automatically and V_{LED} becomes high impedance.

OPEN detection is not active if Brightness is set to 0.

The Error flag output pin (XERR pin) is in the same period with the OUT** pin and outputs a flag.

The flag stored in register retains the state once detected and is not changed until register is read.



Description of Blocks – Continued

(5) LED Current ON/OFF Function by External Pin (OE terminal)

All channels can be controlled by the external pin. If OE pin is HIGH, the LED drivers are active.
The internal PWM control circuit becomes asynchronous.

(6) Unused Pins

Set up the test terminals and the unused terminals as follows.

Pin Name	Connection	Reason
OUT**	Short to GND	To avoid uncertain/unfixed state. (Brightness setting of unused channel should be set to zero.)
SDO	Open	CMOS output terminal
XERR	Open or Short to GND	Open drain output terminal. When XERR is shorted to GND, noise is avoided.
OE	Short to VCC	Voltage clamp is necessary for CMOS input terminal. When OE is set to "LOW", LED current is OFF.
TESTx	Short to GND	To avoid test mode functionality.

(7) LED Current Waveform

To reduce EMI, the on-timing and off-timing of LED are shifted in 8 groups and simultaneous ON or OFF are avoided.
The rise t_r and t_f fall time of the output current is also limited to further reduce EMI noise.

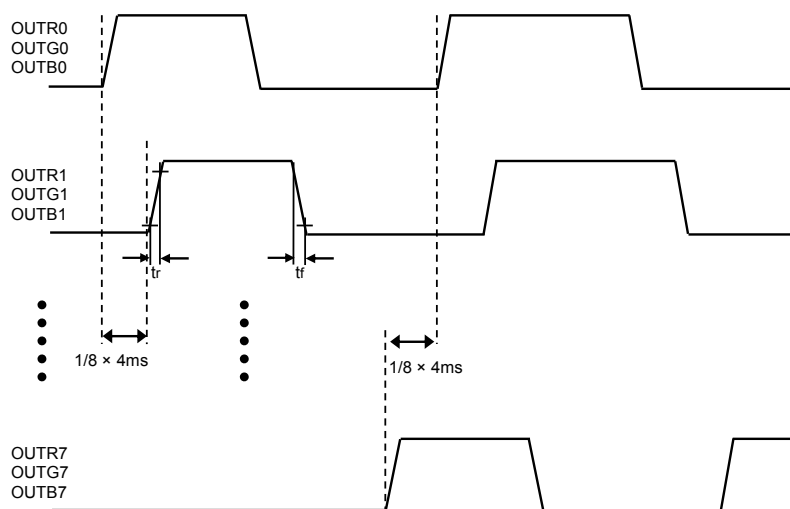


Figure 4. PWM phase-shift (8 groups)

(8) Diming function (PWM and DAC diming)

This IC has 2 diming functions which are PWM and DAC.
It is possible to set independent PWM control for each channel.
DAC diming is made 3 groups(R: Red, G: Green, B: Blue).
There are these detail at page 18, 19.

(9) Others(VREF and OSC)

There are VREF and OSC block for reference voltage and moving digital block.

(10) Test Processing

Test 1-3 are pins that are used for testing.

These pins are not used in normal operations, therefore connect it to ground.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	-0.3 to +7 (Note 1)	V
Output Voltage 1 (Pin No: Pin No: 5-7, 9-14, 16-21, 23-28, 30-32)	V _{LEDmax}	-0.3 to +20 (Note 1)	V
Output Voltage 2 (Pin No: 34)	V _{XERR}	-0.3 to V _{CC}	V
Input Voltage (Pin No: 1-3, 35-38, 41, 43-44, 48)	V _{IN}	-0.3 to V _{CC}	V
Power Dissipation1	Pd1	4.09 (Note 2)	W
Power Dissipation2	Pd2	5.20 (Note 3)	W
Operating Temperature Range	Topr	-40 to +105	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	150	°C
Drive Current (DC)	I _{omaxD}	50	mA

(Note 1) Pd should not be exceeded.

(Note 2) Pd1 is decreased by 32.7mW/°C for temperatures above Ta=25°C, mounted on 114.3mm x76.2mm x1.6mm Glass-epoxy PCB.

(Note 3) Pd2 is decreased by 41.6mW/°C for temperatures above Ta=25°C, mounted on 114.3mm x76.2mm x1.6mm Glass-epoxy PCB.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-40°C to 105°C)

Item	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V _{CC}	3.0	3.3	5.5	V
LED Maximum Output Current	I _{MAX}	-	-	50	mA

Application Conditions (External Constant Range)

Parameters	Symbols	Min	Max	Unit
VCC Capacitor	C _{VCC}	1.0	-	μF
VLED Capacitor	C _{VLED}	10	-	μF
ISER Resistor	R _{ISER}	50	200	kΩ
XERR Resistor	R _{XERR}	10	100	kΩ

Electrical Characteristics(Unless specified, Ta=-40 to 105°C V_{CC}=3.0 to 5.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
【Circuit Current】						
Standby VCC Circuit Current	I _{STB}	-	0.4	20	μA	RESET state (all registers have default values) LED terminal leak current is excluded
VCC Circuit Current	I _{VCC}		2.7	5.0	mA	All Ch=ON, PWM=100% I _{LED} =17.9mA setting, ISET=56kΩ (Note1)
【LED driver】						
LED Current Step	I _{LEDSTP}	64			step	Current DAC
LED Maximum Setup Current	I _{MAX}	-	50		mA	ISET=50kΩ (Note2)
LED Current Accuracy	I _{LED}	-5	0	+5	%	Terminal voltage=1V, Current accuracy of each OUT terminal I _{LED} =17.9mA setting, ISET=56kΩ (Note1)
LED Current Matching	I _{LEDMT}	-5	0	+5	%	An error with the average value of output current, Terminal voltage=1V I _{LED} =17.9mA setting, ISET=56kΩ (Note1)
LED Current Matching between RGB terminal	I _{LEDMT_RGB}	-5	0	+5	%	Terminal voltage=1V I _{LED} =17.9mA setting, ISET=56kΩ (Note1)
LED Current Matching between devices	I _{LEDMT_DEV}	-5	0	+5	%	Terminal voltage=1V I _{LED} =17.9mA setting, ISET=56kΩ (Note1)
Line Regulation	ΔI _{LIN}	-	-	2	%/V	V _{CC} from 3V to 5.5V
Load Regulation	ΔI _{RO}	-	-	1	%/V	V _{OUT} from 1V to 20V
Current Linearity at PWM Control	I _{LINPWM}	-	-	1.5	%	PWM Duty over 3%
LED OFF Leak Current	I _{LKL}	-	-	3	μA	Terminal voltage =20V
ISET Terminal Output Voltage	V _{ISET}	-	0.96	-	V	
ISET Resistance	R _{ISET}	50	-	200	kΩ	
【OSC】						
OSC Frequency	f _{OSC}	0.82	1.02	1.23	MHz	
PWM Frequency	f _{PWM}	200	250	300	Hz	
【UVLO】						
UVLO Detection Voltage	V _{UVLOFall}	2.0	2.4	-	V	When power supply voltage falls
UVLO Release Voltage	V _{UVLORise}	-	-	2.7	V	When power supply voltage rises
Hysteresis Voltage	V _{UVLOHYS}	50	-	-	mV	
【Protection Function】						
LED Terminal Open Detection Voltage	V _{LOD}	-	0.2	0.3	V	
ISET Short Detection Resistance	R _{ISETSHT}	5.0	20	40	kΩ	

(Note1) At DAC Setting R: ad03, data=18h, DAC Setting G: ad04, data=18h, DAC Setting B: ad05, data=18h

(R=56kΩ: I_{MAX}=40*64/56kΩ =45.7mA)(Note2) I_{MAX}=40*64/50kΩ =50mA

Electrical Characteristics - continued(Unless specified, Ta=-40 to 105°C V_{CC}=3.0 to 5.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
【CLK, SDI】						
Input L Level Voltage	V _{ILI1}	-0.3	-	0.25 × V _{CC}	V	
Input H Level Voltage	V _{IHI1}	0.75 × V _{CC}	-	V _{CC} +0.3	V	
Input Hysteresis Voltage	V _{HYSI1}	0.05 × V _{CC}	-	-	V	
Input Current	I _{II1}	-1	-	1	μA	Input voltage= 3.3V
【SDO】 (CMOS Output Pin)						
Output L Level Voltage	V _{OLSDO}	-	-	0.2	V	I _{OL} =1mA
Output H Level Voltage	V _{OHSDO}	V _{CC} -0.2	-	-	V	I _{OH} =1mA
【XERR】 (Open Drain Output Pin)						
Output L Level Voltage	V _{OLXE}	-	-	0.2	V	I _{OL} =1mA
【A0-5, OE】 (CMOS input pin)						
Input L Level Voltage	V _{ILI2}	-0.3	-	0.25 × V _{CC}	V	
Input H Level Voltage	V _{IHI2}	0.75 × V _{CC}	-	V _{CC} +0.3	V	
Input Hysteresis Voltage	V _{HYSI2}	0.05 × V _{CC}	-	-	V	
Input Current	I _{II2}	-1	-	1	μA	Input voltage= 3.3V

Typical Performance Curves

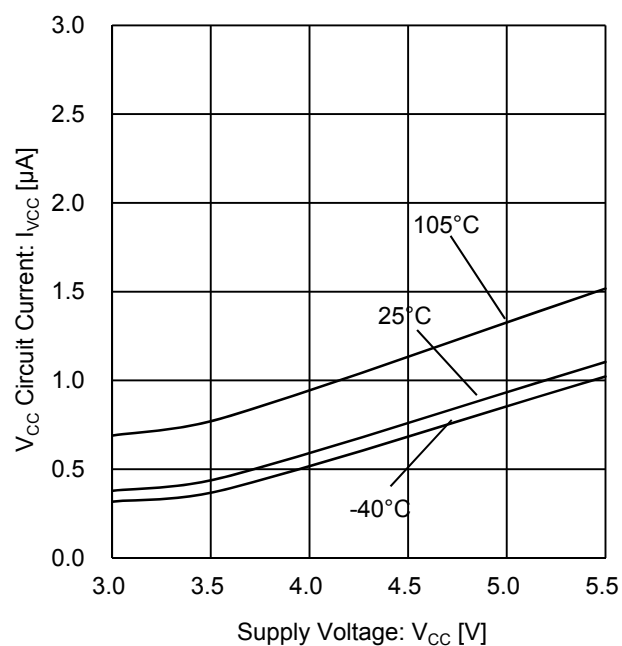


Figure 5. Standby Current
(V_{CC} characteristic)

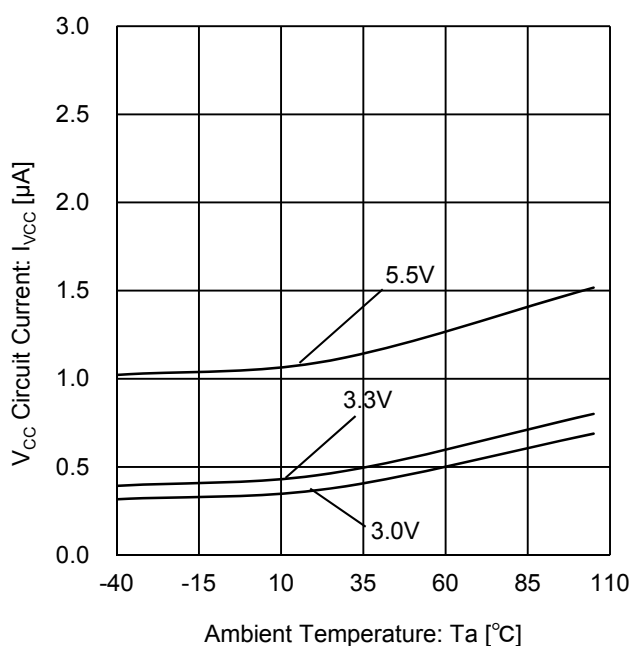


Figure 6. Standby Current
(Temperature characteristic)

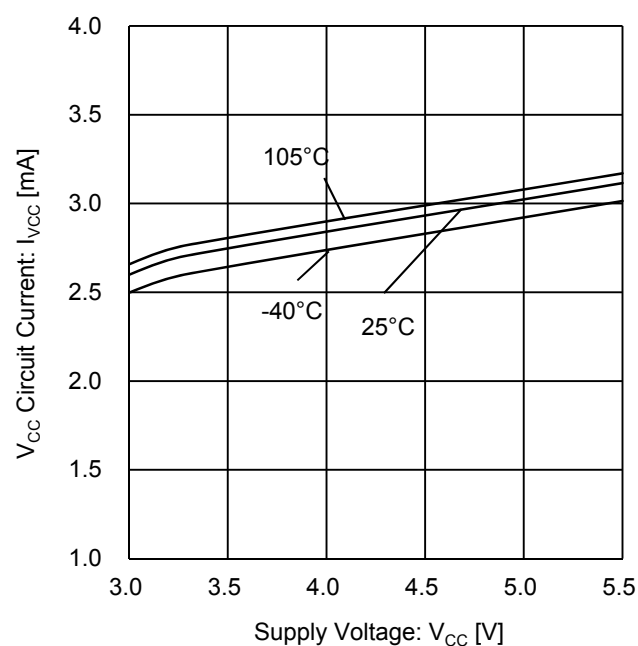


Figure 7. Circuit Current
(V_{CC} characteristic @ All OUTn=ON
PWM=100% ILED=17.9mA ISET=56kΩ)

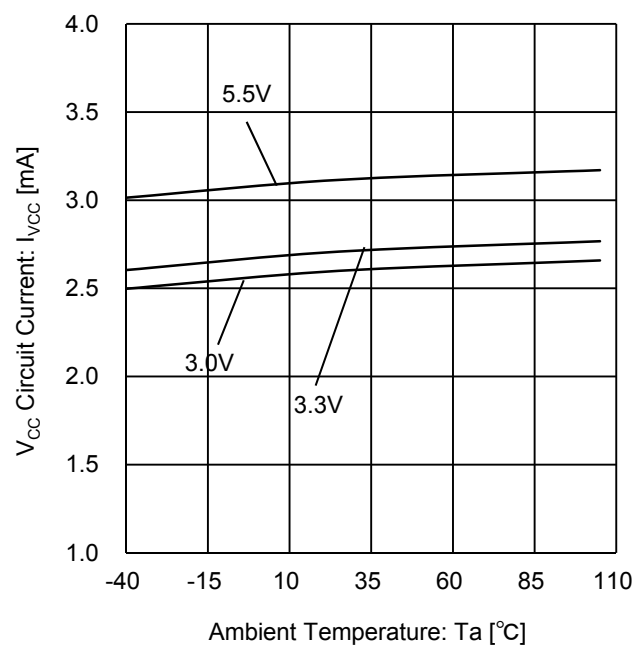


Figure 8. Circuit Current
(Temperature characteristic @ ALL OUTn=ON
PWM=100% ILED=17.9mA ISET=56kΩ)

Typical Performance Curves – continued

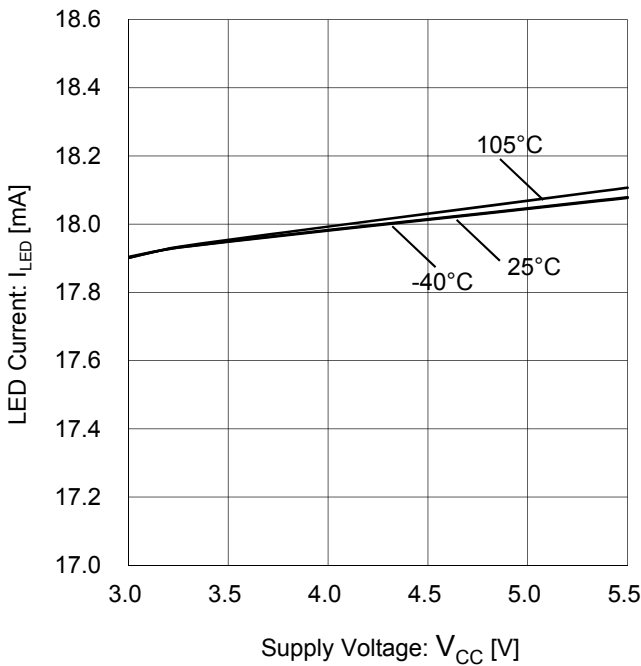


Figure 9. LED Current
(V_{CC} characteristic @ ISET=56kΩ)

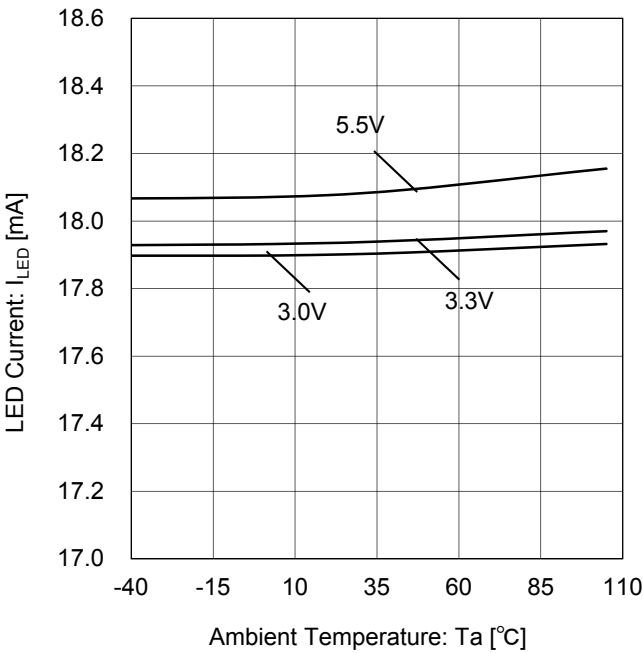


Figure 10. LED Current
(Temperature characteristic @ ISET=56kΩ)

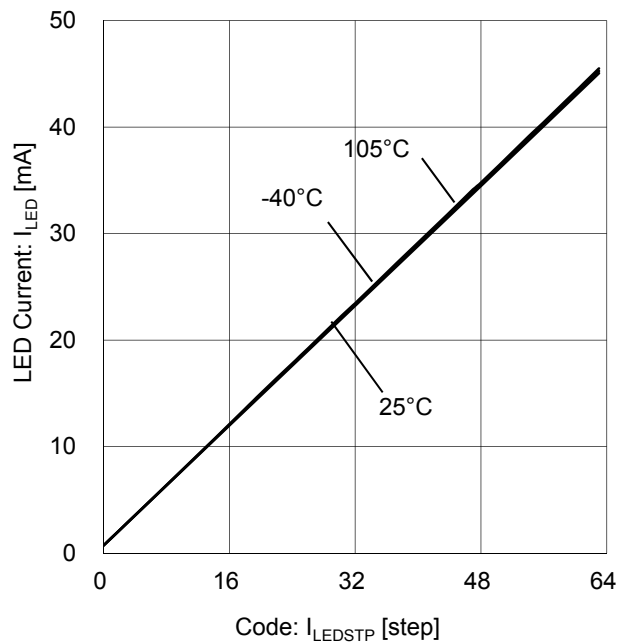


Figure 11. LED Current DAC Step
(V_{CC} =3.3V)

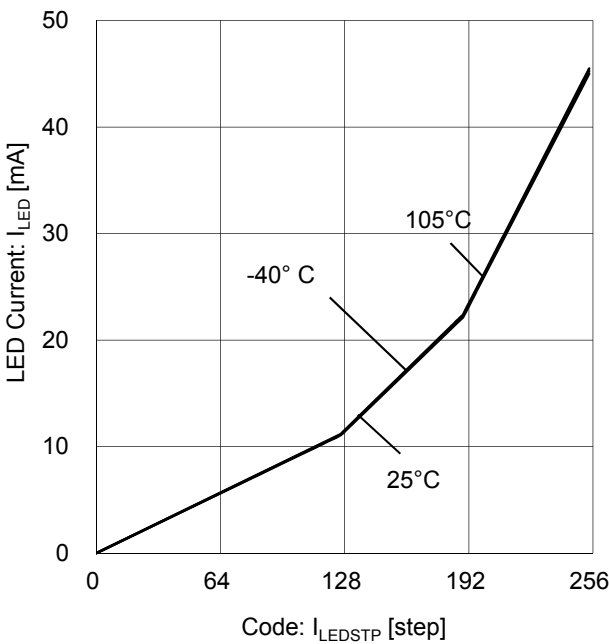


Figure 12. LED Current PWM Step
(V_{CC} =3.3V)

Typical Performance Curves – continued

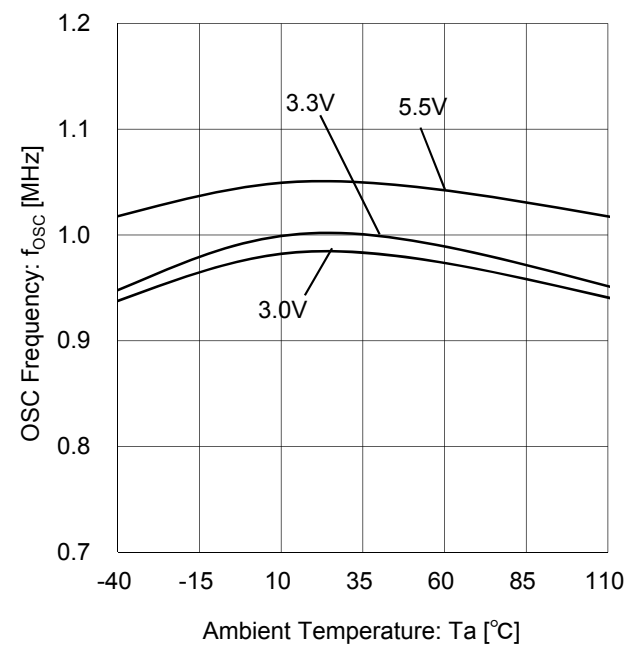


Figure 13. Oscillation Frequency
(Temperature characteristic)

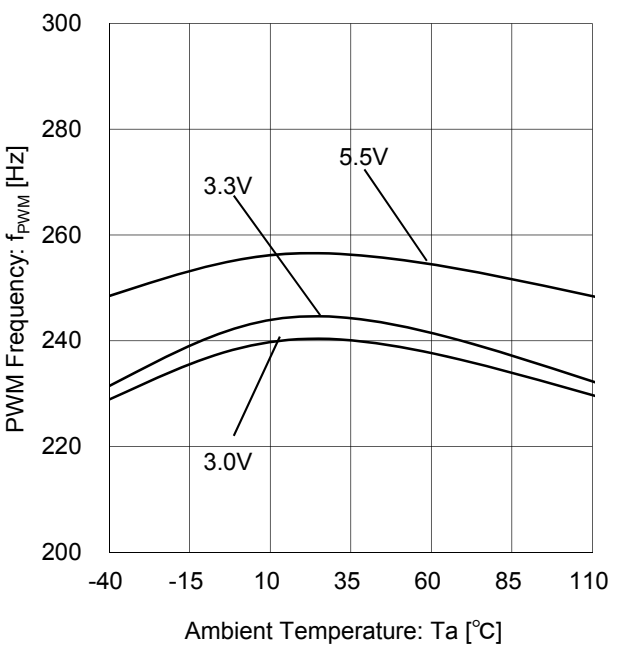


Figure 14. PWM Frequency
(Temperature characteristic)

Bus Format

- Device Address

	A7	A6	A5	A4	A3	A2	A1	A0
Device control mode	0	1	A5	A4	A3	A2	A1	A0
Bus control mode	0	0	*	*	*	*	*	*

Device control mode: Data is dependent on the A0 to A5 terminal settings.

Bus control mode: Data can be received without being dependent on A0 to A5 terminal settings.

- START Condition

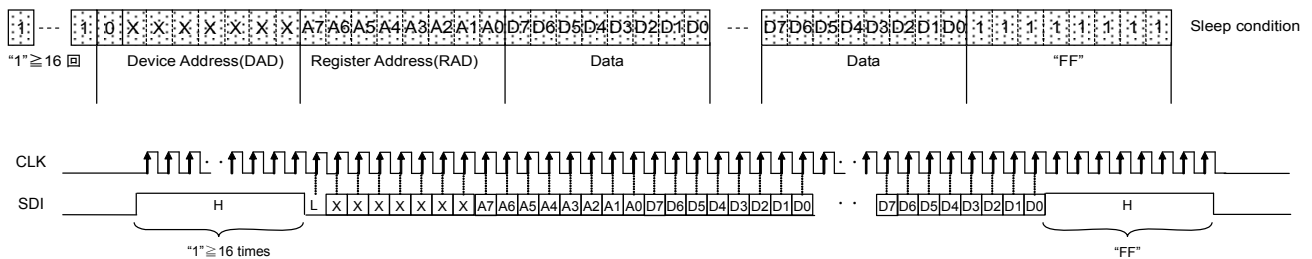
At STARTUP, the device enters WAIT mode when "1" is written 16 times or more, and a device address is recognized after writing "0".

- WRITE PROTOCOL

Data is shifted in the internal shift register on the rising edge CLK. MSB is entered first. The command format is: writing command "00" (2bit), device address (6bit), register address (8bit) and data (8bit).

Register address is incremented after the fourth byte automatically.

Device enters Sleep state when "1" is written eight times.

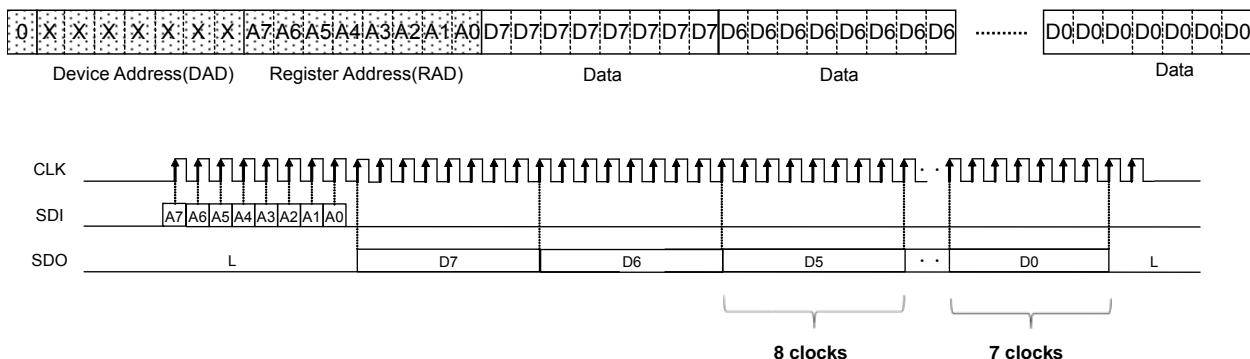


- READ PROTOCOL

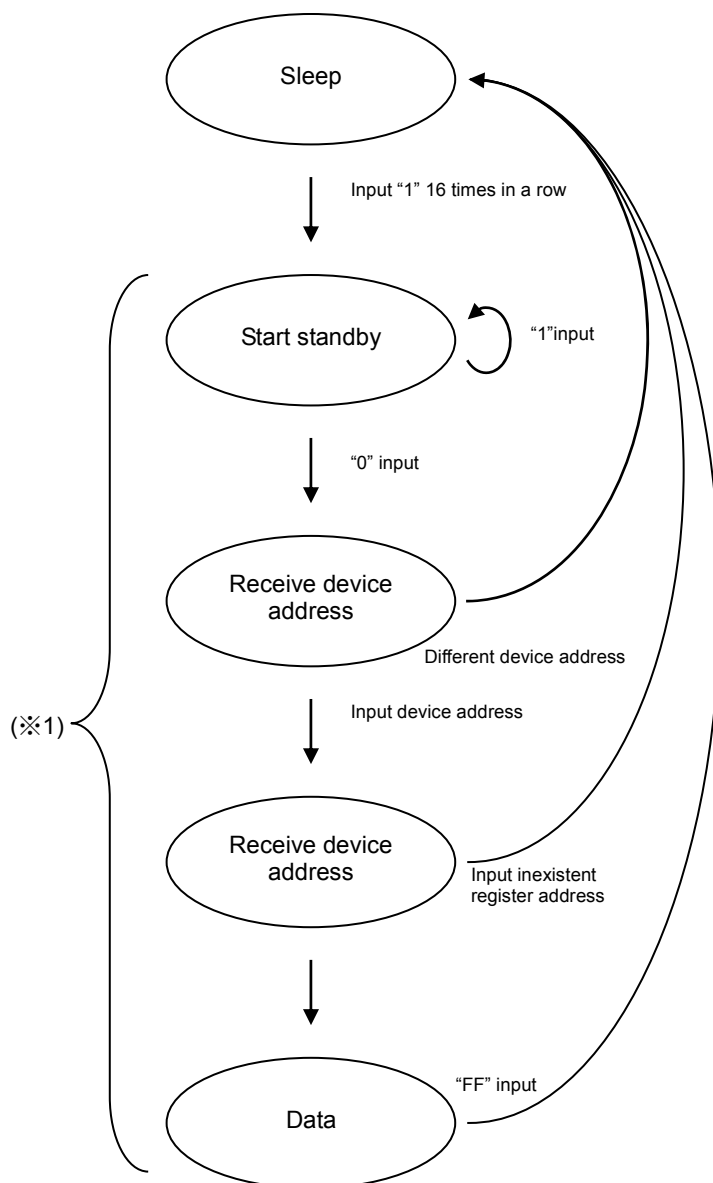
Read from the next byte after register address "WRITE data" for "READ data" and device address.

READ data is output on the SDO pin. For a READ command 8 clocks cycles are necessary. At the 8th clock of last bit of the specified register address, it becomes Sleep state, and the SDO pin becomes "L" output.

The last bit (D0) is outputted 7 clocks.

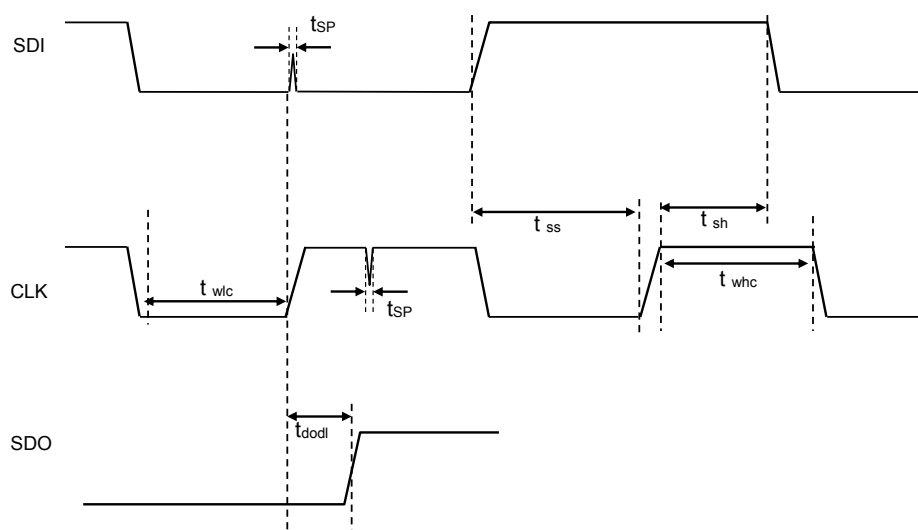


Protocol



※1) Condition becomes START standby in any condition, if "1" is detected more than 16 times. For example, Sleep condition starts if "1" is received 8 times while waiting for register address. Moreover, the condition becomes START standby after receiving "1" 8 times.

Timing Diagram



Timing Characteristics (Ta=-40 to 105 °C VCC=3.0 to 5.5V)

Item	Symbol	Standard value			Unit
		Min	Typ	Max	
【Interface】					
CLK cycle time	t _{scyc}	100	-	-	ns
CLK cycle “H” period	t _{whc}	50	-	-	ns
CLK cycle “L” period	t _{wlc}	50	-	-	ns
SDI setup time	t _{ss}	45	-	-	ns
SDI hold time	t _{sh}	45	-	-	ns
Pulse width of spike removed by input filter of CLK and SDI	t _{SP}	5	-	-	ns
SDO Output Delay (CL = 1,000pF)	T _{dodl}	-	-	500	ns

Register Map

Register Address	Write Or Read	Register data								Function
		D7	D6	D5	D4	D3	D2	D1	D0	
00h	R	-	-	A5	A4	A3	A2	A1	A0	Device address
01h	R	-	-	-	-	-	ISETSH	-	LEDOPN	Error condition detection
02h	W	-	-	-	-	SFTRST	ENMD	MD1	MD0	Mode setup
03h	W	-	-	DAR5	DAR4	DAR3	DAR2	DAR1	DAR0	DAC setting for OUTRx terminal
04h	W	-	-	DAG5	DAG4	DAG3	DAG2	DAG1	DAG0	DAC setting for OUTGx terminal
05h	W	-	-	DAB5	DAB4	DAB3	DAB2	DAB1	DAB0	DAC setting for OUTBx terminal
06h	W	BRR0(7)	BRR0(6)	BRR0(5)	BRR0(4)	BRR0(3)	BRR0(2)	BRR0(1)	BRR0(0)	OUTR0 PWM Setting
07h	W	BRG0(7)	BRG0(6)	BRG0(5)	BRG0(4)	BRG0(3)	BRG0(2)	BRG0(1)	BRG0(0)	OUTG0 PWM Setting
08h	W	BRB0(7)	BRB0(6)	BRB0(5)	BRB0(4)	BRB0(3)	BRB0(2)	BRB0(1)	BRB0(0)	OUTB0 PWM Setting
09h	W	BRR1(7)	BRR1(6)	BRR1(5)	BRR1(4)	BRR1(3)	BRR1(2)	BRR1(1)	BRR1(0)	OUTR1 PWM Setting
0Ah	W	BRG1(7)	BRG1(6)	BRG1(5)	BRG1(4)	BRG1(3)	BRG1(2)	BRG1(1)	BRG1(0)	OUTG1 PWM Setting
0Bh	W	BRB1(7)	BRB1(6)	BRB1(5)	BRB1(4)	BRB1(3)	BRB1(2)	BRB1(1)	BRB1(0)	OUTB1 PWM Setting
0Ch	W	BRR2(7)	BRR2(6)	BRR2(5)	BRR2(4)	BRR2(3)	BRR2(2)	BRR2(1)	BRR2(0)	OUTR2 PWM Setting
0Dh	W	BRG2(7)	BRG2(6)	BRG2(5)	BRG2(4)	BRG2(3)	BRG2(2)	BRG2(1)	BRG2(0)	OUTG2 PWM Setting
0Eh	W	BRB2(7)	BRB2(6)	BRB2(5)	BRB2(4)	BRB2(3)	BRB2(2)	BRB2(1)	BRB2(0)	OUTB2 PWM Setting
0Fh	W	BRR3(7)	BRR3(6)	BRR3(5)	BRR3(4)	BRR3(3)	BRR3(2)	BRR3(1)	BRR3(0)	OUTR3 PWM Setting
10h	W	BRG3(7)	BRG3(6)	BRG3(5)	BRG3(4)	BRG3(3)	BRG3(2)	BRG3(1)	BRG3(0)	OUTG3 PWM Setting
11h	W	BRB3(7)	BRB3(6)	BRB3(5)	BRB3(4)	BRB3(3)	BRB3(2)	BRB3(1)	BRB3(0)	OUTB3 PWM Setting
12h	W	BRR4(7)	BRR4(6)	BRR4(5)	BRR4(4)	BRR4(3)	BRR4(2)	BRR4(1)	BRR4(0)	OUTR4 PWM Setting
13h	W	BRG4(7)	BRG4(6)	BRG4(5)	BRG4(4)	BRG4(3)	BRG4(2)	BRG4(1)	BRG4(0)	OUTG4 PWM Setting
14h	W	BRB4(7)	BRB4(6)	BRB4(5)	BRB4(4)	BRB4(3)	BRB4(2)	BRB4(1)	BRB4(0)	OUTB4 PWM Setting
15h	W	BRR5(7)	BRR5(6)	BRR5(5)	BRR5(4)	BRR5(3)	BRR5(2)	BRR5(1)	BRR5(0)	OUTR5 PWM Setting
16h	W	BRG5(7)	BRG5(6)	BRG5(5)	BRG5(4)	BRG5(3)	BRG5(2)	BRG5(1)	BRG5(0)	OUTG5 PWM Setting
17h	W	BRB5(7)	BRB5(6)	BRB5(5)	BRB5(4)	BRB5(3)	BRB5(2)	BRB5(1)	BRB5(0)	OUTB5 PWM Setting
18h	W	BRR6(7)	BRR6(6)	BRR6(5)	BRR6(4)	BRR6(3)	BRR6(2)	BRR6(1)	BRR6(0)	OUTR6 PWM Setting
19h	W	BRG6(7)	BRG6(6)	BRG6(5)	BRG6(4)	BRG6(3)	BRG6(2)	BRG6(1)	BRG6(0)	OUTG6 PWM Setting
1Ah	W	BRB6(7)	BRB6(6)	BRB6(5)	BRB6(4)	BRB6(3)	BRB6(2)	BRB6(1)	BRB6(0)	OUTB6 PWM Setting
1Bh	W	BRR7(7)	BRR7(6)	BRR7(5)	BRR7(4)	BRR7(3)	BRR7(2)	BRR7(1)	BRR7(0)	OUTR7 PWM Setting
1Ch	W	BRG7(7)	BRG7(6)	BRG7(5)	BRG7(4)	BRG7(3)	BRG7(2)	BRG7(1)	BRG7(0)	OUTG7 PWM Setting
1Dh	W	BRB7(7)	BRB7(6)	BRB7(5)	BRB7(4)	BRB7(3)	BRB7(2)	BRB7(1)	BRB7(0)	OUTB7 PWM Setting
1Eh	W	-	-	-	-	-	-	-	EN	Brightness reflection (latch)

Assume that the input of “-” is “0”.

An undefined address may be assigned for test purposes. Access to undefined register is prohibited.

Register Description**Register address 00h < Read Device address>**

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	R	-	-	A5	A4	A3	A2	A1	A0
Initial value	(Arbitrary)	0	0	0	0	0	0	0	0

Bit [5: 0]: Device address (Read only)

Device address set by external terminal (A0 – A5) is returned.

Register address 01h <Read Error condition detection>

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01h	R	-	-	-	-	-	ISSETSH	-	LEDOPN
Initial Value	(Arbitrary)	0	0	0	0	0	0	0	0

Bit 2: ISSETSH ISET terminal short detection

“0”: Normal operation

“1”: ISET terminal GND short-circuit is detected

Bit 0: LEDOPN LED open detect

“0”: Normal operation

“1”: Detect LED open on any channel

(At LED is ON, detect LED terminal < 0.2V (Typ))

Register address 02h <Write Mode setup>

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h	W	-	-	-	-	SFTRST	ENMD	MD1	MD0
Initial value	00h	0	0	0	0	0	0	0	0

Bit 3: SFTRST Soft reset

“0”: Release reset

“1”: Reset (Auto return zero)

Sleep condition starts after soft reset.

Bit 2: ENMD Enable mode

“0”: Brightness register is latched on edge of EN

“1”: Ignore EN (brightness register is updated immediately)

Bit [1: 0]: MD(1: 0) Mode setup

“00”: Increment mode0 Sleep after register address 1Eh.

Example) 1Ch→1Dh→1Eh→Sleep

“01”: Increment mode1 Return to 03h after register address 1Eh. (Round)

Example) 1Ch→1Dh→1Eh→03h→04h→...

“10”: Increment mode2 Return to 06h after register address 1Eh. (Round)

Example) 1Ch→1Dh→1Eh→06h→07h→...

“11”: Prohibited command

Register address 03h-05h < Write RGB DAC setup>

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03h	W	-	-	DACR5	DACR4	DACR3	DACR2	DACR1	DACR0
04h	W	-	-	DACG5	DACG4	DACG3	DACG2	DACG1	DACG0
05h	W	-	-	DACB5	DACB4	DACB3	DACB2	DACB1	DACB0
Initial value	00h	0	0	0	0	0	0	0	0

DAC (R, G, B) deserve for changing OUT (R, G, B) current.

Bit [5: 0]: RGB DAC setup

"000000": Maximum LED current × 1/64

"000001": Maximum LED current × 2/64

"000010": Maximum LED current × 3/64

"000011": Maximum LED current × 4/64

"000100": Maximum LED current × 5/64

"000101": Maximum LED current × 6/64

"000110": Maximum LED current × 7/64

· ·

· · (Maximum LED current × 1/64 step)

· ·

"111000": Maximum LED current × 57/64

"111001": Maximum LED current × 58/64

"111010": Maximum LED current × 59/64

"111011": Maximum LED current × 60/64

"111100": Maximum LED current × 61/64

"111101": Maximum LED current × 62/64

"111110": Maximum LED current × 63/64

"111111": Maximum LED current × 64/64

Maximum LED current : $I_{LED_max} [mA] = 40 \times 64 / R_{SET} [k\Omega]$ (Typ)

Register address 06h-1Dh <Write OUT** brightness setup>

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
06h – 1Dh	W	BR**(7)	BR**(6)	BR**(5)	BR**(4)	BR**(3)	BR**(2)	BR**(1)	BR**(0)
Initial value	00h	0	0	0	0	0	0	0	0

Bit [7: 0]: OUT** brightness setup

“00000000” : PWM Duty 0/512 LED driver OFF setting (OUT terminal open detect function OFF)

“00000001” : PWM Duty 1/512 1/512 step setting

“00000010” : PWM Duty 2/512 1/512 step setting

“00000011” : PWM Duty 3/512 1/512 step setting

·
· (1/512 step)

“01111101” : PWM Duty 125/512 1/512 step setting

“01111110” : PWM Duty 126/512 1/512 step setting

“01111111” : PWM Duty 128/512 2/512 step setting

“10000000” : PWM Duty 130/512 2/512 step setting

·
· (2/512 step)

“10111100” : PWM Duty 250/512 2/512 step setting

“10111101” : PWM Duty 252/512 2/512 step setting

“10111110” : PWM Duty 256/512 4/512 step setting

“10111111” : PWM Duty 260/512 4/512 step setting

“11000000” : PWM Duty 264/512 4/512 step setting

·
· (4/512 step)

“11111101” : PWM Duty 508/512 4/512 step setting

“11111110” : PWM Duty 512/512 DC setting

It is possible to control PWM brightness by individual channels.

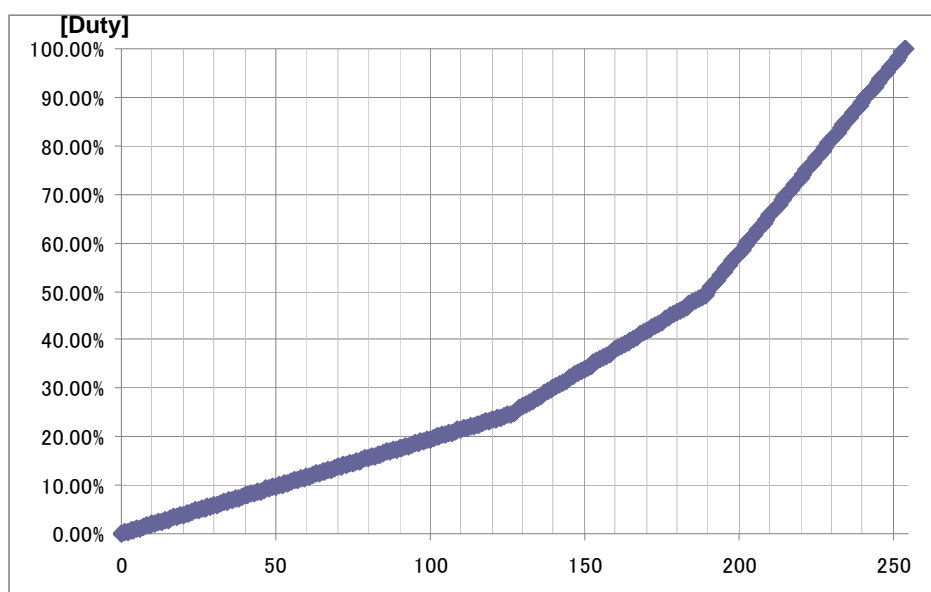


Figure 15. Register setup

Register address 1Eh <Write Enable>

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Eh	W	-	-	-	-	-	-	-	EN
Initial value	00h	0	0	0	0	0	0	0	0

Bit 0: EN enable control

“0”: No reflect

“1”: Reflect into output data of 03h to 1Dh (Auto return zero)

However, this bit is ignored at ENMD=1.

Timing Diagram

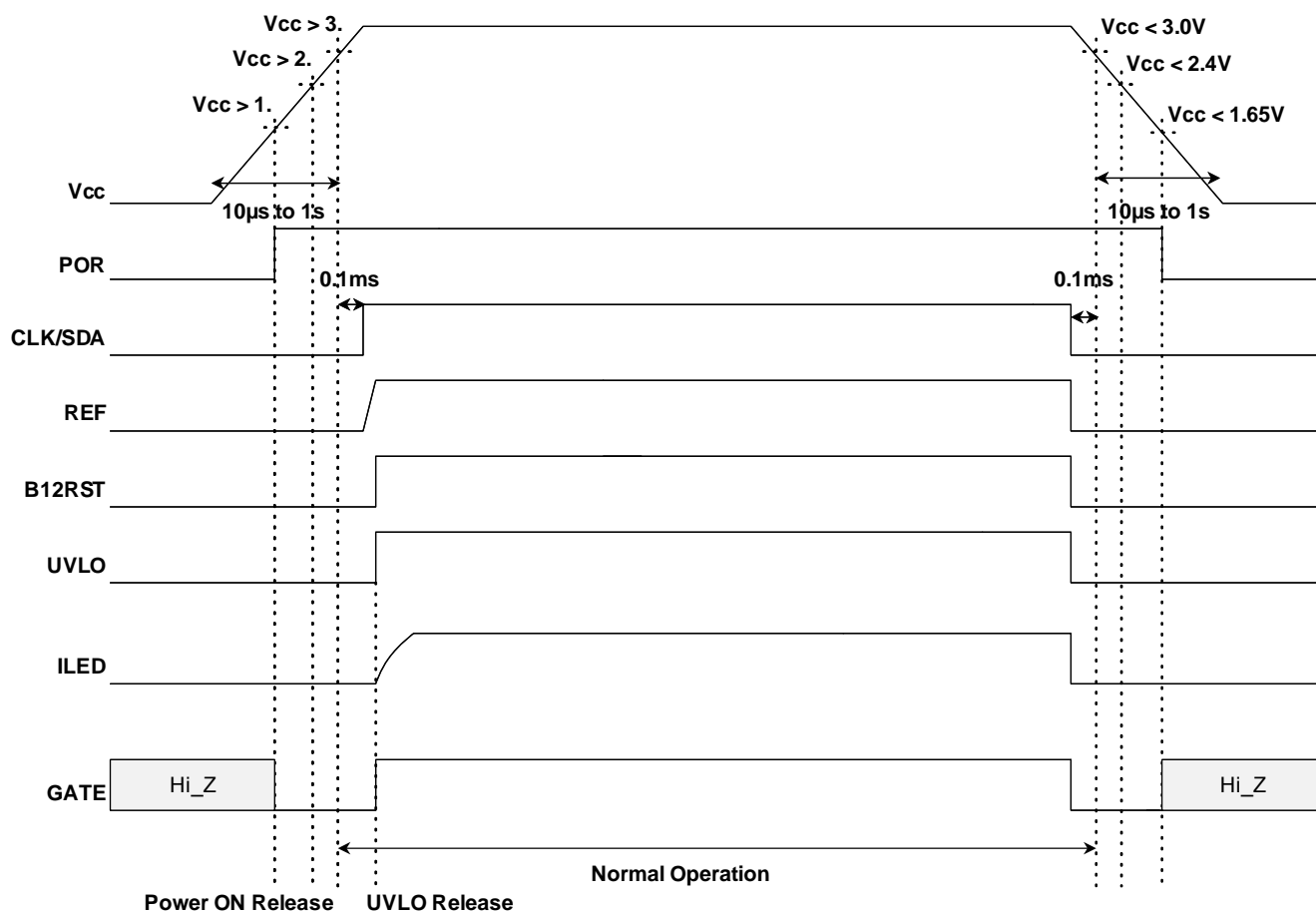


Figure 16. Timing Diagram

The Power supply Rise and Fall time should be in the range of 10μs to 1s.
 Digital communication can only start 0.1ms after VCC exceeds 3V.
 Always set the register voltage lower than VCC voltage.
 Otherwise, when it is driven with more than the VCC, LED may flicker at the start.

Application Example

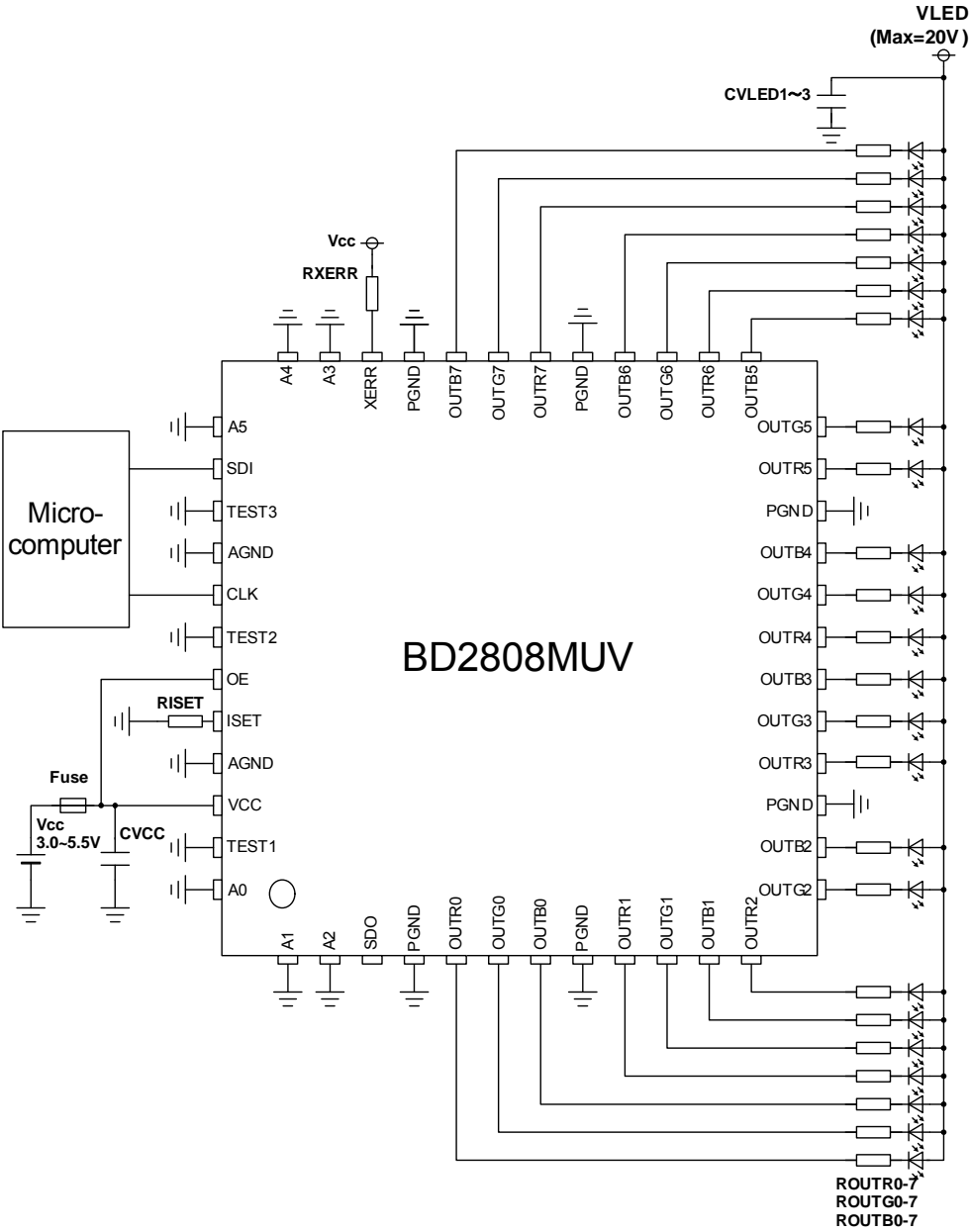


Figure 17. Application Circuit diagram

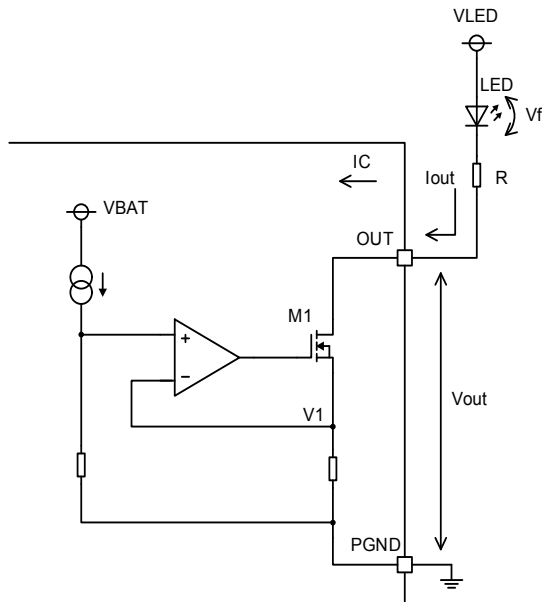
No.	Component Name	Component Value	Product Name	Company
1	CVCC	1μF	GCM188R71C105KA49	Murata
2	Riset	56kΩ	MCR03 Series	Rohm
3	RXERR	10kΩ	MCR03 Series	Rohm
4	CVLED1	4.7μF	GCM31CR71E475KA40	Murata
5	CVLED2	4.7μF	GCM31CR71E475KA40	Murata
6	CVLED3	4.7μF	GCM31CR71E475KA40	Murata
7	ROUTR0-7/ROUTG0-7 /ROUTB0-7	-	ESR25 Series	Rohm

OUT pin and selection of external resistor

(a) Loss on OUT pin

The LED current is controlled by the driver.

However to limit the power dissipation of the IC an external resistor can be used. This resistor limits the V_{out} seen by the IC, to reduce the power dissipation of the IC.



The power dissipation of each channel is given by:

$$P = (V_{LED} - V_f) \times I_{out}$$

$$= V_{OUT} \times I_{out}$$

There are 24 channels and W of total must be less than the power dissipation limit P_d of the IC. Then, the following expression holds true.

$$24 \times P < P_d$$

$$V_{out} < P_d / (I_{out} \times 24) \dots \textcircled{1}$$

For correct operation the following expression must be satisfied

$$V_{out} > V_{OUTmin} \dots \textcircled{2}$$

Figure 18. OUT terminal Output Circuit Diagram

From ① and ②, V_{out} voltage must meet the following ranges

$$V_{OUTmin} < V_{out} < P_d / (I_{out} \times 24)$$

$\dots \textcircled{3}$

(if all 24 channels are active)

When ③ is not satisfied, a resistor is required between OUT pin and LED of the IC to reduce the power dissipation of the IC by dropping the voltage seen by OUT pin.

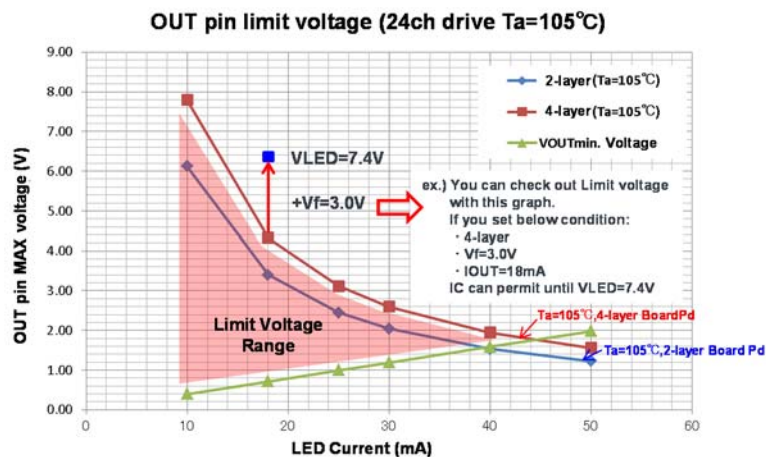


Figure 19. OUT terminal Limit Voltage

(b) OUT pin and GND short

When OUT pin is shorted to GND, high current may flow VLED to GND through the LED.

It is recommended to insert a resistor in the path so that current can be restricted, similar to that of Figure 20.

(c) Constant resistance of OUT pin and setting of LED voltage

Set the value of R by this formula:

$$R < (V_{LED} - V_f - V_{OUT})/I_{out}$$

If there is a maximum current, I_{max} , then the resistor value must meet the following equation:

$$V_{LED} - V_f - V_{OUT}/I_{MAX} < R < (V_{LED} - V_f - V_{OUT})/I_{out}$$

Power Dissipation

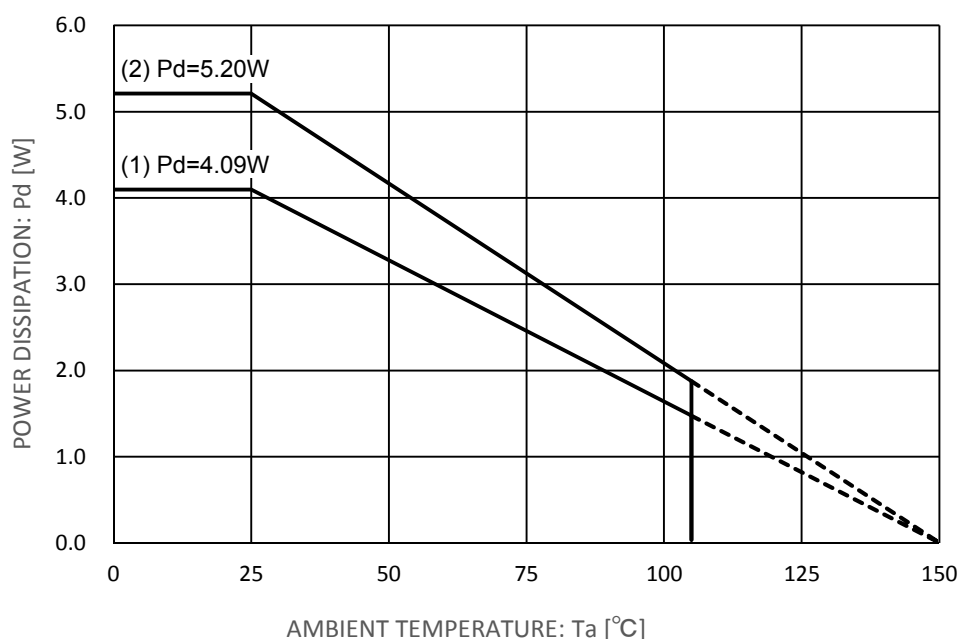


Figure 20. VQFN48MCV070 Power Dissipation

Note 1: Power dissipation is calculated when mounted on 114.3mm X 76.2mm X 1.6mm glass epoxy substrate.

Note 2: Connect the back exposure cooling body of package and board.

Board(1): 2 Layer Board (Back Copper foil 74.2mm × 74.2mm)

$\theta_{ja} = 30.5 \text{ }^{\circ}\text{C/W}$ $P_d = 2.13\text{W}$ ($T_a=85^{\circ}\text{C}$)

Board(2): 4 Layer Board (2,3 Cu Layer, Back Copper foil 74.2mm × 74.2mm)

$\theta_{ja} = 24.0 \text{ }^{\circ}\text{C/W}$ $P_d = 2.71\text{W}$ ($T_a=85^{\circ}\text{C}$)

Power dissipation changes with copper foil density of the board. This value represents only observed values, not guaranteed values.

I/O Equivalence Circuits

Pin46(VCC)	Pin4,8,15,22,29,33 (PGND), Pin40,45(AGND)	Pin44(ISET)
Pin1(A1),Pin2(A2),Pin35(A3), Pin36(A4),Pin37(A5),Pin38(SDI) Pin43(OE),Pin41(CLK),Pin48(A0)	Pin3(SDO)	Pin34(XERR)
Pin5,9,12,16,19,23,26,30 (OUTR[0:7]), Pin6,10,13,17,20,24,27,31(OUTG[0:7]), Pin7,11,14,18,21,25,28,32 (OUTB[0:7])		

() – Pin Name

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

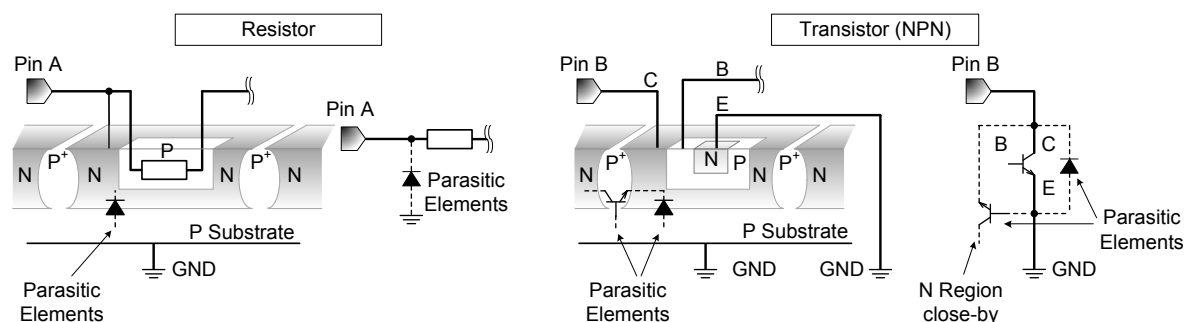


Figure 21. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

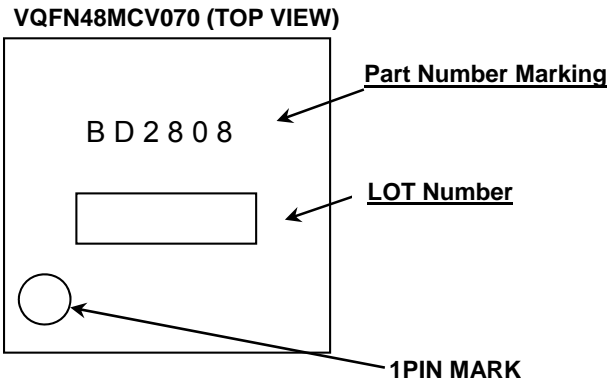
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

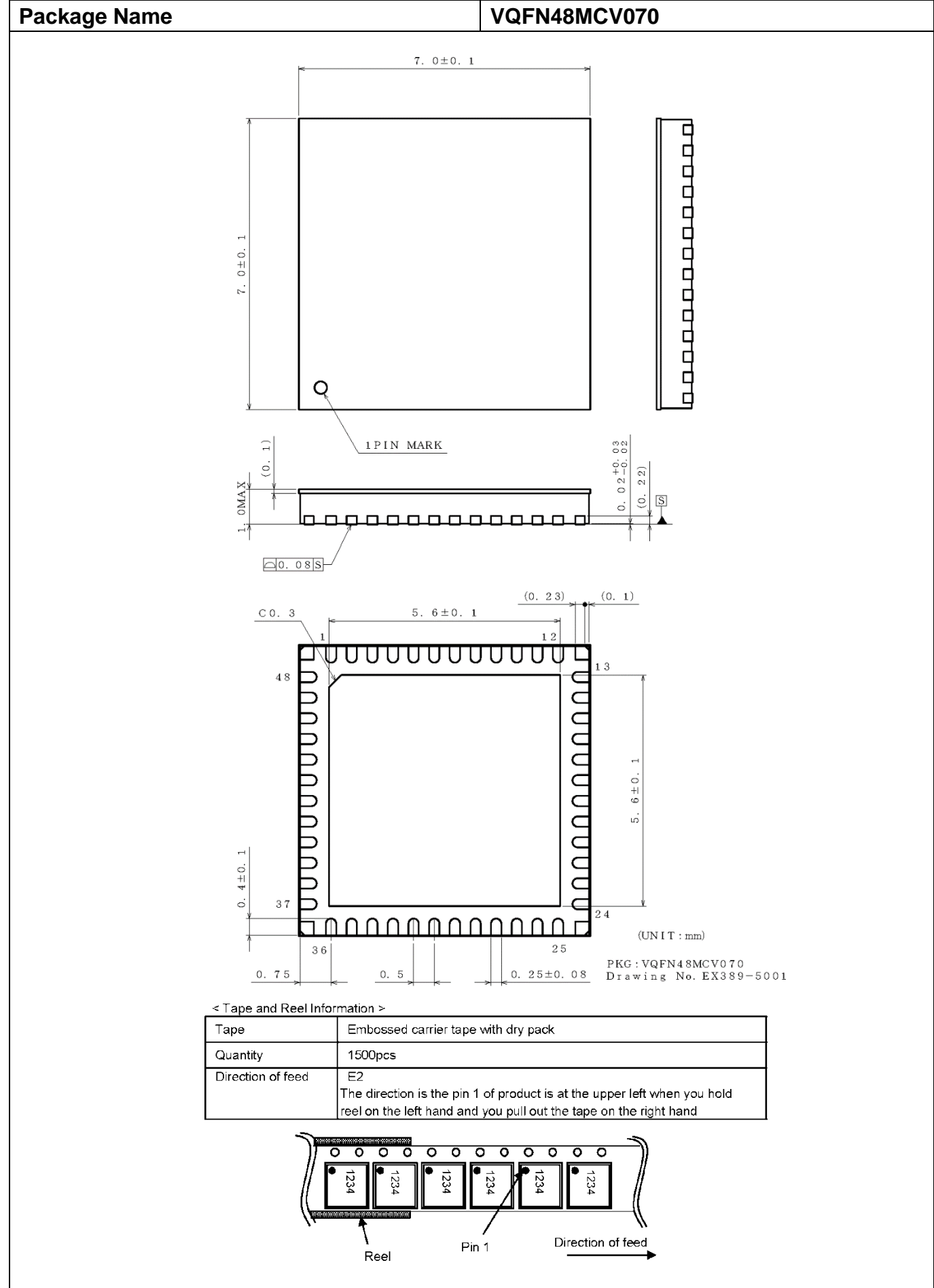
Ordering Information

B D 2 8 0 8 M U V										-	M E 2		
Part Number										Package MUV : VQFN48MCV070			Packaging and forming specification M: High reliability E2: Embossed tape and reel

Marking Diagram



Physical Dimension, Tape and Reel Information



Revision History

Date	Revision	Changes
2014.12.12	001	New Release
2015.06.04	002	Page11 Delete Figure 13, 14 Page23 Add Figure 19

Notice

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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