24AA014/24LC014

1K I²C™ Serial EEPROM

DEVICE SELECTION TABLE

Part Number	Vcc Range	Max Clock	Temp. Range
24AA014	1.8V - 5.5V	400 kHz(1)	I
24LC014	2.5V - 5.5V	400 kHz	I

Note 1: 100 kHz for Vcc < 2.5V

FEATURES

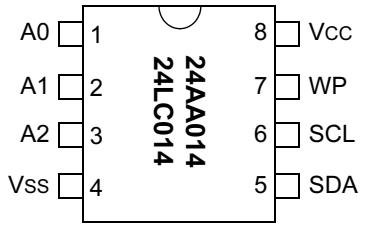
- Single-supply with operation down to 1.8V
- Low-power CMOS technology
  - 1 mA active current, typical
  - 1 μA standby current typical at 5.5V
- Organized as a single block of 128 bytes (128 x 8)
- Hardware write-protection for entire array
- 2-wire serial interface bus, I²C™ compatible
- 100 kHz and 400 kHz clock compatibility
- Page write buffer for up to 16 bytes
- Self-timed write cycle (including auto-erase)
- 10 ms max. write cycle
- Address lines allow up to eight devices on bus
- 1,000,000 erase/write cycles
- ESD protection > 4,000V
- Data retention > 200 years
- 8-pin PDIP, SOIC, TSSOP and MSOP packages
- Available for extended temperature ranges
  - Industrial (I): -40°C to +85°C

DESCRIPTION

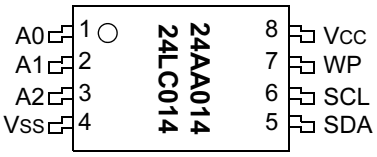
The Microchip Technology Inc. 24AA014/24LC014 is a 1 Kbit Serial Electrically Erasable PROM with operation down to 1.8V. The device is organized as a single block of 128 x 8-bit memory with a 2-wire serial interface. Low current design permits operation with typical standby and active currents of only 1 μA and 1 mA, respectively. The device has a page write capability for up to 16 bytes of data. Functional address lines allow the connection of up to eight 24AA014/24LC014 devices on the same bus for up to 8 Kbits of contiguous EEPROM memory. The device is available in the standard 8-pin PDIP, 8-pin SOIC (150 mil), TSSOP and MSOP packages.

PACKAGE TYPES

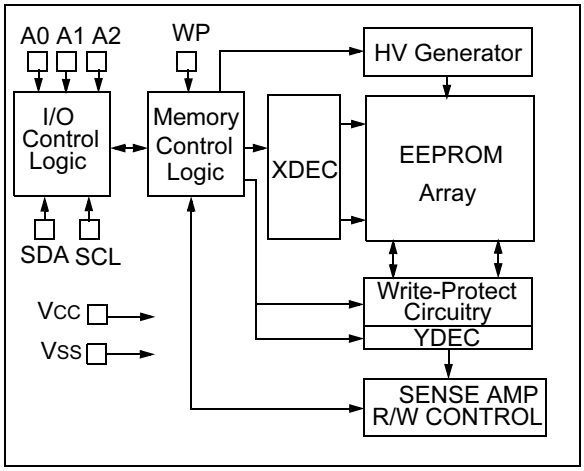
PDIP/SOIC



TSSOP/MSOP



BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temperature with power applied.....-65°C to +125°C
ESD protection on all pins .....≥ 4 KV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Data
SCL	Serial Clock
VCC	Power Supply
A0, A1, A2	Chip Selects
WP	Hardware Write-Protect

TABLE 1-2: DC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	**VCC = +1.8V to +5.5V Industrial (I): TAMB = -40°C to +85°C**				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
SCL and SDA pins:					
High-level input voltage	VIH	0.7 VCC	—	V	—
Low-level input voltage	VIL		0.3 VCC	V	—
Hysteresis of Schmitt Trigger inputs	VHYS	0.05 VCC	—	V	**(Note 1)**
Low-level output voltage	VOL	—	0.40	V	IOL = 3.0 mA, VCC = 4.5V IOL = 2.1 mA, VCC = 2.5V
Input leakage current	ILI	—	±10	µA	VIN = 0.1V to 5.5V, WP = Vss
Output leakage current	ILO	—	±10	µA	VOUT = 0.1V to 5.5V
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V **(Note 1)** TAMB = 25°C, f = 1 MHz
Operating current	ICC Read	—	1	mA	VCC = 5.5V, SCL = 400 kHz
	ICC Write	—	3	mA	VCC = 5.5V
Standby current	ICCS	—	1	µA	VCC = 5.5V, SDA = SCL = VCC WP = VSS, A0, A1, A2 = VSS

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.		**Vcc = 1.8V to 5.5V** **Industrial (I): TAMB = -40°C to +85°C**					
Parameter	**Symbol**	**Vcc = 1.8V - 5.5V STD MODE**		**Vcc = 2.5V - 5.5V FAST MODE**		**Units**	**Remarks**
		Min.	**Max.**	**Min.**	**Max.**		
Clock frequency	FCLK	—	100	—	400	kHz	—
Clock high time	THIGH	4000	—	600	—	ns	—
Clock low time	TLOW	4700	—	1300	—	ns	—
SDA and SCL rise time	TR	—	1000	—	300	ns	**(Note 1)**
SDA and SCL fall time	TF	—	300	—	300	ns	**(Note 1)**
START condition hold time	THD:STA	4000	—	600	—	ns	After this period, the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	**(Note 2)**
Data input setup time	TSU:DAT	250	—	100	—	ns	—
STOP condition setup time	TSU:STO	4000	—	600	—	ns	—
Output valid from clock	TAA	—	3500	—	900	ns	**(Note 2)**
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 +0.1 CB	250	ns	**(Note 1)**, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	**(Note 3)**
Write cycle time	TWC	—	10	—	10	ms	Byte or Page mode
Endurance		1M	—	1M	—	cycles	25°C, **(Note 4)**

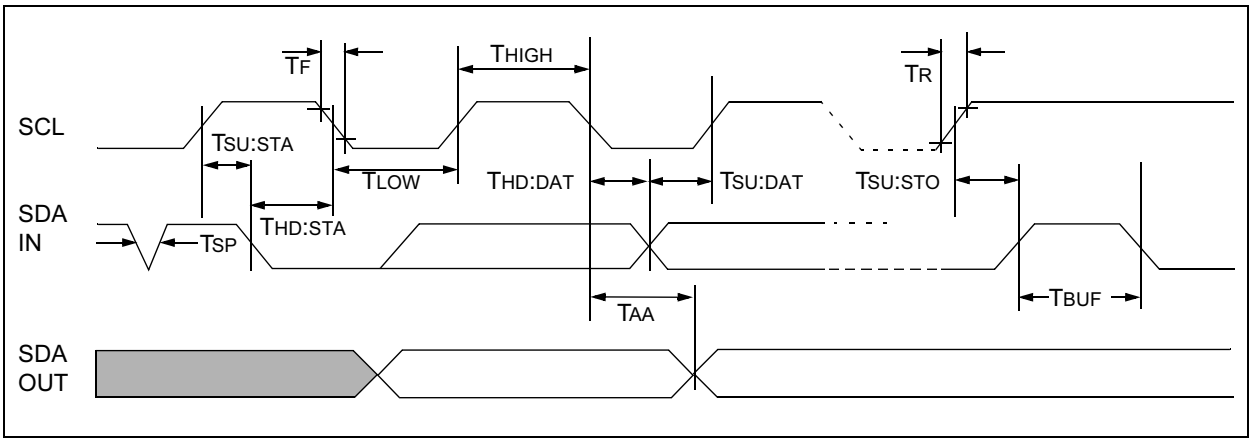
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be downloaded at www.microchip.com.

FIGURE 1-1: BUS TIMING DATA



2.0 PIN DESCRIPTIONS

2.1 SDA Serial Data

This is a bi-directional pin used to transfer addresses and data into and out of the device. It is an open drain terminal. Therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

2.2 SCL Serial Clock

The SCL input is used to synchronize the data transfer to and from the device.

2.3 A0, A1, A2

The levels on the inputs A0, A1 and A2 are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24AA014/24LC014 devices may be connected to the same bus by using different chip select bit combinations. These inputs must be connected to either VCC or VSS.

2.4 WP

WP is the hardware write-protect pin. It must be tied to VCC or VSS. If tied to VCC, the hardware write-protection is enabled. If the WP pin is tied to VSS the hardware write-protection is disabled.

2.5 Noise Protection

The 24AA014/24LC014 employs a VCC threshold detector circuit that disables the internal erase/write logic if the VCC is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits that suppress noise spikes to assure proper device operation even on a noisy bus.

3.0 FUNCTIONAL DESCRIPTION

The 24AA014/24LC014 supports a bi-directional, 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device that generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions while the 24AA014/24LC014 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a START condition. All commands must be preceded by a START condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a STOP condition. All operations must be ended with a STOP condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is, theoretically, unlimited, though only the last sixteen will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first-in first-out fashion.

4.5 Acknowledge

Each receiving device, when addressed, is required to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24AA014/24LC014 does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition (Figure 4-2).

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS CHARACTERISTICS

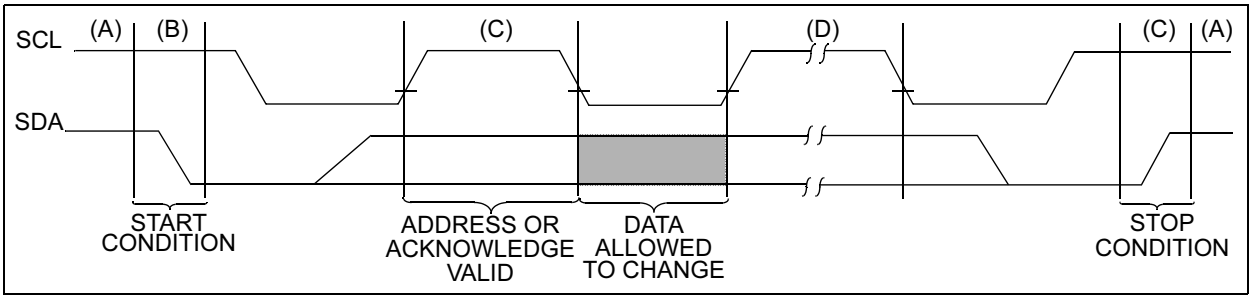
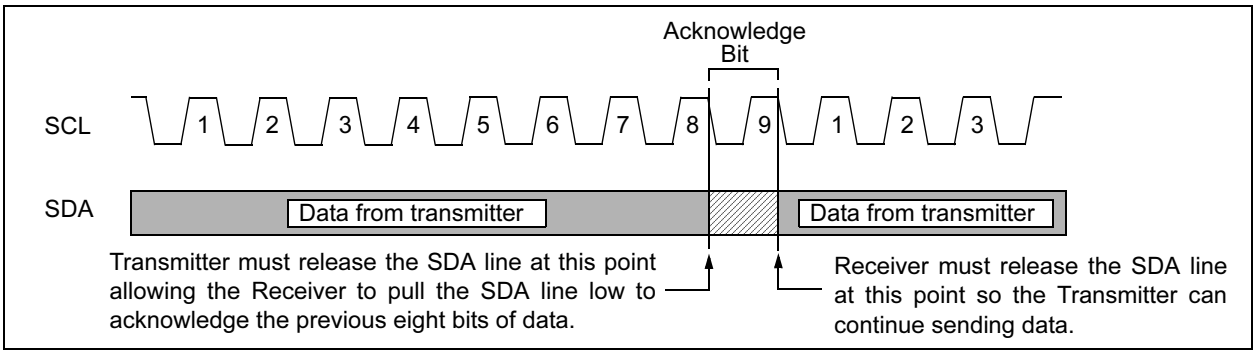


FIGURE 4-2: ACKNOWLEDGE TIMING

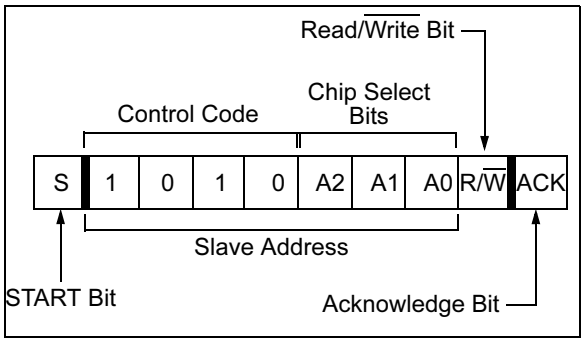


5.0 DEVICE ADDRESSING

A control byte is the first byte received following the START condition from the master device (Figure 5-1). The control byte consists of a four-bit control code; for the 24AA014/24LC014 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the chip select bits (A2, A1, A0). The chip-select bits allow the use of up to eight 24AA014/24LC014 devices on the same bus and are used to select which device is accessed. The chip select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are in effect the three Most Significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a one, a read operation is selected. When set to a zero, a write operation is selected. Following the START condition, the 24AA014/24LC014 monitors the SDA bus, checking the control byte being transmitted. Upon receiving a 1010 code and appropriate chip select bits, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA014/24LC014 will select a read or write operation.

FIGURE 5-1: CONTROL BYTE FORMAT



5.1 Contiguous Addressing Across Multiple Devices

The chip select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 16K bits by adding up to eight 24AA014/24LC014 devices on the same bus. In this case, software can use A0 of the control byte as address bit A8, A1 as address bit A9 and A2 as address bit A10. It is not possible to sequentially read across device boundaries.

6.0 WRITE OPERATIONS

6.1 Byte Write

Following the start signal from the master, the device code (4 bits), the chip select bits (3 bits) and the R/$\overline{W}$ bit (which is a logic low) are placed onto the bus by the master transmitter. The device will acknowledge this control byte during the ninth clock pulse. The next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA014/24LC014. After receiving another Acknowledge signal from the 24AA014/24LC014, the master device will transmit the data word to be written into the addressed memory location. The 24AA014/24LC014 acknowledges again and the master generates a STOP condition. This initiates the internal write cycle and the 24AA014/24LC014 will not generate Acknowledge signals during this time (Figure 6-1). If an attempt is made to write to the protected portion of the array when the hardware write-protection has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if write-protection is enabled.

6.2 Page Write

The write-control byte, word address and the first data byte are transmitted to the 24AA014/24LC014 in the same way as in a byte write. But instead of generating a STOP condition, the master transmits up to 15 additional data bytes to the 24AA014/24LC014 that are temporarily stored in the on-chip page buffer and will be written into the memory once the master has transmitted a STOP condition. Upon receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order four bits of the word address remain constant. If the master should transmit more than 16 bytes prior to generating the STOP condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the STOP condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the protected portion of the array when the hardware write-protection has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if write-protection is enabled.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary that the application software prevent page write operations that would attempt to cross a page boundary.

6.3 WRITE-PROTECTION

The WP pin must be tied to VCC or VSS. If tied to VCC, the entire array will be write-protected. If the WP pin is tied to VSS, write operations to all address locations are allowed.

FIGURE 6-1: BYTE WRITE

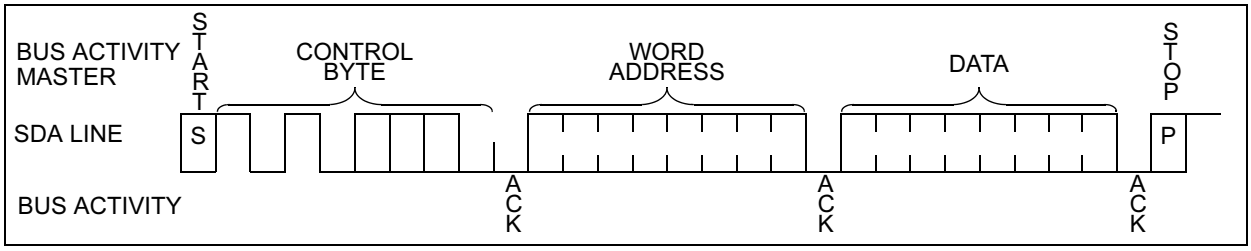
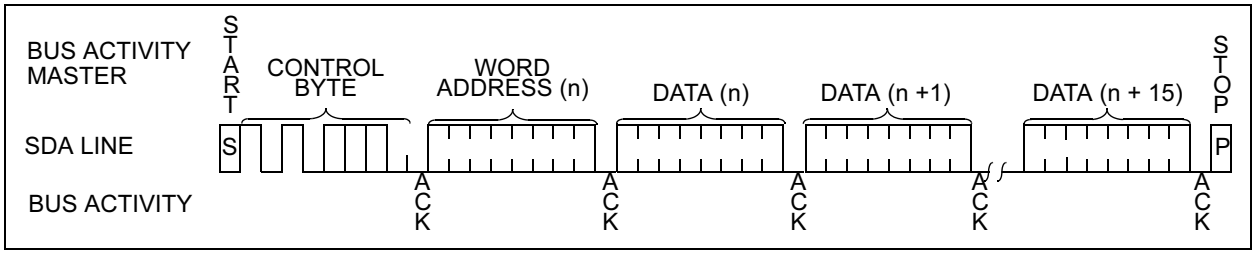


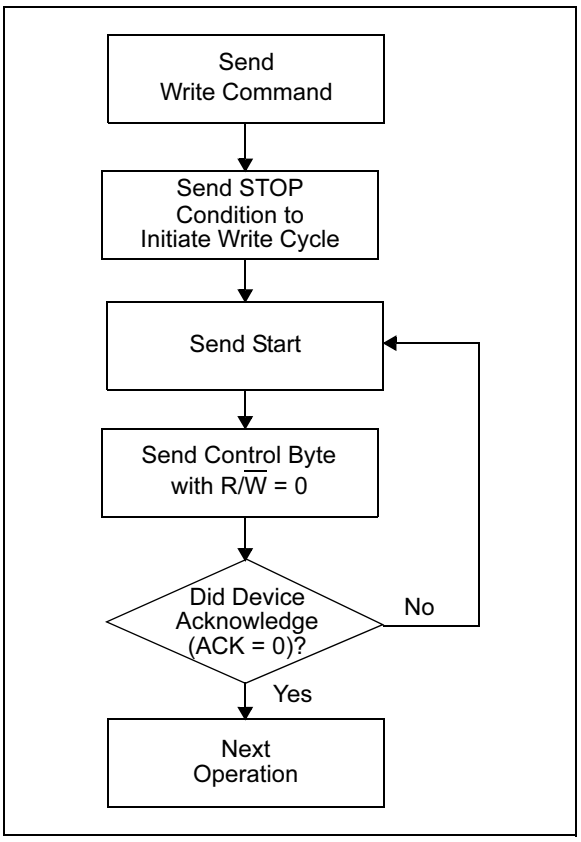
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the STOP condition for a write command has been issued from the master, the device initiates the internally-timed write cycle and ACK polling can be initiated immediately. This involves the master sending a START condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, no ACK will be returned. If no ACK is returned, the START bit and control byte must be resent. If the cycle is complete, the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for a flow diagram of this operation.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATIONS

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24AA014/24LC014 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to '1', the 24AA014/24LC014 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a STOP condition and the 24AA014/24LC014 discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is done by sending the word address to the 24AA014/24LC014 as part of a write operation. Once the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. The master then issues the control byte again but with the R/$\overline{W}$ bit set to a '1'. The 24AA014/24LC014 will then issue an acknowledge and transmits the eight-bit data word. The master will not acknowledge the transfer but does generate a STOP condition and the 24AA014/24LC014 discontinues transmission (Figure 8-2). After this command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA014/24LC014 transmits the first data byte, the master issues an acknowledge as opposed to a STOP condition in a random read. This directs the 24AA014/24LC014 to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads the 24AA014/24LC014 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 0FFh to address 000h.

FIGURE 8-1: CURRENT ADDRESS READ

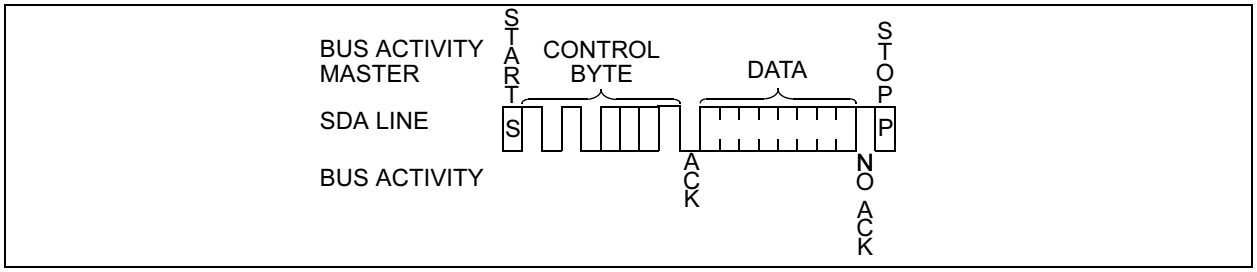


FIGURE 8-2: RANDOM READ

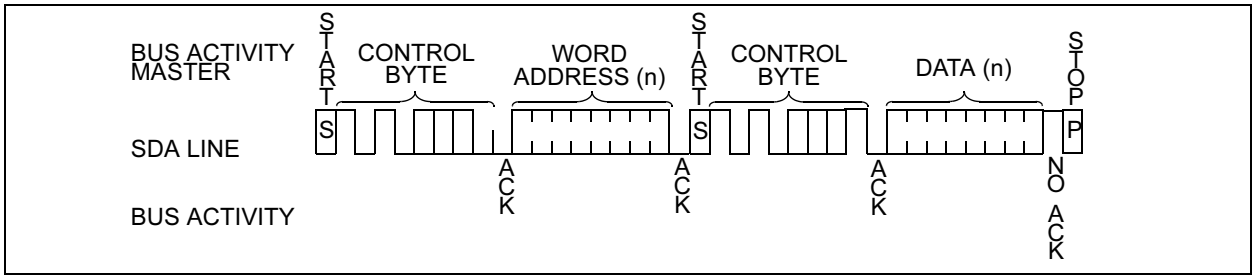
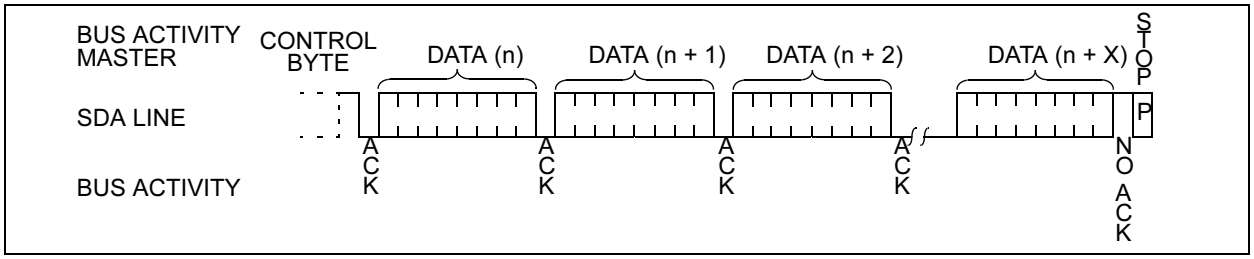


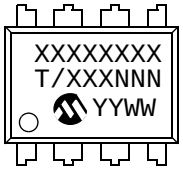
FIGURE 8-3: SEQUENTIAL READ



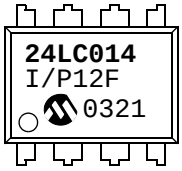
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

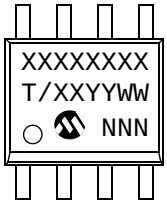
8-Lead PDIP (300 mil)



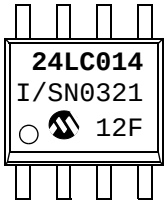
Example:



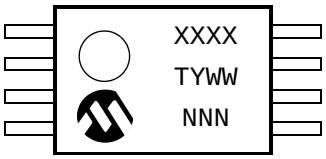
8-Lead SOIC (150 mil)



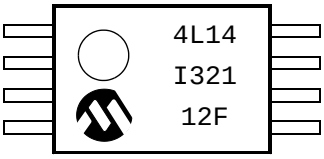
Example:



8-Lead TSSOP

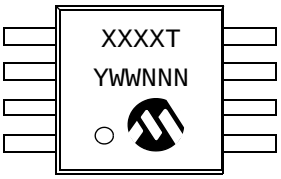


Example:

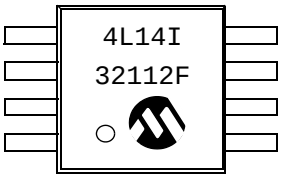


Part Number	TSSOP/MSOP Marking Code
24AA014	4A14
24LC014	4L14

8-Lead MSOP



Example:

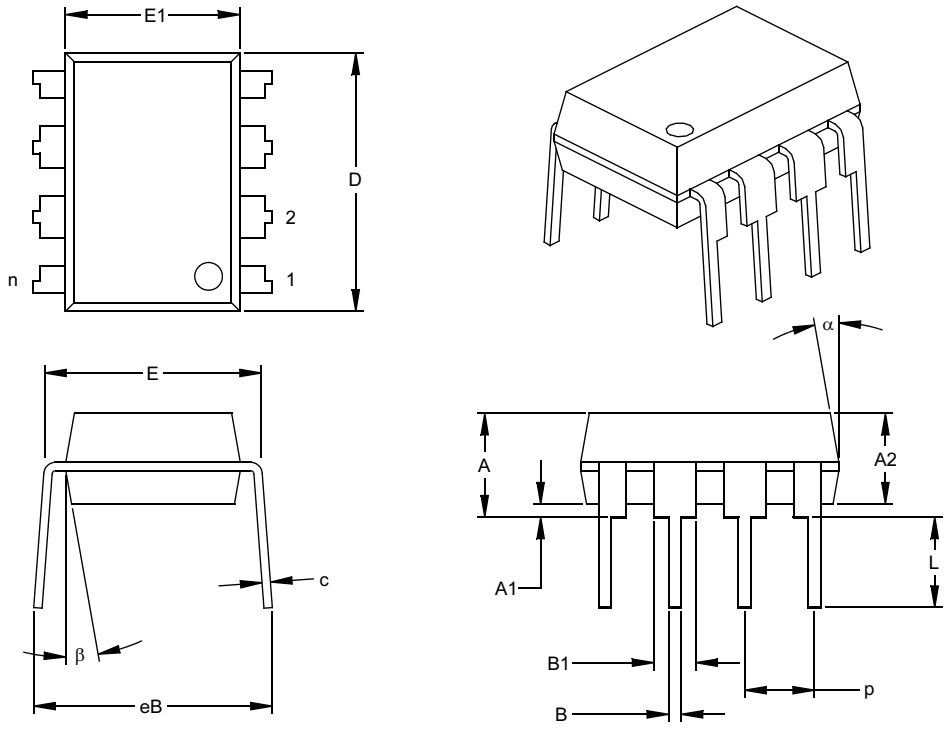


Legend:	XX...X	Customer specific information*
	T	Temperature grade (I,E)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

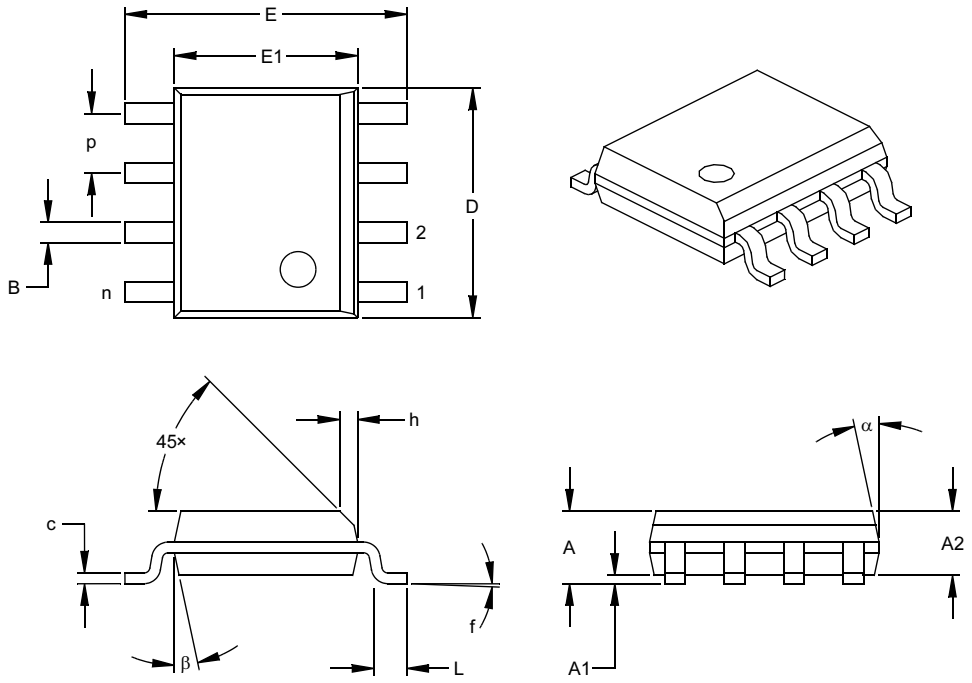


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

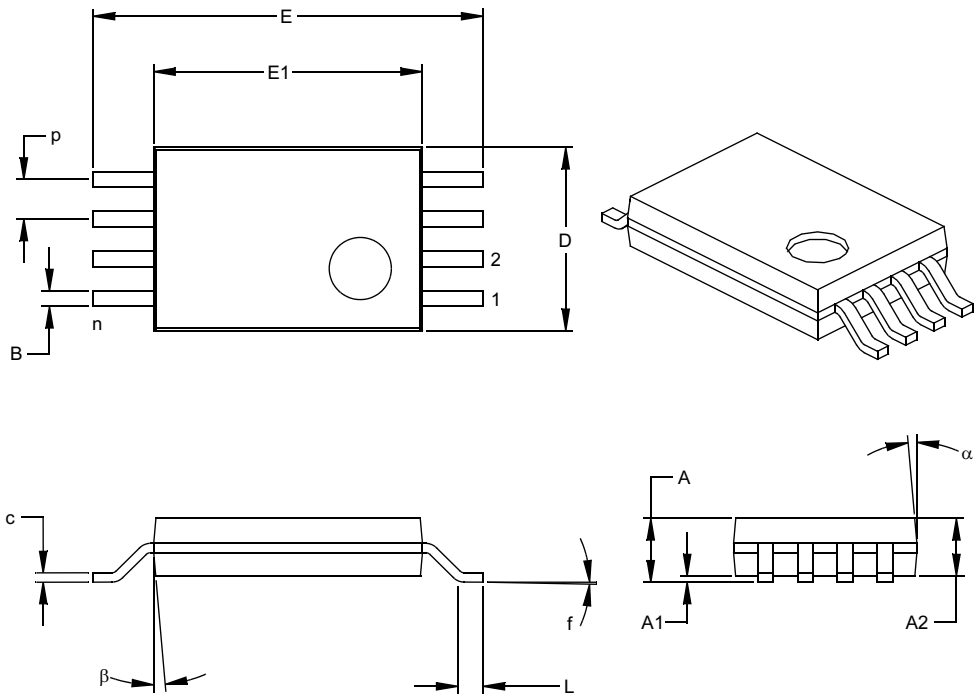


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)

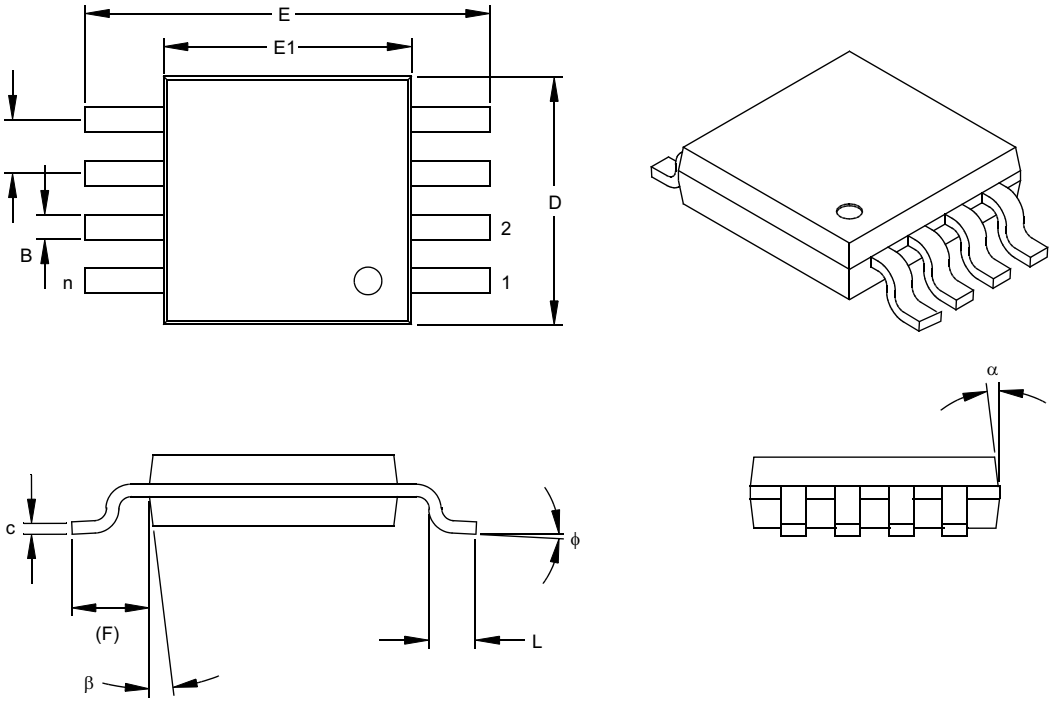


Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

8-Lead Plastic Micro Small Outline Package (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p		.026			0.65	
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	.5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	ϕ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

*Controlling Parameter
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed.010" (0.254mm) per side.

Drawing No. C04-111

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	24AA014:	1.8V, 1 Kbit Addressable Serial EEPROM	
	24AA014T:	1.8V, 1 Kbit Addressable Serial EEPROM (Tape and Reel)	
	24LC014:	2.5V, 1 Kbit Addressable Serial EEPROM	
	24LC014T:	2.5V, 1 Kbit Addressable Serial EEPROM (Tape and Reel)	
Temperature Range:	I	=	-40°C to +85°C
Package:	P	=	Plastic DIP, (300 mil Body), 8-lead
	SN	=	Plastic SOIC, (150 mil Body)
	ST	=	TSSOP, 8-lead
	MS	=	MSOP, 8-lead

Examples:

a) 24AA014-I/P: Industrial Temperature, 1.8V, PDIP package.
b) 24AA014-I/SN: Industrial Temperature, 1.8V, SOIC Package.
c) 24AA014T-I/ST: Industrial Temperature, 1.8V, TSSOP Package, Tape and Reel

a) 24LC014-I/P: Industrial Temperature, 2.5V, PDIP Package.
b) 24LC014T-I/SN: Industrial Temperature, 2.5V, SOIC Package, Tape and Reel
c) 24LC014T-I/MS: Industrial Temperature, 2.5V, MSOP Package, Tape and Reel.

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1. Your local Microchip sales office
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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