



256-Position SPI Compatible Digital Potentiometer

Preliminary Technical Data

AD5160

FEATURES

- 256-Position
- End-to-End Resistance 5k, 10k, 50k, 100k Ω
- Compact SOT23-8 (2.9 x 3mm) Package
- SPI Compatible Interface
- Power ON Reset to Midscale
- Single Supply +2.7V to +5.5V
- Low Temperature Coefficient 35ppm/ $^{\circ}$ C
- Low power, $I_{DD}=5\mu$ A
- Wide Operating Temperature -40° C to $+125^{\circ}$ C

Applications

- Mechanical Potentiometer Replacement in new designs
- Transducer Adjustment of pressure, temperature, position, chemical and optical sensors
- RF Amplifier biasing
- Automotive Electronics Adjustment
- Gain Control and Offset Adjustment

GENERAL DESCRIPTION

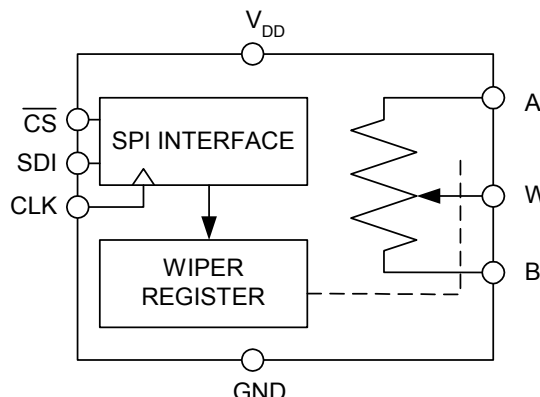
The AD5160 provides a compact 2.9x3mm packaged solution for 256-position adjustment applications.

This device performs the same electronic adjustment function as a mechanical potentiometer or a variable resistor. Available in four different end-to-end resistance values (5k, 10k, 50k, 100k Ω) these low temperature coefficient devices are ideal for high accuracy and stability variable resistance adjustments.

The wiper settings are controllable through the SPI compatible digital interface. The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the RDAC latch¹.

Operating from a 2.7 to 5.5 volt power supply consuming less than 5 μ A allows for usage in portable battery operated applications.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

1	W	A	8
2	V _{DD}	B	7
3	GND	$\overline{\text{CS}}$	6
4	CLK	SDI	5

Notes:

1. The terms digital potentiometers, VR, and RDAC are used interchangeably.

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PRELIMINARY TECHNICAL DATA

256 Position Digital Potentiometer

AD5160

AD5160 ELECTRICAL CHARACTERISTICS 5K, 10K, 50K, 100KΩ VERSION ($V_{DD} = +5V \pm 10\%$, or $+3V \pm 10\%$, $V_A = +V_{DD}$, $V_B = 0V$, $-40^\circ C < T_A < +125^\circ C$ unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential Nonlinearity ²	R-DNL	R_{WB} , $V_A = \text{No Connect}$	-1	± 0.25	+1	LSB
Resistor Integral Nonlinearity ²	R-INL	R_{WB} , $V_A = \text{No Connect}$	-2	± 0.5	+2	LSB
Nominal Resistor Tolerance ³	ΔR_{AB}	$T_A = 25^\circ C$	-30		30	%
Resistance Temperature Coefficient	$R_{AB}/\Delta T$	$V_{AB} = V_{DD}$, Wiper = No Connect		35		ppm/ $^\circ C$
Wiper Resistance	R_W	$V_{DD} = +5V$		50	100	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE Specifications apply to all VRs						
Resolution	N		8			Bits
Differential Nonlinearity ⁴	DNL		-1	$\pm 1/4$	+1	LSB
Integral Nonlinearity ⁴	INL		-2	$\pm 1/2$	+2	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 80 _H		5		ppm/ $^\circ C$
Full-Scale Error	V_{WFSE}	Code = FF _H	-1.5	-0.5	+0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00 _H	0	+0.5	+1.5	LSB
RESISTOR TERMINALS						
Voltage Range ⁵	$V_{A,B,W}$		V_{SS}		V_{DD}	V
Capacitance ⁶ A, B	$C_{A,B}$	$f = 1 \text{ MHz}$, measured to GND, Code = 80 _H		45		pF
Capacitance ⁶ W	C_W	$f = 1 \text{ MHz}$, measured to GND, Code = 80 _H		60		pF
Shutdown Supply Current ⁷	I_{DD_SD}	$V_{DD} = 5.5V$		0.01	5	μA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS & OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	$V_{DD} = +3V$	2.1			V
Input Logic Low	V_{IL}	$V_{DD} = +3V$			0.6	V
Input Current	I_{IL}	$V_{IN} = 0V$ or $+5V$			± 1	μA
Input Capacitance ⁶	C_{IL}			5		pF
POWER SUPPLIES						
Logic Supply	V_{LOGIC}		2.7		5.5	V
Power Supply Range	$V_{DD \text{ RANGE}}$	$V_{SS} = 0V$	-0.3		5.5	V
Supply Current	I_{DD}	$V_{IH} = +5V$ or $V_{IL} = 0V$		5		μA
Power Dissipation ⁸	P_{DISS}	$V_{IH} = +5V$ or $V_{IL} = 0V$, $V_{DD} = +5V$			0.2	mW
Power Supply Sensitivity	PSS	$\Delta V_{DD} = +5V \pm 10\%$, Code = Midscale	-0.01	0.001	+0.01	%/%
DYNAMIC CHARACTERISTICS ^{6, 9}						
Bandwidth -3dB	BW_10K	$R_{AB} = 10K\Omega$, Code = 80 _H		600		KHz
Bandwidth -3dB	BW_50K	$R_{AB} = 50K\Omega$, Code = 80 _H		100		KHz
Total Harmonic Distortion	THD _W	$V_A = 1V_{rms}$, $V_B = 0V$, $f = 1KHz$, $R_{AB} = 10K\Omega$		0.003		%
V_W Settling Time (10K Ω /50K Ω)	t_S	$V_A = 5V$, $V_B = 0V$, ± 1 LSB error band		2/9		μs
Resistor Noise Voltage Density	e_{N_WB}	$R_{WB} = 5K\Omega$, $RS = 0$		9		nV/ $\sqrt{Hz}$

PRELIMINARY TECHNICAL DATA

256 Position Digital Potentiometer

AD5160

AD5160 ELECTRICAL CHARACTERISTICS 5K, 10K, 50K, 100KΩ VERSION ($V_{DD} = +5V \pm 10\%$, or $+3V \pm 10\%$, $V_A = +V_{DD}$, $V_B = 0V$, $-40^\circ C < T_A < +125^\circ C$ unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Units
INTERFACE TIMING CHARACTERISTICS applies to all parts (Notes 6,10)						
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock level high or low		20		ns
Data Setup Time	t_{DS}			5		ns
Data Hold Time	t_{DH}			5		ns
$\overline{CS}$ Setup Time	t_{CSS}			15		ns
$\overline{CS}$ High Pulse Width	t_{CSW}			40		ns
CLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}			0		ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH}			0		ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}			10		ns

NOTES:

- Typicals represent average readings at $+25^\circ C$ and $V_{DD} = +5V$.
- Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
- $V_{AB} = V_{DD}$, Wiper (V_W) = No connect
- INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and $V_B = 0V$. DNL specification limits of $\pm 1LSB$ maximum are Guaranteed Monotonic operating conditions.
- Resistor terminals A,B,W have no limitations on polarity with respect to each other.
- Guaranteed by design and not subject to production test.
- Measured at the A terminal. A terminal is open circuited in shutdown mode.
- P_{DISS} is calculated from $(I_{DD} \times V_{DD})$. CMOS logic level inputs result in minimum power dissipation
- All dynamic characteristics use $V_{DD} = +5V$.
- See timing diagram for location of measured values. All input control voltages are specified with $t_R = t_F = 2ns$ (10% to 90% of $+3V$) and timed from a voltage level of 1.5V. Switching characteristics are measured using $V_{Logic} = +5V$.
- The AD5160 contains 2532 transistors. Die Size: 30.7mil x 76.8 mil, 2358sq. mil.
- See timing diagram for location of measured values.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5160 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



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AD5160

ABSOLUTE MAXIMUM RATINGS¹ ($T_A = +25^\circ\text{C}$, unless otherwise noted)

V_{DD} to GND	-0.3, +7V
V_A , V_B , V_W to GND	V_{DD}
I_{MAX}	$\pm 20\text{mA}$ ²
Digital Inputs & Output Voltage to GND	0V, +7V
Operating Temperature Range	-40°C to $+125^\circ\text{C}$
Maximum Junction Temperature (T_{JMAX})	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$+300^\circ\text{C}$
Thermal Resistance ³ θ_{JA} , SOT23-8	230°C/W

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance

3. Package Power Dissipation ($T_{JMAX} - T_A$) / θ_{JA}

ORDERING GUIDE

Model#	R_{AB} (Ω)	Package Description	Package Option	Brand
AD5160BRJ5	5K	SOT23-8	RJ-8	D08
AD5160BRJ10	10K	SOT23-8	RJ-8	D09
AD5160BRJ50	50K	SOT23-8	RJ-8	D0A
AD5160BRJ100	100K	SOT23-8	RJ-8	D0B

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TABLE 1: AD5160 Serial-Data Word Format

B7	B6	B5	B4	B3	B2	B1	B0
D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB
2^7							2^0

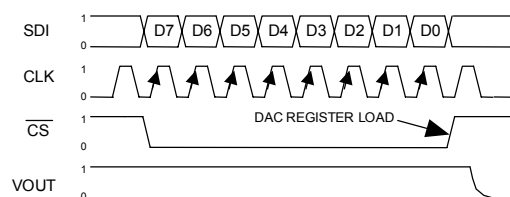


Figure 1A. AD5160 Timing Diagram($V_A = 5V$, $V_B = 0V$, $V_W = V_{OUT}$)

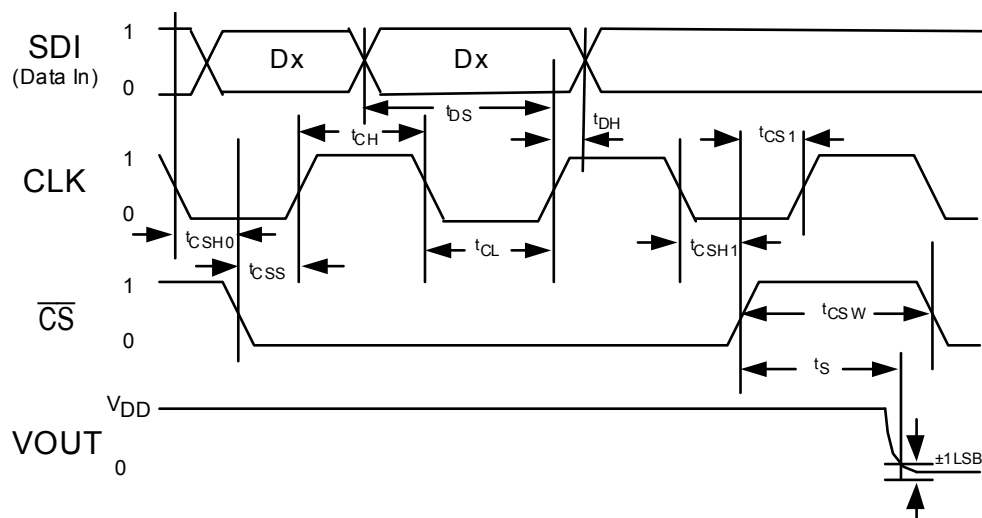


Figure 1B. Detail Timing Diagram($V_A = 5V$, $V_B = 0V$, $V_W = V_{OUT}$)

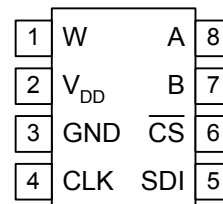
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TABLE 2: AD5160 PIN Descriptions

Pin	Name	Description
1	V_W	W Terminal
2	V_{DD}	Positive Power Supply
3	GND	Ground
4	CLK	Serial Clock Input, positive edge triggered
5	SDI	Serial Data Input
6	$\overline{CS}$	Chip Select Input, Active Low. When CS returns high, data will be loaded into the DAC register.
7	V_B	B Terminal
8	V_A	A Terminal

PIN CONFIGURATION



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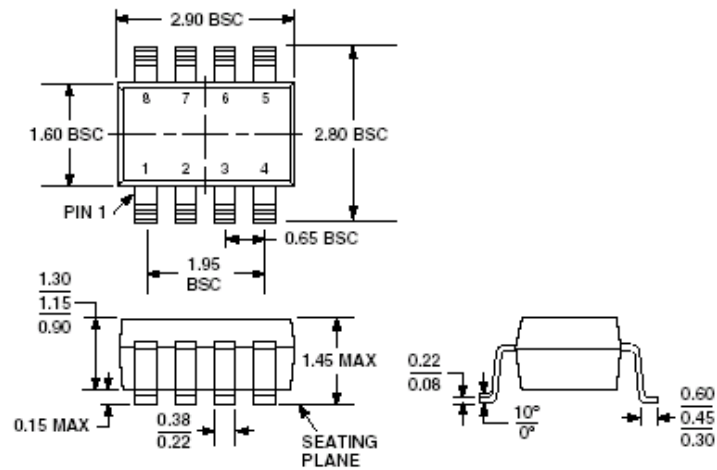
AD5160

OUTLINE DIMENSIONS

8-Lead Plastic Surface-Mount Package [SOT-23]

RJ-8

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178BA