

Smart Modular Compact Linear Flash™ Memory Card - with 3V Intel® StrataFlash™ Components

Description

The Smart Modular Technology Compact Linear Flash™(CLF) card is a Linear FLASH Memory Card in a Compact form factor, which provides a flexible storage medium and large memory capacity. These cards incorporate Intel® manufactured StrataFlash™ memory components to provide battery-free, non-volatile preservation of data and/or programs, with no requirement for additional voltages (V_{pp}) to support card erase/program operations.

With several embedded program/erase algorithms to choose from, host system designers can make trade off decisions regarding card performance, including programming speed and card power consumption.

Features

- Extremely Convenient Storage Solution
 - ◆ Small (3.3 x 36.4 x 42.8 mm) Form Factor
 - ◆ Large Storage Capacity
 - ◆ Light Weight
 - ◆ Rugged, Reliable, Removable and Replaceable
 - ◆ 2.7V to 3.6V supply voltage operation
- Card Architecture
 - ◆ Embedded Program/Erase Algorithms
 - ◆ 128 Kilobyte Erase Sector Resolution
 - ◆ Erase Suspend/Resume Capabilities
 - ◆ High Write Endurance
 - ◆ Battery Free, Non-Volatile Storage
 - ◆ CMOS compatible inputs and outputs
 - ◆ Up to 16MWords(32MB) of data storage
- ISO 9001 Quality Controls

PIN DESCRIPTION

Signal	Name	Function
A[24:1]	Address Bus	Address Inputs, A24-A1
D[15:0]	Data Bus	Data Input/Outputs
/OE	Output Enable	Active Low for Read
/WE	Write Enable	Active Low for Write
/CE1	Card Enable Low Byte	Active Low for Read/ Write Even Byte
/CE2	Card Enable High Byte	Active Low for Read/ Write Odd Byte
/CD1	Card Detect	Tied to GND
/CD2	Card Detect	Tied to GND
V_{CC}	Power Supply	Power Supply Voltage, +2.7V to +3.6V
GND (V_{SS})	Ground	Card Ground

PIN ASSIGNMENTS

Pin #	Signal	I/O	Function	Pin #	Signal	I/O	Function
1	GND		Card Ground	26	/CD1	O	Card Detect 1
2	D3	I/O	Data Bit 3	27	D11	I/O	Data Bit 11
3	D4	I/O	Data Bit 4	28	D12	I/O	Data Bit 12
4	D5	I/O	Data Bit 5	29	D13	I/O	Data Bit 13
5	D6	I/O	Data Bit 6	30	D14	I/O	Data Bit 14
6	D7	I/O	Data Bit 7	31	D15	I/O	Data Bit 15
7	/CE1	I	Chip Enable Even Byte	32	/CE2	I	Card Enable Odd Byte
8	A11	I	Address Bit 11	33	A22	I	Address Bit 22
9	/OE	I	Output Enable	34	A21	I	Address Bit 21
10	A10	I	Address Bit 10	35	A20	I	Address Bit 20
11	A9	I	Address Bit 9	36	/WE	I	Write Enable
12	A8	I	Address Bit 8	37	A24	I	Address Bit 24 <i>(Note 1)</i>
13	Vcc		Voltage Power Supply	38	Vcc		Voltage Power Supply
14	A7	I	Address Bit 7	39	A19	I	Address Bit 19
15	A6	I	Address Bit 6	40	A18	I	Address Bit 18
16	A5	I	Address Bit 5	41	A23	I	Address Bit 23 <i>(Note 2)</i>
17	A4	I	Address Bit 4	42	A17	I	Address Bit 17
18	A3	I	Address Bit 3	43	A16	I	Address Bit 16
19	A2	I	Address Bit 2	44	A15	I	Address Bit 15
20	A1	I	Address Bit 1	45	A14	I	Address Bit 14
21	D0	I/O	Data Bit 0	46	A13	I	Address Bit 13
22	D1	I/O	Data Bit 1	47	D8	I/O	Data Bit 8
23	D2	I/O	Data Bit 2	48	D9	I/O	Data Bit 9
24	A12	I	Address Bit 12	49	D10	I/O	Data Bit 10
25	/CD2	O	Card Detect 2	50	GND		Card Ground

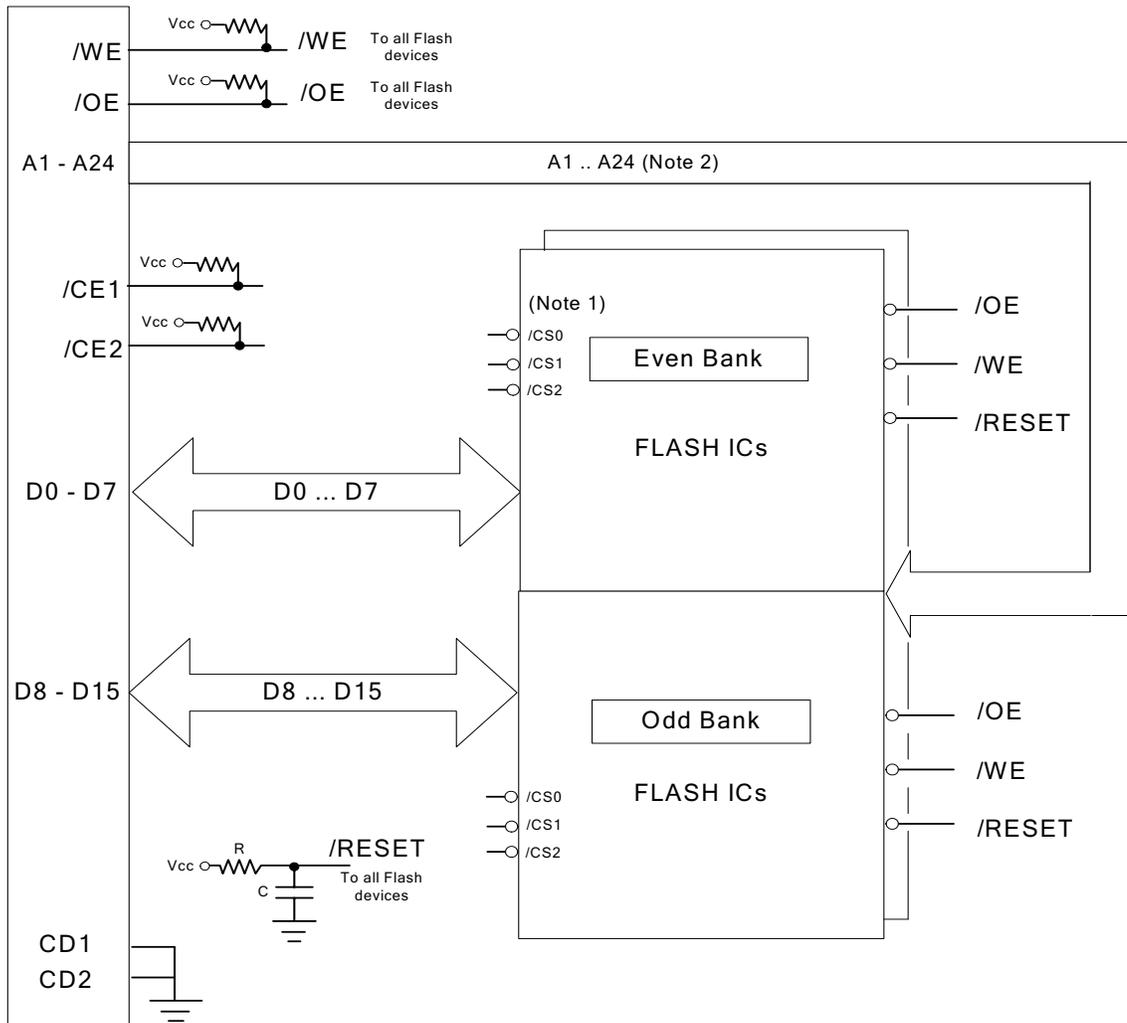
Notes:

1. This address line is not connected for cards less than 32Mbytes in capacity.
2. This address line is not connected for cards less than 16Mbytes in capacity.

Legend:

- I = Input to card only
- O = Output from card only
- I/O = Bi-directional signal
- / = Active Low Signal

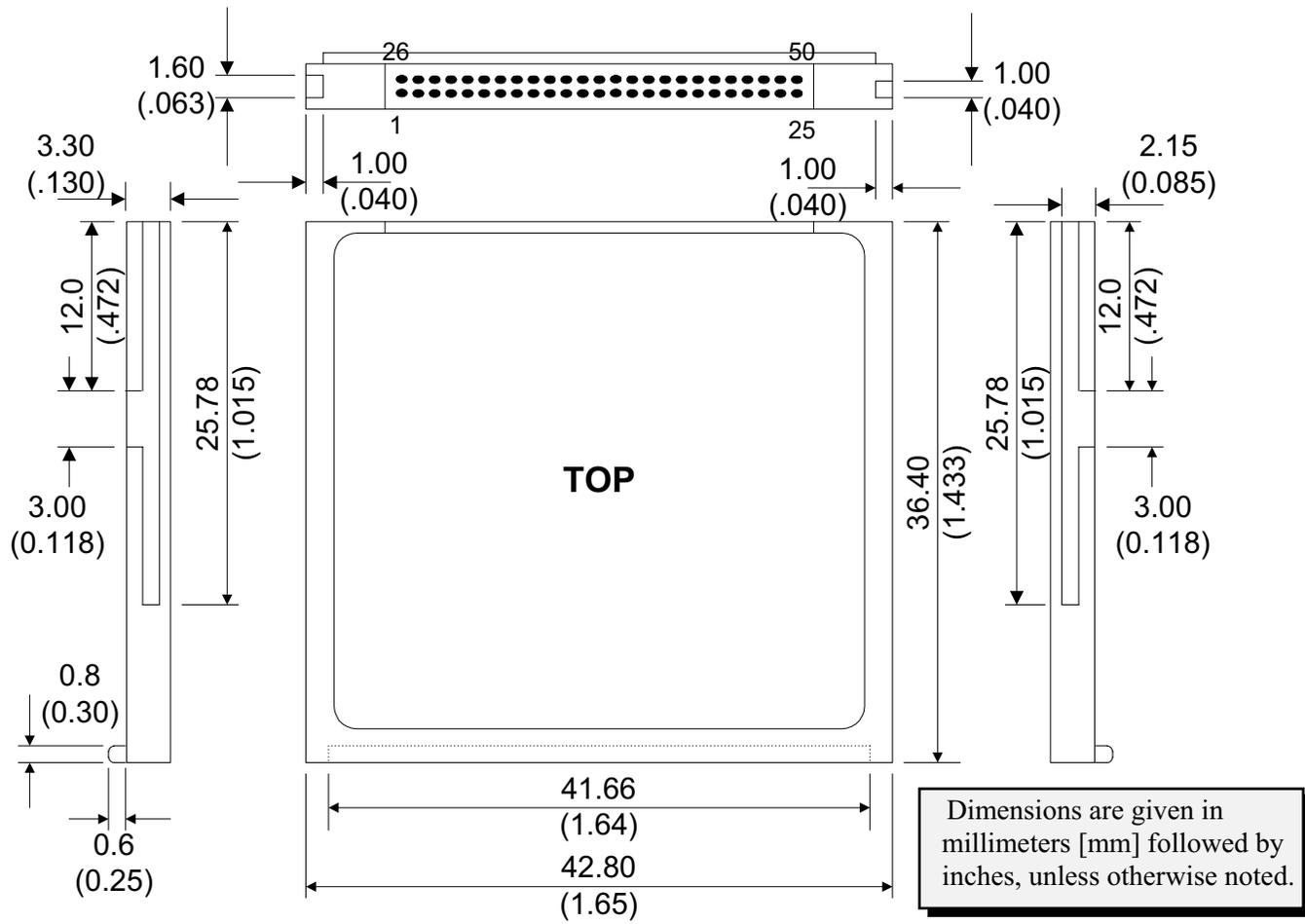
FUNCTIONAL BLOCK DIAGRAM



Note 1: The routing of signals /CS[2:0] are dependent on flash chip capacity and card capacity.

Note 2: The address lines A[24:23] may be No Connects depending on card capacity. Refer to Pin assignment section for more detail.

Standard Compact Housing Dimensions



Dimensions conform to CompactFlash Association specifications.

Interface Connector Characteristics

Category	Item	Standard
Electrical Performance	Contact Resistance	50 milliohms Maximum
	Current Rating	0.5 Amps. per contact
	Insulation Resistance	100 MegaOhms Minimum
Mechanical Performance	Connector Mating Force	28.8 N Maximum
	Connector Unmating Force	4.9 N Minimum, 28.8 N Maximum
	Insertion/Removal Cycles	5000 mating cycles

MEMORY BUS OPERATIONS

Operation	/CE2	/CE1	/WE	/OE	D[15:8]	D[7:0]
READ						
Standby	H	H	X	X	High-Z	High-Z
Output Disable	L	L	H	H	High-Z	High-Z
Low Byte Access	H	L	H	L	High-Z	Low Data Out
High Byte	L	H	H	L	High-Data Out	High-Z
Word Access	L	L	H	L	High Data Out	Low Data Out
WRITE						
Standby	H	H	X	X	High-Z	High-Z
Low Byte Access	H	L	L	H	High-Z	Low Data In
High Byte	L	H	L	H	High Data In	High-Z
Word Access	L	L	L	H	High Data In	Low Data In

Legend:

$H = V_{IH}$

$L = V_{IL}$

$X = Don't\ Care$

$/ = Active\ Low$

PIN DESCRIPTIONS

A[24:1]

Input Address

Address A1 through A24 are card address inputs that select a unique location within a range of 16MWords (32 MByte).

D[15:0]

Data Input/Output

Data lines D0 through D15 constitute the 16 bit (2 byte) data bus. D0 through D7 are enabled by /CE1, while D8 through D15 are enabled by /CE2.

/OE

Output Enable

/OE is an active low input signal that controls read accesses from the card. It is used in conjunction with /CE1, /CE2, and the asserted address to read a specific location of memory from the on card FLASH memory array.

/WE

Write Enable

/WE is an active low input signal that controls write accesses to the card. It is used in conjunction with /CE1, /CE2 and the asserted address to write to a specific location of memory of the on card FLASH memory array.

/CD1 and /CD2

Card Detect

/CD1 and /CD2 are output low signals from the card used to indicate that the card is fully inserted. /CD1 and /CD2 will force the Host input detect signals low when the card is fully inserted into the host socket. The Host interface circuitry is required to provide a pull-up resistor to Vcc on each of these input signals.

/CE1

Card Enable Low

/CE1 is an active low input signal that enables the even bank of FLASH ICs. Used in conjunction with the asserted address, /CE1 enables the Low order Data Byte [D7:D0].

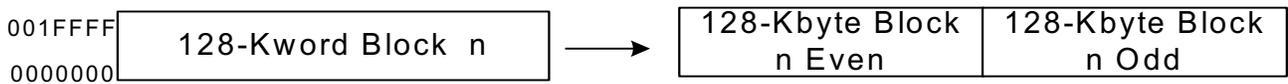
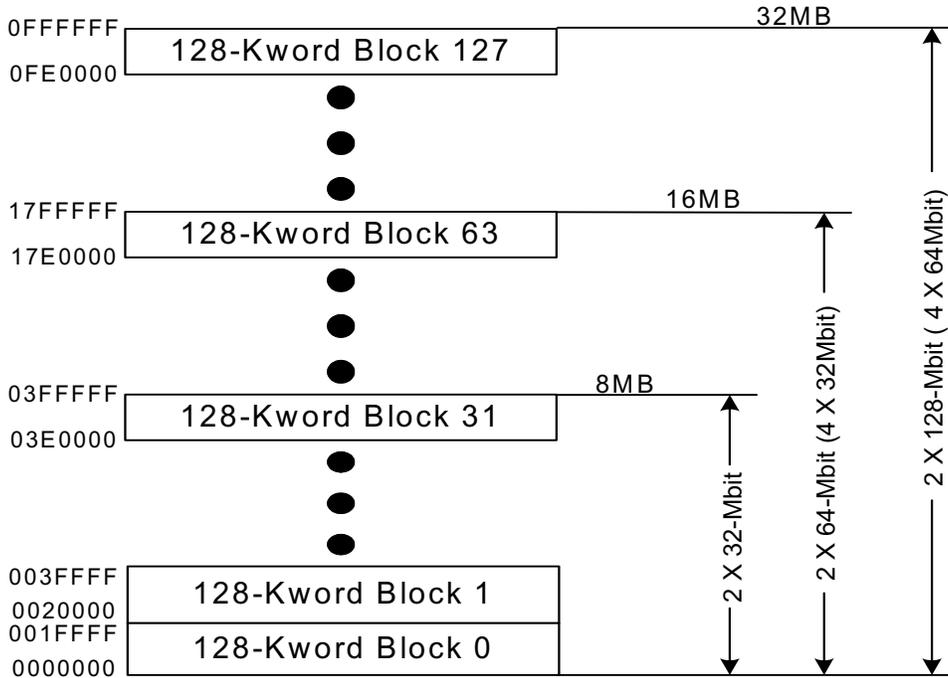
/CE2

Card Enable High

/CE2 is an active low input signal that enables the odd bank of FLASH ICs. Used in conjunction with the asserted address, /CE2 enables the High order Data Byte [D15:D8].

Card Common Memory Map

A [24 – 1]



Command Definitions Table

The Command definitions listed in the table below are for Common Memory operations only.

Command Code Sequence	Bus Cycles	1 st Bus Cycle			2 nd Bus Cycle		
		Bus Opr	Addr	Data	Bus Opr	Addr	Data
Read Array	1	WRT	X	FFh			
Read Identifier Codes	≥2	WRT	X	90h	RD	IA	ID
Read Status Register	2	WRT	X	70h	RD	X	SRD
Clear Status Register	1	WRT	X	50h			
Block Erase	2	WRT	BA	20h	WRT	BA	D0h
Word/Byte Write	2	WRT	WA	40h/10h	WRT	WA	WD
Erase/Write Suspend	1	WRT	X	B0h			
Erase/Write Resume	1	WRT	X	D0h			

Data is latched on the rising edge of /WE (See CARD TIMING CHARACTERISTICS).

For the complete instruction command set refer to the Intel specification for the 28F128J3A.

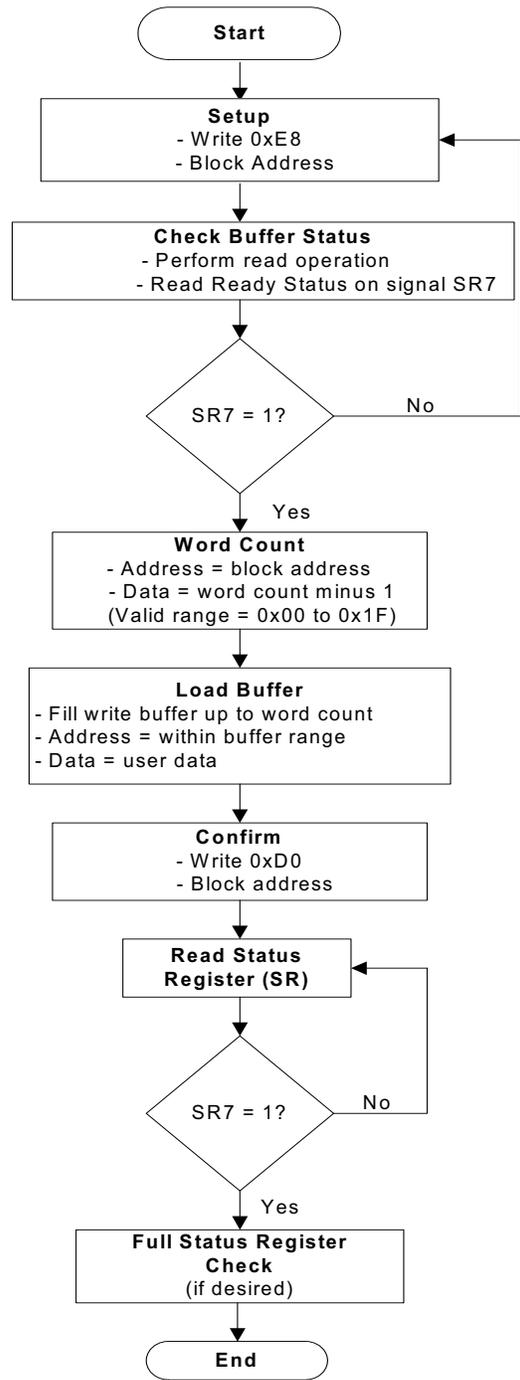
Legend:

RD = Read operation
WRT = Write operation

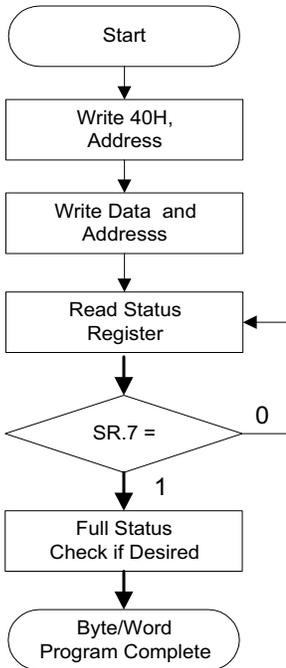
X = Any valid address within a memory device
IA = Identifier Code Address
BA = Address within the block being erased
WA = Address of the memory location to be written

SRD = Data read from status register
WD = Data to be written at location *WA*
ID = Read identifier code data

Write to Buffer Flowchart



Byte/Word Program Flowchart:



Bus Operation	Command	Comments
Write	Setup Byte/Word Program	Data = 40H Addr = Location to Be Programmed
Write	Byte/Word Program	Data = Data to Be Programmed Addr = Location to Be Programmed
Read (note 1)		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

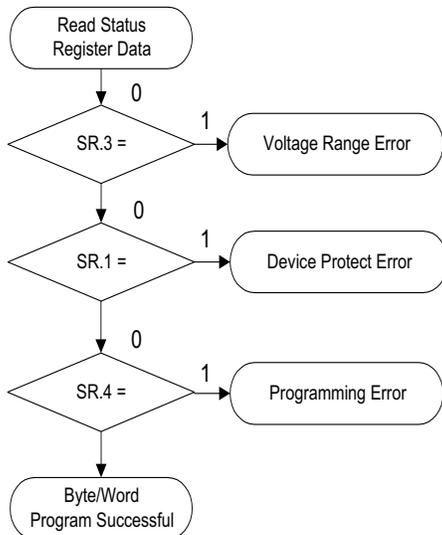
Note: 1

Toggleing OE# (low to high to low) updates the status register. This can be done in place of issuing the Read Status Register command. Repeat for subsequent programming operations.

SR full status check can be done after each program operation, or after a sequence of programming operations.

Write FFH after the last program operation to place device in read array mode.

Full Status Check Procedure



Bus Operation	Comments
Standby	Check SR.3 1 = Programming to Voltage Error Detect
Standby	Check SR.1 1 = Device Protect Detect RP# = VIH, Block Lock-Bit Is Set Only required for systems implementing lock-bit Configuration.
Standby	Check SR.4 1 = Programming Error

Note:

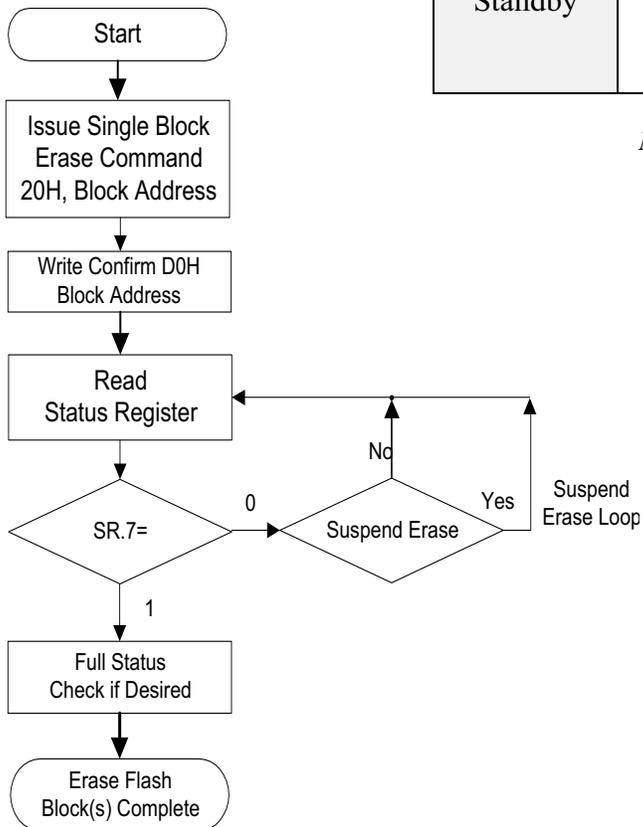
Toggleing OE# (low to high to low) updates the status register. This can be done in place of issuing the Read Status Register command. Repeat for subsequent programming operations.

SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in case where multiple locations are programmed before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

Erase Flowchart:

Bus Operation	Command	Comments
Write	Erase Block	Data = 20H Addr = Block Address
Write <i>(note 1)</i>	Erase Confirm	Data = D0H Addr = Block Address
Read		Status register data With the device enabled, OE# low updates SR Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy



Note: 1

The Erase Confirm byte must follow Erase Setup. This device does not support erase queuing. Please see Application note AP-646 (Intel) for software erase queuing compatibility

Full status check can be done after all erase and write sequences complete. Write FFh after the last operation to reset the device to read array mode.

Card Configuration

Each card is comprised of an array of individual StrataFlash memory devices. Even and odd data bytes of information are stored in separate memory devices. The even byte is the low order byte and the odd byte is the high order byte.

The card data bus operates in word wide mode of operation. A group of two memory devices, one device specifically for the Even bytes and one specifically for the Odd bytes, constitutes a “device pair”. A “device pair” is used to store words of information. Even and Odd bytes can be enabled separately (see memory Bus operations)

Following versions of this card are available in different memory capacities;

- An 8 MByte card, composed of two Intel 28F320J3 4 MByte devices.
- A 16 MByte card, composed of two Intel 28F640J3 8 MByte devices. (or four Intel 28F3200J3 4Mbyte devices)
- A 32 MByte card, composed of two Intel 28F128J3 16 MByte devices. (or four Intel 28F6400J3 8Mbyte devices)

Memory Component Characteristics

Device	Manufacturer	Hex Data	
		Manufacturer Code	Device Code
28F320J3	Intel	89H	16H
28F640J3	Intel	89H	17H
28F128J3	Intel	89H	18H

Write Endurance	100,000 write/erase cycles Minimum per Block
Block Architecture	128(28F128J3), 64(28F640J3), or 32(28F320J3) symmetrical Blocks
Block Size	128 KBytes Erase Block size
Voltage Supply	2.7V – 3.6V for read and write operations

These Intel memory components include Erase and Program routines embedded directly on the devices themselves. These routines can simplify the Host control requirements. The component manufacturer and device ID codes may be read directly from each memory device by writing the appropriate command sequence codes to a device. Devices default to read array mode on power up, to prevent inadvertent writes.

CARD TIMING CHARACTERISTICS

AC Read Characteristics

V_{CC} = 2.7 V-3.6V

#	Sym	Parameter	Density	-75		Unit	Notes
				Min	Max		
R1	t _{AVAV}	Read/Write Cycle Time	32Mbit	75		ns	1
			64Mbit	75			1
			128Mbit	75			1
R2	t _{AVQV}	Address to Output Delay	32Mbit		75	ns	
			64Mbit		75		
			128Mbit		75		
R3	t _{ELQV}	CE _x to Output Delay	32Mbit		75	ns	1
			64Mbit		75		
			128Mbit		75		
R4	t _{GLQV}	OE# to Non-Array Output Delay			25	ns	1,2
R5	t _{PHQV}	RP# High to Output Delay	32Mbit		150	ns	1
			64Mbit		180		
			128Mbit		210		
R6	t _{ELQX}	CE _x to Output in Low Z	All	0		ns	1
R7	t _{GLQX}	OE# to Output in Low Z		0		ns	1
R8	t _{EHQZ}	CE _x High to Output in High Z			25	ns	1
R9	t _{GHQZ}	OE# High to Output in High Z			15	ns	1
R10	t _{OH}	Output Hold from Address, CE _x , or OE# Change, Whichever Occurs First		0		ns	1
R11	t _{ELFL} / t _{ELFH}	CE _x Low to BYTE# High or Low			10	ns	1
R12	t _{FLQV} / t _{FHQV}	BYTE# to Output Delay			1	μs	1
R13	t _{FLQZ}	BYTE# to Output in High Z			1	μs	1
R14	t _{EHEL}	CE _x High to CE _x Low		0		ns	1

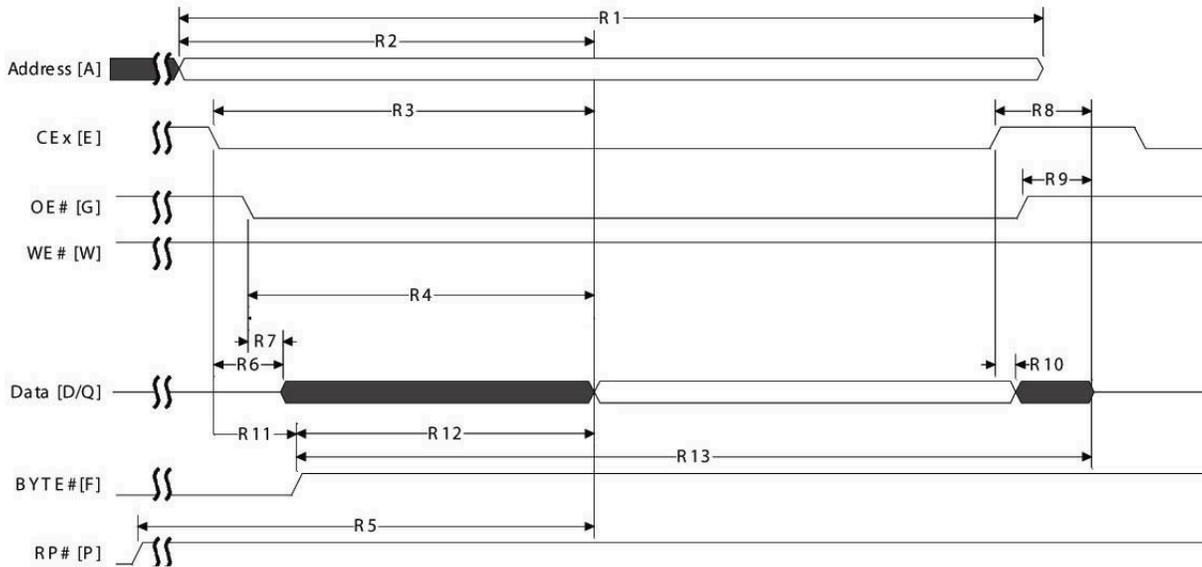
Notes:

CE_x low is defined as the first edge of CE0, CE1, or CE2 that enables the device. CE_x high is defined at the first edge of CE0, CE1, or CE2 that disables the device.

1. OE# may be delayed up to t_{ELQV}:t_{GLQV} after the first edge of CE0, CE1, or CE2 that enables the device.
2. Sample, not 100% tested

Memory Read Timing Diagram

Read Cycle Timing (/WE = V_{IH})



NOTES:

1. CE_x low is defined as the last edge of CE₀, CE₁, or CE₂ that enables the device. CE_x high is defined at the first edge of CE₀, CE₁, or CE₂ that disables the device.

CARD TIMING CHARACTERISTICS (CONTINUED)

AC Write / Erase Characteristics

Program Cycle Timing (/OE = V _{IH} , V _{CC} = 2.7V-3.6V)							
#	Symbol	Parameter	Density	Valid for All Speeds		Unit	Notes
				Min	Max		
W1	t _{PHWL} (t _{PHL})	RP# High Recovery to WE# (CE _x) Going Low	32Mbit	150		ns	1,2,3
			64Mbit	180			
			128Mbit	210			
W2	t _{ELWL} (t _{WLEL})	CE _x (WE#) Low to WE# (CE _x) Going Low	All	0		ns	1,2,4
W3	t _{WP}	Write Pulse Width		60			1,2,4
W4	t _{DVWH} (t _{DVEH})	Data Setup to WE# (CE _x) Going High		50			1,2
W5	t _{AVWH} (t _{AVEH})	Address Setup to WE# (CE _x) Going High		55			1,2
W6	t _{WHEH} (t _{EHWH})	CE _x (WE#) Hold from WE# (CE _x) High		0			1,2
W7	t _{WHDH} (t _{EHDX})	Data Hold from WE# (CE _x) High		0			1,2
W8	t _{WHAX} (t _{EHAX})	Address Hold from WE# (CE _x) High		0			1,2
W9	t _{WPH}	Write Pulse Width High		30			1,2,5
W12	t _{WHGL} (t _{EHGL})	Write Recovery before Read		35			1,2,6
W15	t _{QVVL}	V _{PEN} Hold from Valid SRD, STS Going High		0			1,2,3,7

NOTES:

CE_x low is defined as the first edge of CE₀, CE₁, or CE₂ that enables the device. CE_x high is defined at the first edge of CE₀, CE₁, or CE₂ that disables the device.

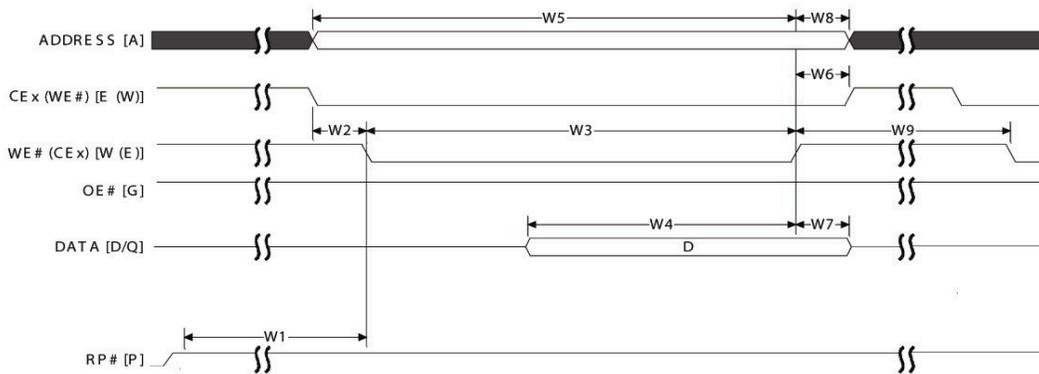
1. Read timing characteristics during block erase, program, and lock-bit configuration operations are the same as during read-only operations.
2. A write operation can be initiated and terminated with either CE_x or WE#.
3. Sampled, not 100% tested.
4. Write pulse width (t_{WP}) is defined from CE_x or WE# going low (whichever goes low last) to CE_x or WE# going high (whichever goes high first). Hence, t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}.
5. Write pulse width high (t_{WPH}) is defined from CE_x or WE# going high (whichever goes high first) to CE_x or WE# going low (whichever goes low first). Hence, t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}.
6. For array access, t_{AVQV} is required in addition to t_{WHGL} for any accesses after a write.
7. STS timings are based on STS configured in its RY/BY# default mode.

CARD TIMING CHARACTERISTICS (CONTINUED)

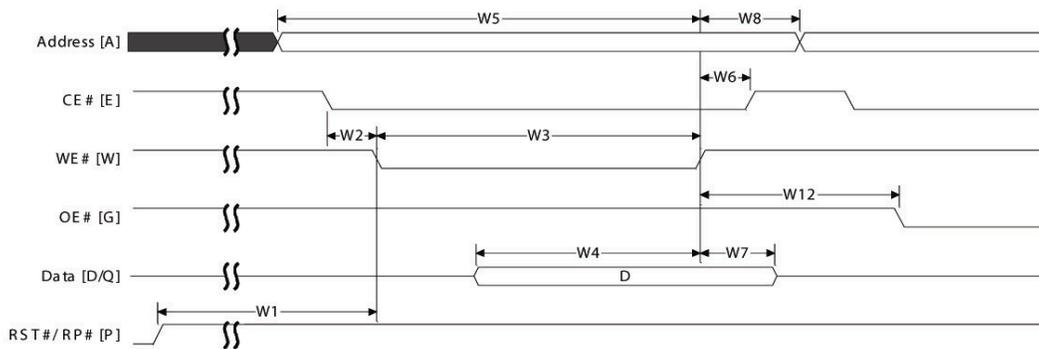
Memory Write Timing Diagram

Write /Erase Cycle Timing (/OE = V_{IH})

Asynchronous Write Waveform



Asynchronous Write to Read Waveform



CARD DC CHARACTERISTICS

Absolute Maximum Ratings :

Storage Temperature	-55°C to +125°C
Operating Temperature with Power Applied	-0°C to +70°C
V _{CC} Supply Voltage	2.7V to 3.6V
Voltage on any pin	-2.0V to 5.0V

Cards are not guaranteed to function at Absolute Maximum Ratings and are not intended to be exposed to these conditions for extended periods of time. Long term exposure may damage these cards or adversely effect the card reliability.

DC Characteristics:

Power Supply Voltage V_{CC} = 2.7V – 3.6V, CMOS Compatible

Symbol	Parameter	Condition	Typ	Max	Units
I _{CCS}	V _{CC} Standby Current (Note 1)	V _{CC} = V _{CC} Max, /CE1, /CE2 = V _{CC}	50	120	μA
I _{CCR}	V _{CC} Active Read Current (Note 2)	StrataFlash Device Enabled; Byte Mode	40	55	mA
I _{CCW}	V _{CC} Program/Erase Current (Note 3)	/CE1, /CE2 = V _{IL} , /OE = V _{IL} /WE = V _{IH}	35	70	mA

Notes:

1. I_{CCS} values are per active memory component of memory.
2. I_{CCR} values are per active memory component of memory. I_{CCR} currents include both DC operating current and the frequency dependent components (at 6MHz). The frequency component typically is less than 1mA/MHz, with /OE at V_{IH}.
3. I_{CCW} values are per active memory component of memory. I_{CCW} is active while the Embedded Program or Erase Algorithm is in progress.

Power Supply Voltage V_{CC} = 2.7V – 3.6V, CMOS Compatible

Symbol	Parameter	Condition	Min	Max	Units
V _{IL}	Input Low Voltage		- 0.5	0.8	V
V _{IH}	Input High Voltage		2.0	V _{CC} + 0.5	V
V _{OL}	Output Low Voltage	I _{OL} = 2 mA, V _{CC} = V _{CC} Min		0.4	V
V _{OH}	Output High Voltage	I _{out} = -2.5mA, V _{CC} = V _{CC} Min	0.85 × V _{CC}		V

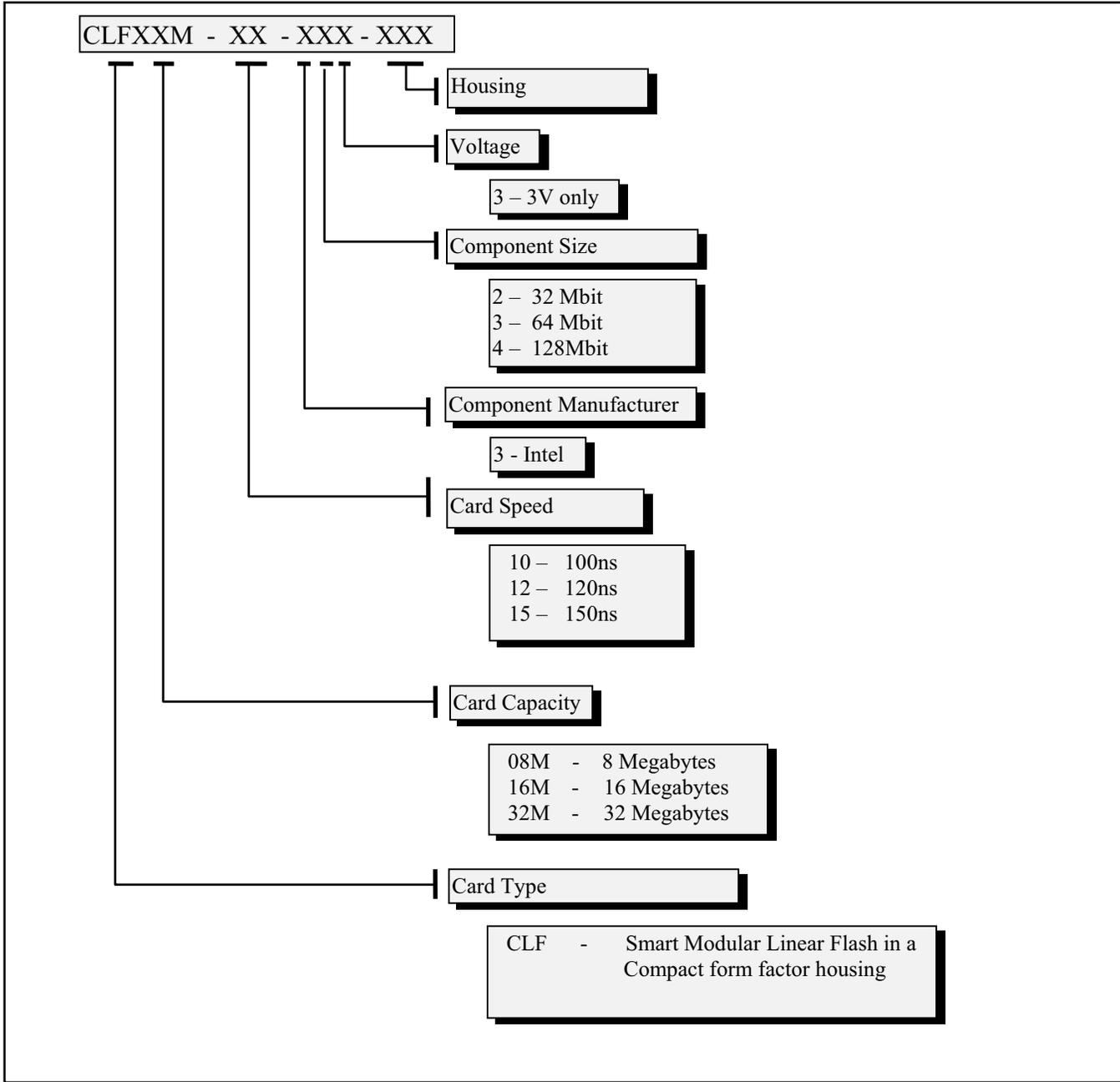
CARD AND PAD CAPACITANCE (Note 1,2)

Symbol	Parameter	Typical	Max	Units
C _{input}	Card Input Capacitance	50	100	pF
C _{I/O}	Card I/O Capacitance	50	100	pF

Notes:

1. Value is for four memory components installed on PCB.
2. Estimated Values (non-testable).

PART NUMBER INFORMATION



ORDERING INFORMATION

Description	Ordering Part Number	
	RoHS	Non RoHS
CLF08M-10-323-122	PG27032	PM27032
CLF16M-12-333-122	PG27033	PM27033
CLF32M-12-333-122	PG27034	PM27034

Note:

PM = Non RoHS products

PG = RoHS products

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