

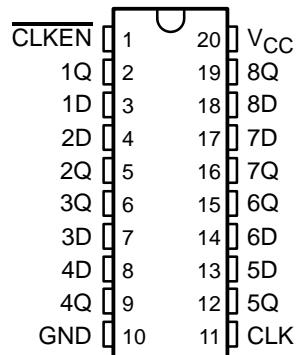
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 12$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Eight Flip-Flops With Single-Rail Outputs
- Clock Enable Latched to Avoid False Clocking
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

### description/ordering information

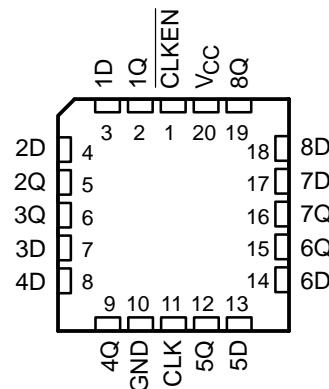
These devices are positive-edge-triggered octal D-type flip-flops with an enable input. The 'HC377 devices are similar to the 'HC273 devices, but feature a latched clock-enable (CLKEN) input instead of a common clear.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse, if CLKEN is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. These devices are designed to prevent false clocking by transitions at CLKEN.

SN54HC377 . . . J OR W PACKAGE  
SN74HC377 . . . DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54HC377 . . . FK PACKAGE  
(TOP VIEW)



### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74HC377N	SN74HC377N
	SOIC – DW	Tube	SN74HC377DW	HC377
		Tape and reel	SN74HC377DWR	
–55°C to 125°C	SOP – NS	Tape and reel	SN74HC377NSR	HC377
	CDIP – J	Tube	SNJ54HC377J	SNJ54HC377J
	CFP – W	Tube	SNJ54HC377W	SNJ54HC377W
	LCCC – FK	Tube	SNJ54HC377FK	SNJ54HC377FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

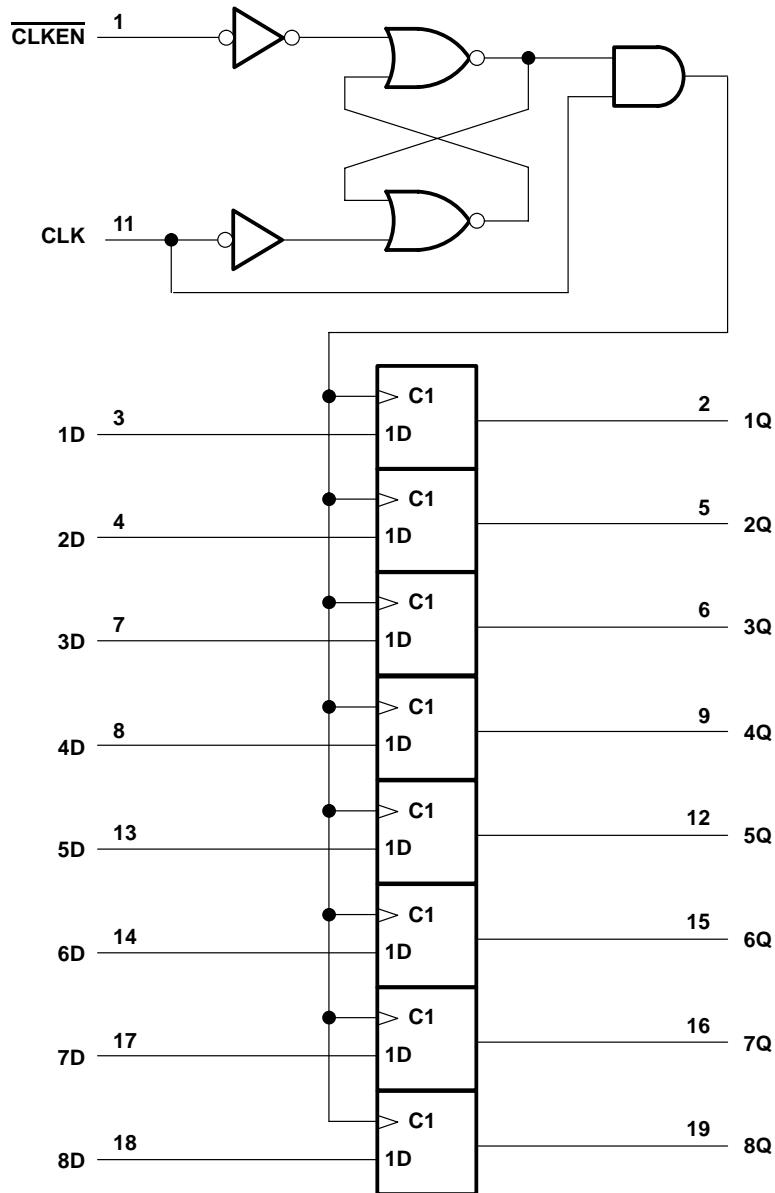
**SN54HC377, SN74HC377  
OCTAL D-TYPE FLIP-FLOPS  
WITH CLOCK ENABLE**

SCLS307B—JANUARY 1996—REVISED JANUARY 2003

**FUNCTION TABLE  
(each flip-flop)**

INPUTS			OUTPUT
CLKEN	CLK	D	Q
H	X	X	$Q_0$
L	↑	H	H
L	↑	L	L
X	L	X	$Q_0$

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

			SN54HC377			SN74HC377			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage			2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage		V <sub>CC</sub> = 2 V	1.5	1.5				V
			V <sub>CC</sub> = 4.5 V	3.15	3.15				
			V <sub>CC</sub> = 6 V	4.2	4.2				
V <sub>IL</sub>	Low-level input voltage		V <sub>CC</sub> = 2 V		0.5			0.5	V
			V <sub>CC</sub> = 4.5 V		1.35			1.35	
			V <sub>CC</sub> = 6 V		1.8			1.8	
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>		V <sub>CC</sub>	V
Δt/Δv	Input transition rise/fall time		V <sub>CC</sub> = 2 V		1000			1000	ns
			V <sub>CC</sub> = 4.5 V		500			500	
			V <sub>CC</sub> = 6 V		400			400	
T <sub>A</sub>	Operating free-air temperature			-55	125	-40	85	°C	

NOTE 3: All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54HC377, SN74HC377  
OCTAL D-TYPE FLIP-FLOPS  
WITH CLOCK ENABLE**

SCLS307B—JANUARY 1996—REVISED JANUARY 2003

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC377	SN74HC377	UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 µA	2 V	1.9	1.998	1.9	1.9	V
			4.5 V	4.4	4.499	4.4	4.4	
			6 V	5.9	5.999	5.9	5.9	
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3	3.7	3.84	
		I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8	5.2	5.34	
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 µA	2 V	0.002	0.1	0.1	0.1	V
			4.5 V	0.001	0.1	0.1	0.1	
			6 V	0.001	0.1	0.1	0.1	
		I <sub>OL</sub> = 4 mA	4.5 V	0.17	0.26	0.4	0.33	
		I <sub>OL</sub> = 5.2 mA	6 V	0.15	0.26	0.4	0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V	±0.1	±100		±1000	±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8	160	80	µA
C <sub>i</sub>		2 V to 6 V		3	10	10	10	pF

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC377	SN74HC377	UNIT
			MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V		5	3	4	MHz
		4.5 V		25	16	20	
		6 V		29	19	23	
t <sub>w</sub>	Pulse duration, CLK high or low	2 V	100		150	125	ns
		4.5 V	20		30	25	
		6 V	17		25	21	
t <sub>su</sub>	Setup time before CLK↑	D	2 V	100	150	125	ns
			4.5 V	20	30	25	
		6 V	17		25	21	
	CLKEN high or low	CLKEN	2 V	100	150	125	
			4.5 V	20	30	25	
		6 V	17		25	21	
t <sub>h</sub>	Hold time after CLK↑	CLKEN inactive or active, data	2 V	5	5	5	ns
			4.5 V	5	5	5	
			6 V	5		5	

**SN54HC377, SN74HC377  
OCTAL D-TYPE FLIP-FLOPS  
WITH CLOCK ENABLE**

SCLS307B– JANUARY 1996 – REVISED JANUARY 2003

switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC377		SN74HC377		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			2 V	5	11		3		4		MHz
			4.5 V	25	54		16		20		
			6 V	29	64		19		23		
$t_{pd}$	CLK	Any	2 V		56	160		240		200	ns
			4.5 V		15	32		48		40	
			6 V		12	27		41		34	
$t_t$		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

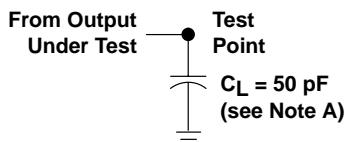
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per flip-flop	No load	30	pF

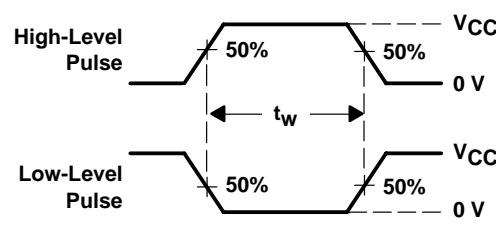
# SN54HC377, SN74HC377 OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

SCLS307B—JANUARY 1996—REVISED JANUARY 2003

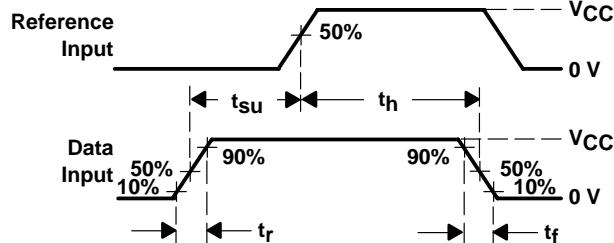
## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

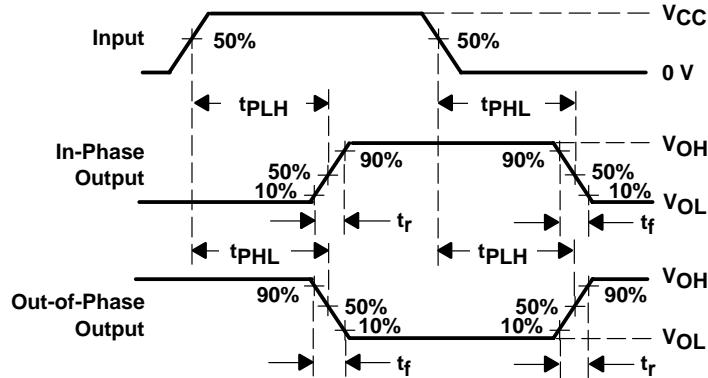


VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS

SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES:

- $C_L$  includes probe and test-fixture capacitance.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
- For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.
- The outputs are measured one at a time with one input transition per measurement.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87807012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87807012A SNJ54HC377FK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-8780701RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8780701RA SNJ54HC377J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN54HC377J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC377J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC377DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC377	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC377DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC377	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC377DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC377	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC377DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC377	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC377DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC377	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC377DWG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC377	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC377N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC377N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC377NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC377N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC377NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC377	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC377NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC377	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HC377NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC377	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54HC377FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87807012A SNJ54HC377FK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54HC377J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8780701RA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54HC377J	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN54HC377, SN74HC377 :

- Catalog: [SN74HC377](#)

- Military: [SN54HC377](#)



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## PACKAGE OPTION ADDENDUM

25-Sep-2013

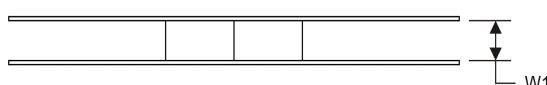
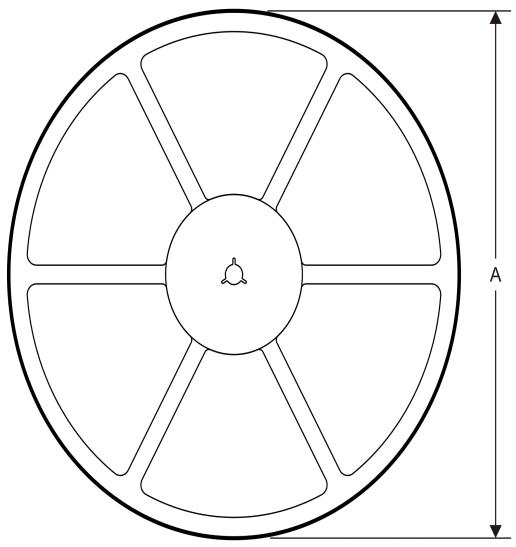
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NOTE: Qualified Version Definitions:

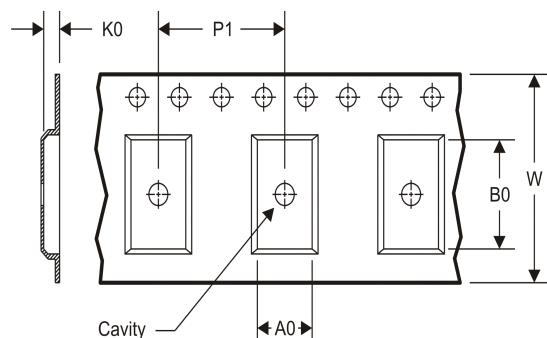
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC377DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74HC377NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

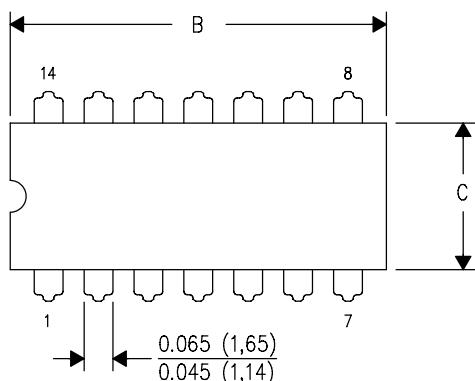
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC377DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC377NSR	SO	NS	20	2000	367.0	367.0	45.0

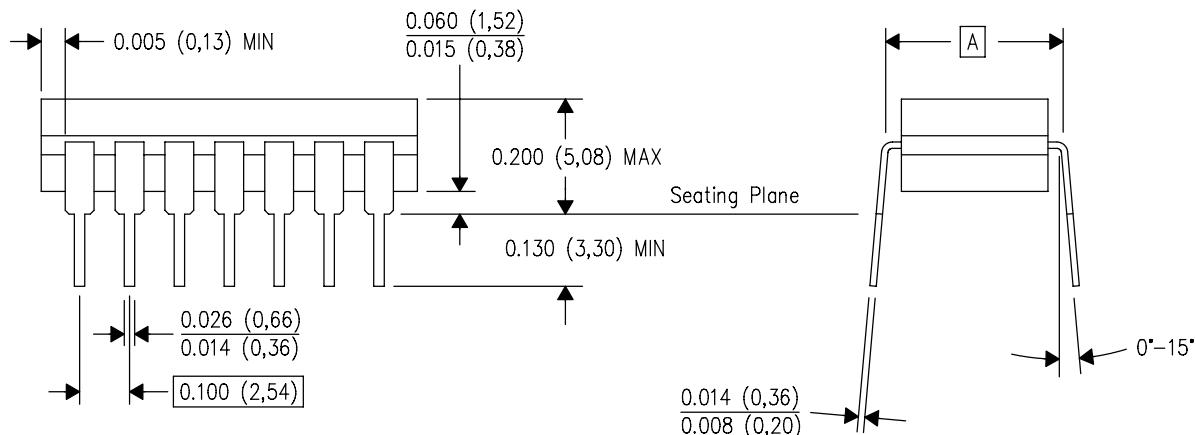
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



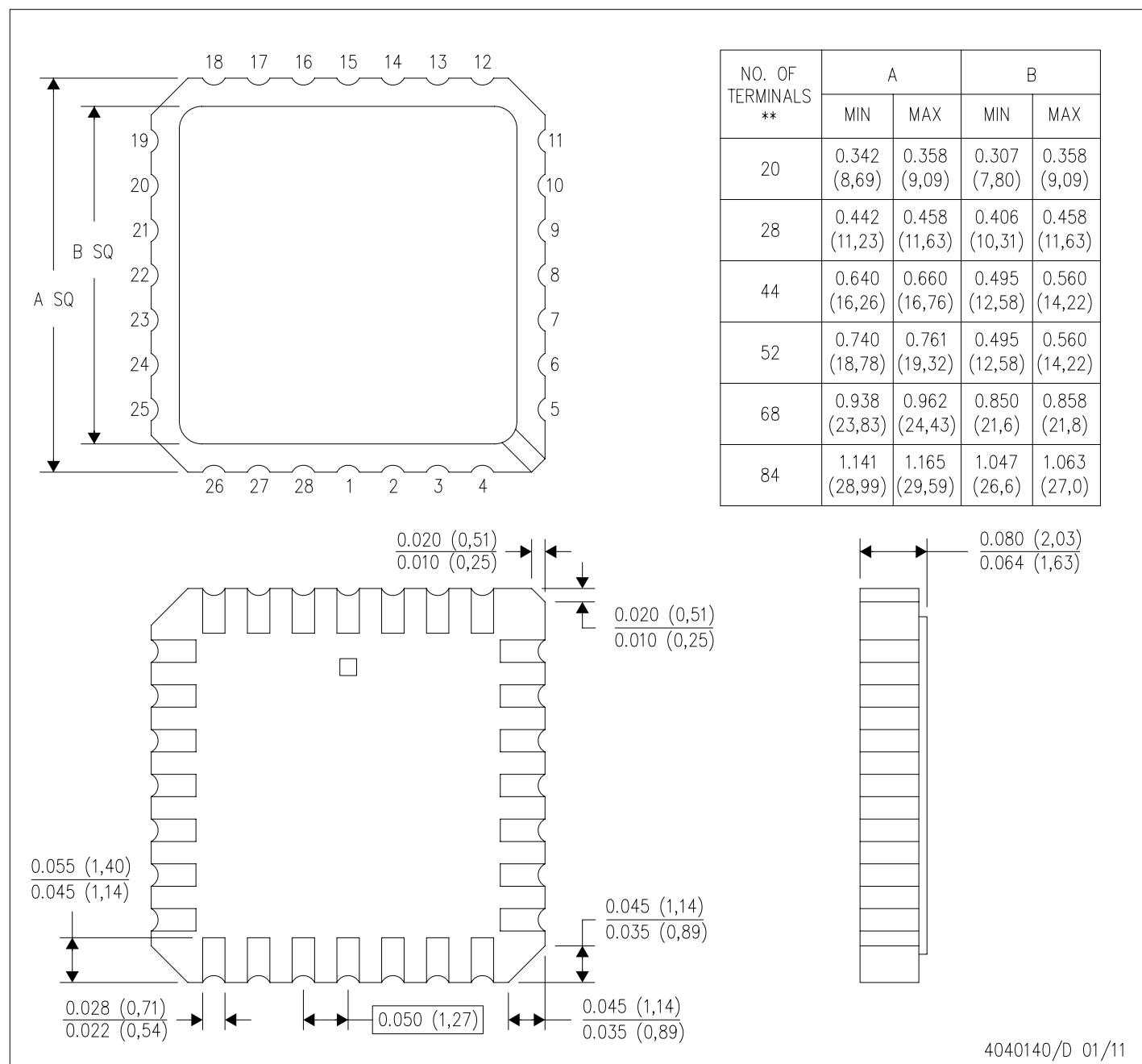
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

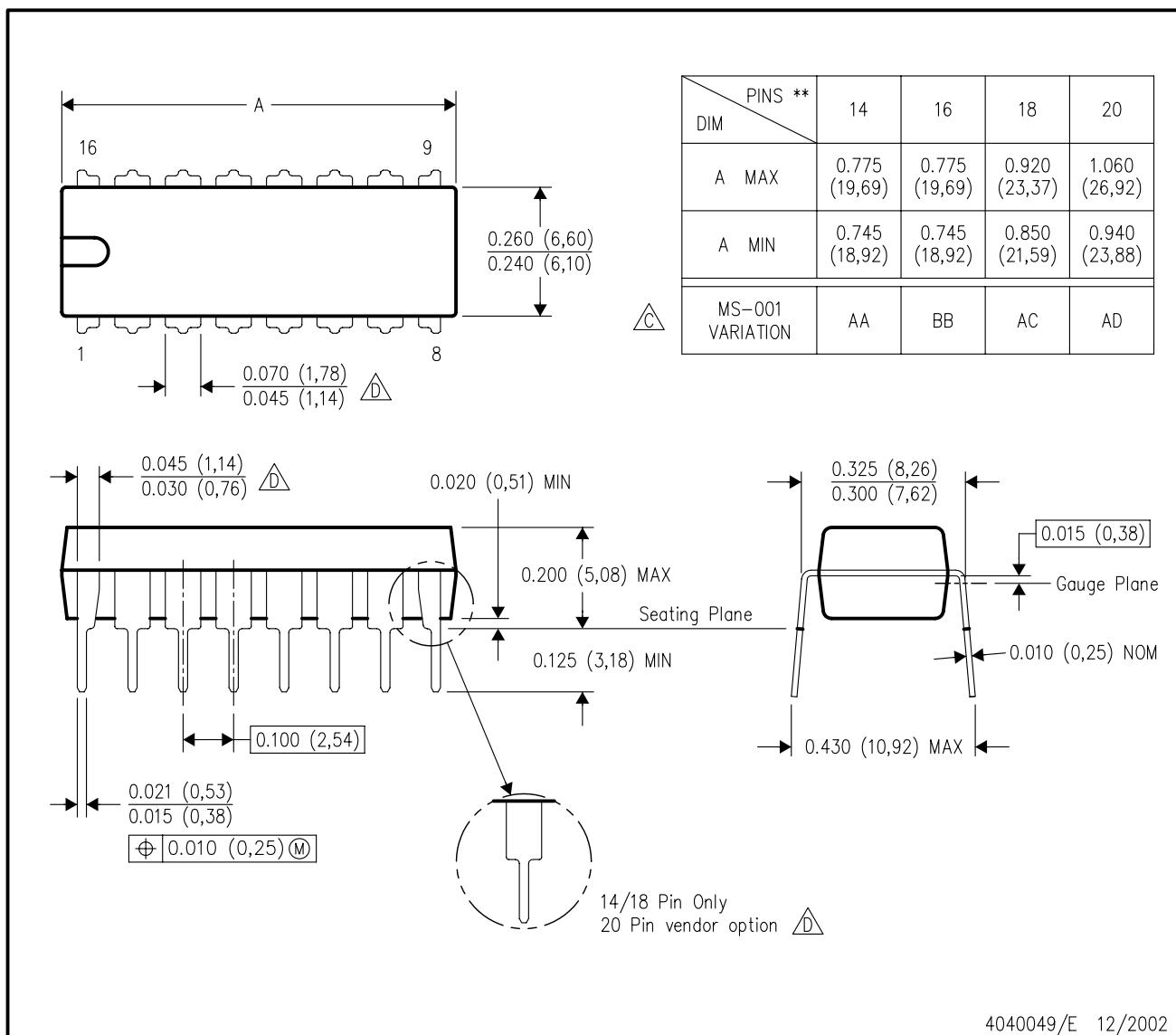
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



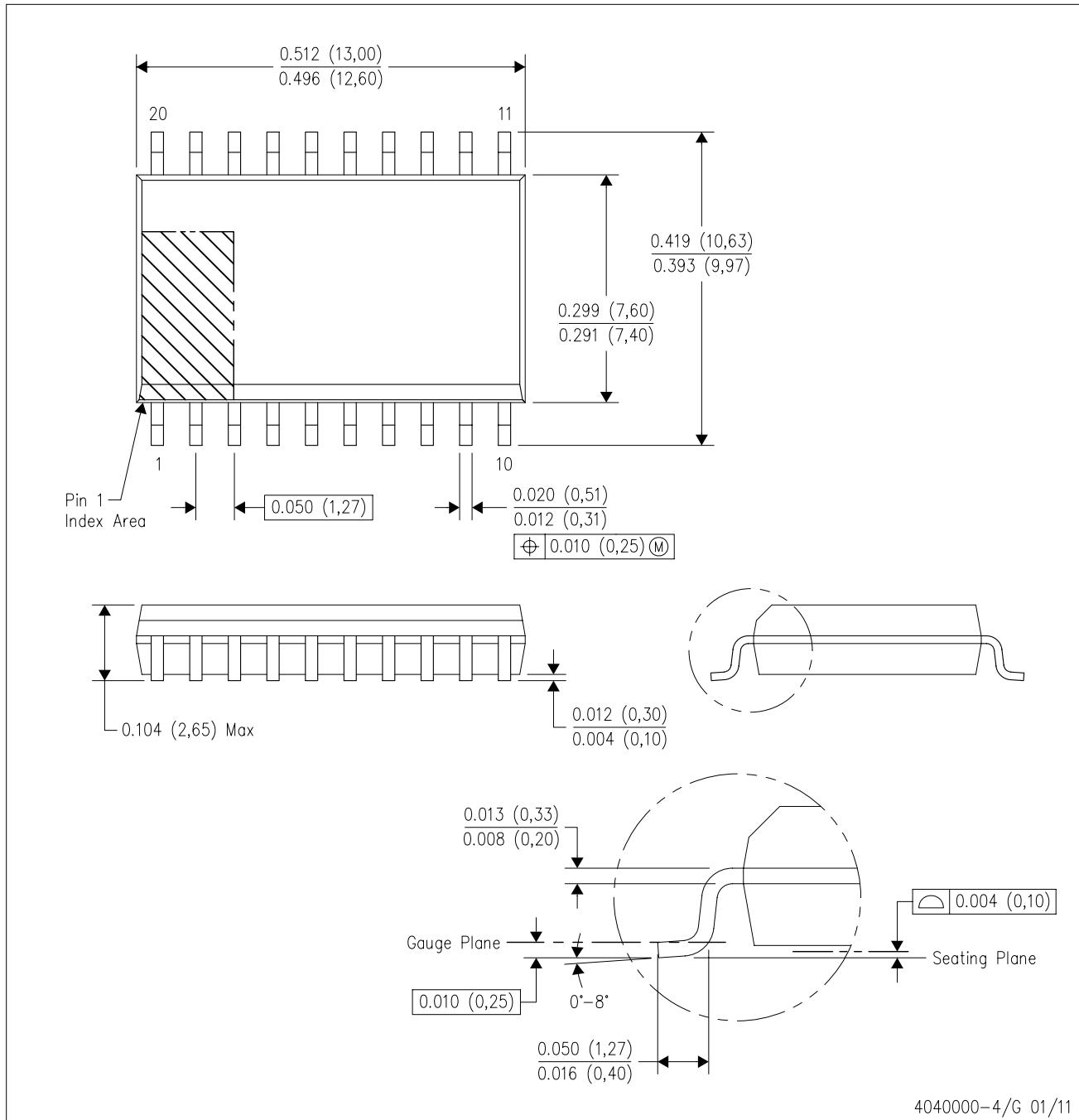
NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

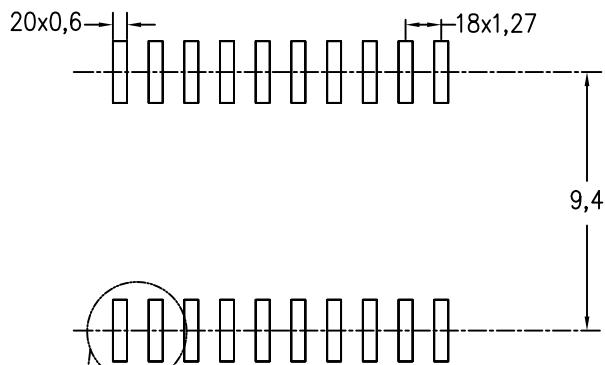
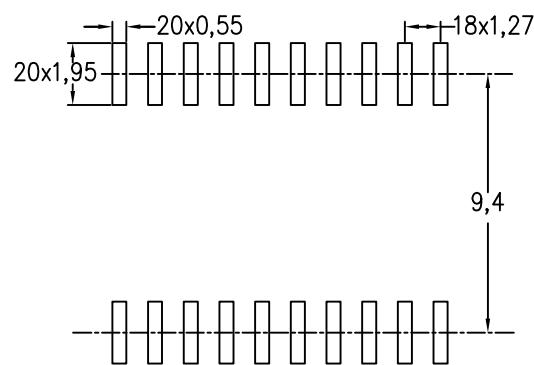


NOTES:

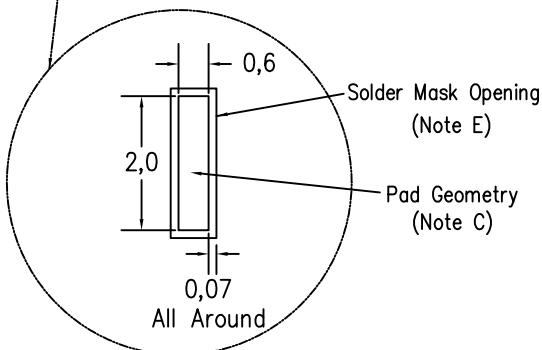
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)

Non Solder Mask Define Pad



4209202-4/F 08/13

NOTES:

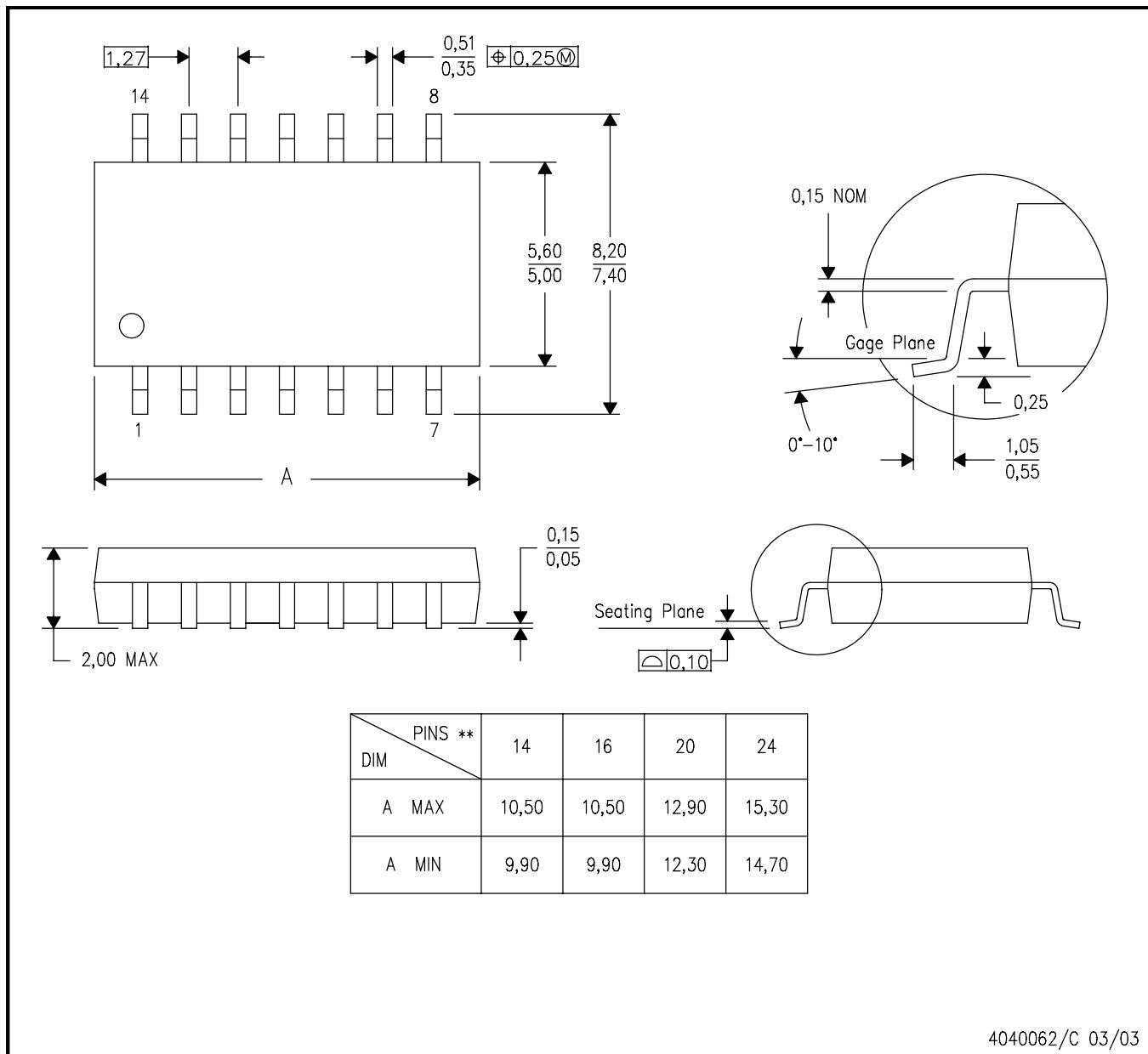
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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