# REDUCED LATENCY DRAM (RLDRAM®)

## MT49H8M32 – 1 Meg x 32 x 8 banks
## MT49H16M16 – 2 Meg x 16 x 8 banks

For the latest data sheet, refer to Micron's Web site: www.micron.com/rldram

## Features

- Organization 8 Meg x 32, 16 Meg x 16 in 8 banks
- Cyclic bank addressing for maximum data bandwidth
- Non multiplexed addresses
- Non interruptible sequential burst of two (2-bit prefetch) and four (4-bit prefetch) DDR
- Up to 600 Mb/sec/pin data rate
- Programmable READ latency (RL) of 5-6
- Data valid signal (DVLD) activated as read data is available
- Data mask signals (DM0/DM1) to mask first and
- second part of write data burst
- IEEE 1149.1 compliant JTAG boundary scan
- 2.5V VEXT, 1.8V VDD, 1.8V VDDQ I/O
- Pseudo-HSTL 1.8V I/O Supply
- Internal auto precharge
- Refresh requirements: 32ms at 95°C case temperature (8K refresh for each bank, 64K refresh command must be issued in total each 32ms)
- 144-pin, 11mm x 18.5mm µBGA package

| Options | Marking |
|---|---|
| • Clock Cycle Timing | |
| 3.3ns (300 MHz) | -33 |
| 4ns (250 MHz) | -4 |
| 5ns (200 MHz) | -5 |
| • Configuration | |
| 8 Meg x 32 (1 Meg x 32 x 8 banks) | MT49H8M32 |
| 16 Meg x 16 (2 Meg x 16 x 8 banks) | MT49H16M16 |
| • Operating temperature range | |
| Commercial: 0° to +95°C | None |
| Industrial: $T_C$ = -40°C to +95°C<br>$T_A$ = -40°C to 85°C) | IT |
| • Package | |
| 144-ball, 11mm x 18.5mm µBGA (Standard) | FM |
| 144-ball, 11mm x 18.5mm µBGA (Lead-Free) | BM[1] |

Notes: 1. Contact factory for availability.

**Figure 1: 144-Ball µBGA**

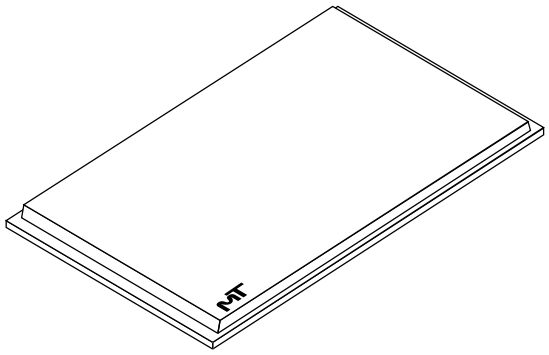



**Table 1: Valid Part Numbers**

| Part Number | Description |
|---|---|
| MT49H8M32FM-xx | 8 Meg x 32 |
| MT49H16M16FM-xx | 16 Meg x 16 |

## General Description

The Micron® 256Mb reduced latency DRAM (RLDRAM®) contains 8 banks x32Mb of memory accessible with 32-bit or 16-bit I/Os in a double data rate (DDR) form at where the data is provided and synchronized with a differential echo clock signal. RLDRAM does not require row/column address multiplexing and is optimized for fast random access and high-speed bandwidth.

RLDRAM is designed for high bandwidth communication data storage—telecommunications, networking, and cache applications, etc.

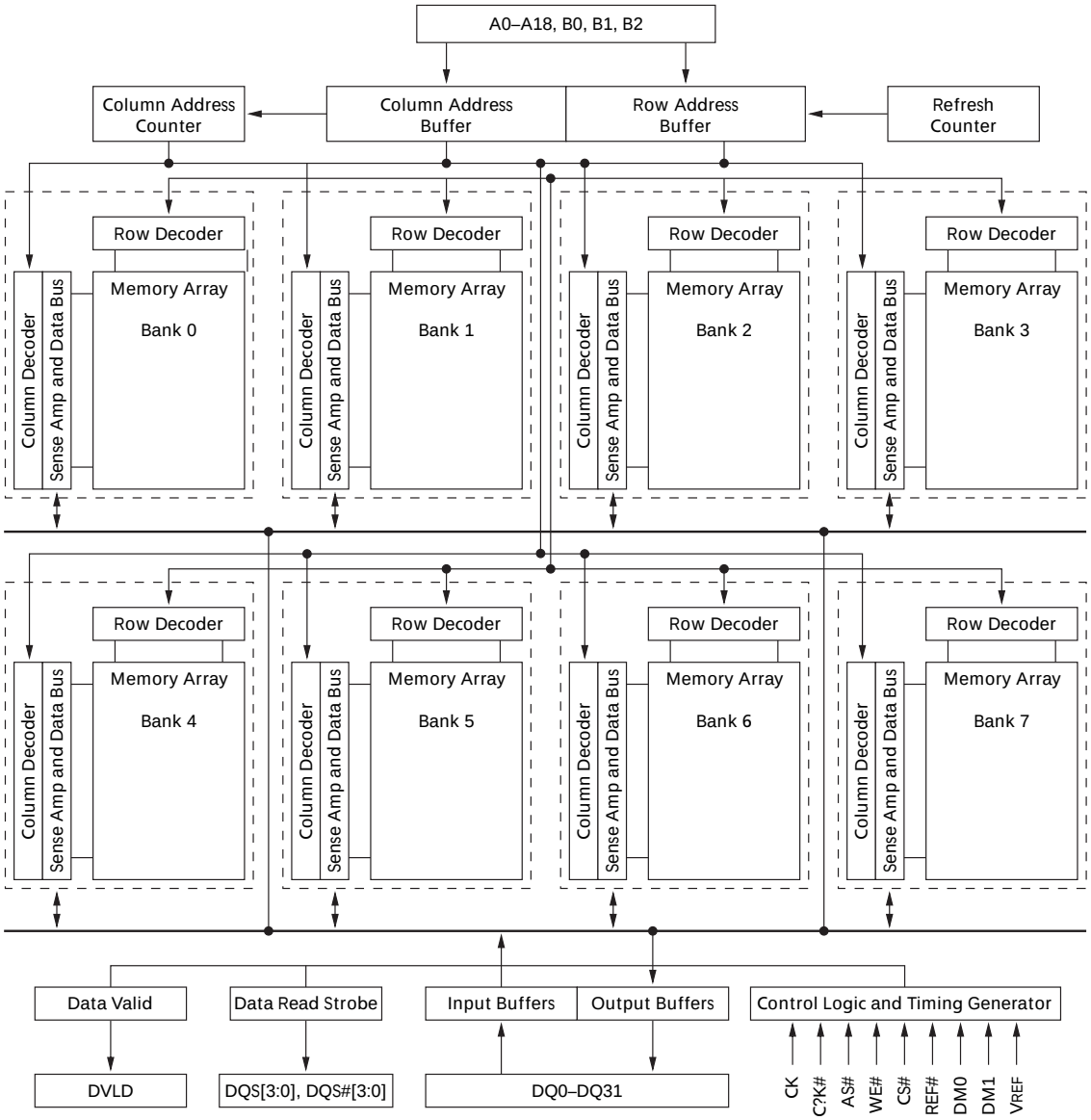
## Table of Contents

## List of Figures

## List of Tables

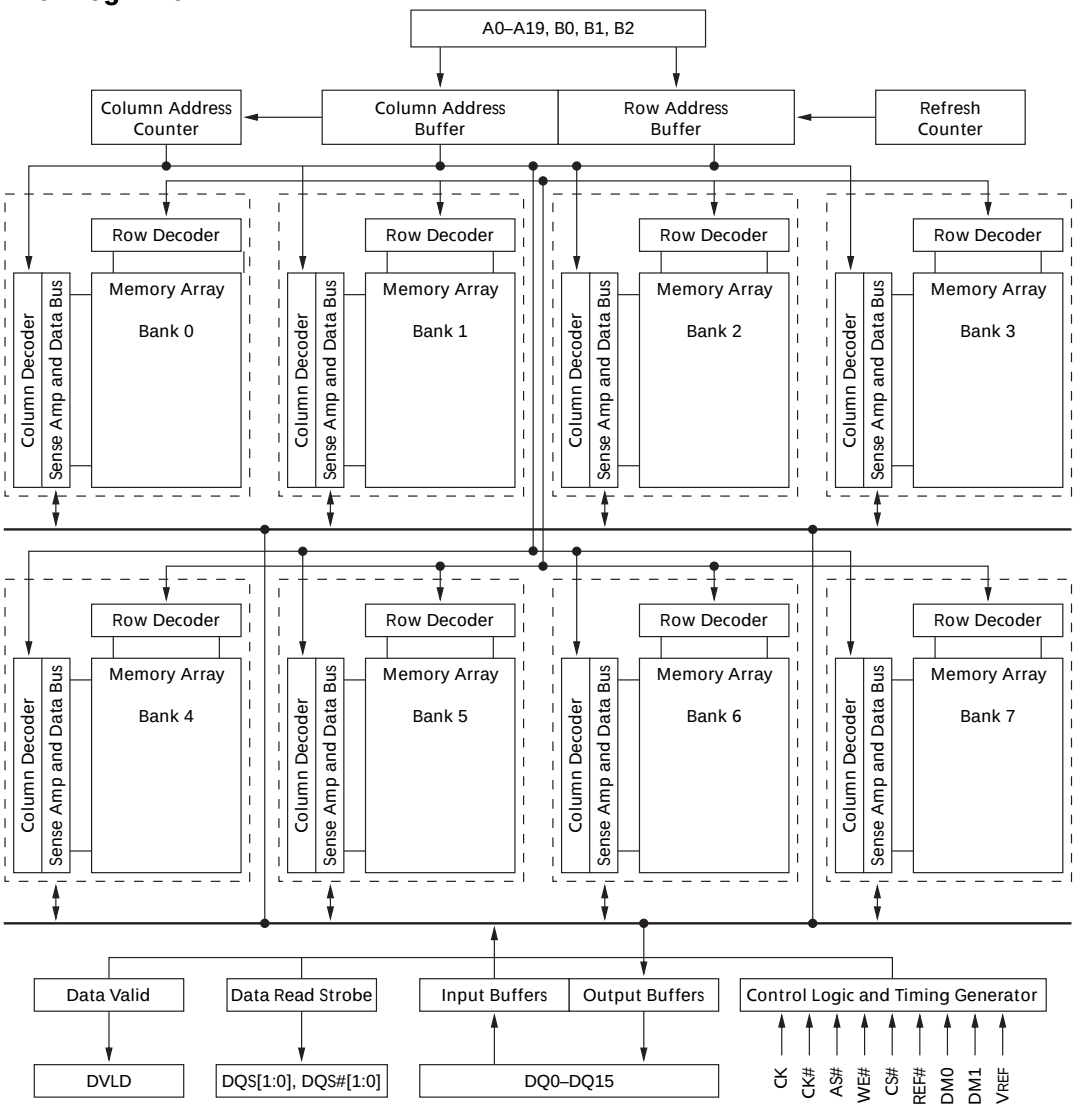
# Functional Block Diagrams

**Figure 2: 8 Meg x 32**




Note: When the BL = 4 setting is used, A18 is a "Don't Care."

**Figure 3: 16 Meg x 16**




Notes: 1. When the BL = 4 setting is used, A19 is a "Don't Care."
2. In the 16 Meg x 16 configuration, only DQS[1:0] and DQS#[1:0] are used.

# Ball Assignment and Description

**Table 2: 8 Meg x 32 Ball Assignment (Top View) 144-Ball µBGA**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | VSS | VEXT | VREF | VSS | | | | | VSS | VEXT | TMS | TCK |
| **B** | VSS | DQ8 | DQ9 | VSSQ | | | | | VSSQ | DQ1 | DQ0 | VSS |
| **C** | VSS | DQ10 | DQ11 | VDDQ | | | | | VDDQ | DQ3 | DQ2 | VSS |
| **D** | VSS | DQS1 | DQS1# | VSSQ | | | | | VSSQ | DQS0# | DQS0 | VSS |
| **E** | VSS | DQ12 | DQ13 | VDDQ | | | | | VDDQ | DQ5 | DQ4 | VSS |
| **F** | DM0 | DQ14 | DQ15 | VSSQ | | | | | VSSQ | DQ7 | DQ6 | DVLD |
| **G** | A5 | A6 | A7 | VDD | | | | | VDD | A2 | A1 | A0 |
| **H** | A8 | A9 | VSS | VSS | | | | | VSS | VSS | A4 | A3 |
| **J** | AS# | B2 | VDD | VDD | | | | | VDD | VDD | B0 | CK |
| **K** | WE# | REF# | VDD | VDD | | | | | VDD | VDD | B1 | CK# |
| **L** | A18 | CS# | VSS | VSS | | | | | VSS | VSS | A14 | A13 |
| **M** | A15 | A16 | A17 | VDD | | | | | VDD | A12 | A11 | A10 |
| **N** | DM1 | DQ22 | DQ23 | VSSQ | | | | | VSSQ | DQ31 | DQ30 | NF[1] |
| **P** | VSS | DQ20 | DQ21 | VDDQ | | | | | VDDQ | DQ29 | DQ28 | VSS |
| **R** | VSS | DQS2 | DQS2# | VSSQ | | | | | VSSQ | DQS3# | DQS3 | VSS |
| **T** | VSS | DQ18 | DQ19 | VDDQ | | | | | VDDQ | DQ27 | DQ26 | VSS |
| **U** | VSS | DQ16 | DQ17 | VSSQ | | | | | VSSQ | DQ25 | DQ24 | VSS |
| **V** | VSS | VEXT | VREF | VSS | | | | | VSS | VEXT | TDO | TDI |

Notes: 1. No Function. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.

**Table 3: 16 Meg x 16 Ball Assignment (Top View) 144-Ball µBGA**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | VSS | VEXT | VREF | VSS | | | | | VSS | VEXT | TMS | TCK |
| **B** | VSS | NF[1] | NF[1] | VSSQ | | | | | VSSQ | DQ1 | DQ0 | VSS |
| **C** | VSS | NF[1] | NF[1] | VDDQ | | | | | VDDQ | DQ3 | DQ2 | VSS |
| **D** | VSS | NF[2] | NF[2] | VSSQ | | | | | VSSQ | DQS0# | DQS0 | VSS |
| **E** | VSS | NF[1] | NF[1] | VDDQ | | | | | VDDQ | DQ5 | DQ4 | VSS |
| **F** | DM0 | NF[1] | NF[1] | VSSQ | | | | | VSSQ | DQ7 | DQ6 | DVLD |
| **G** | A5 | A6 | A7 | VDD | | | | | VDD | A2 | A1 | A0 |
| **H** | A8 | A9 | VSS | VSS | | | | | VSS | VSS | A4 | A3 |
| **J** | AS# | B2 | VDD | VDD | | | | | VDD | VDD | B0 | CK |
| **K** | WE# | REF# | VDD | VDD | | | | | VDD | VDD | B1 | CK# |
| **L** | A19 | CS# | VSS | VSS | | | | | VSS | VSS | A14 | A13 |
| **M** | A15 | A16 | A17 | VDD | | | | | VDD | A12 | A11 | A10 |
| **N** | DM1 | NF[1] | NF[1] | VSSQ | | | | | VSSQ | DQ15 | DQ14 | A18 |
| **P** | VSS | NF[1] | NF[1] | VDDQ | | | | | VDDQ | DQ13 | DQ12 | VSS |
| **R** | VSS | NF[1] | NF[2] | VSSQ | | | | | VSSQ | DQS1# | DQS1 | VSS |
| **T** | VSS | NF[1] | NF[1] | VDDQ | | | | | VDDQ | DQ11 | DQ10 | VSS |
| **U** | VSS | NF[1] | NF[1] | VSSQ | | | | | VSSQ | DQ9 | DQ8 | VSS |
| **V** | VSS | VEXT | VREF | VSS | | | | | VSS | VEXT | TDO | TDI |

Notes: 1. No Function. This signal is internally connected and has parasitic characteristics of an I/O signal. This may optionally be connected to GND.
2. No Function. This signal is internally connected and has parasitic characteristics of an DQS signal. This may optionally be connected to GND.

**Table 4: Ball Descriptions**

| Symbol | Type | Description |
|---|---|---|
| CK, CK# | Input | Input clock: CK and CK# are differential clock inputs. Addresses and commands are latched on the rising edge of CK, input data is latched on both edges of CK. CK# is ideally 180 degrees out of phase with CK. |
| CS# | Input | Chip select: CS# enables the command decoder when low and disables it when high. When the command decoder is disabled, new commands are ignored, but internal operations continue. |
| AS#, WE#, REF# | Input | Command inputs: Sampled at the positive edge of CK, AS#, WE#, and REF# define (together with CS#) the command to be executed. |
| A[0:19] | Input | Address inputs: A[0:19] define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings. They are sampled at the rising edge of CK. In the x32 configuration, A[19] is not used. Refer to Table 5 on page 9 for burst length considerations. |
| BA[0:2] | Input | Bank address inputs: Select to which internal bank a command is being applied. |
| DQ[0:31] | Input/ Output | Data input/output: The DQ signals form the 32-bit data bus. During READ commands, the data is referenced to both edges of DQS/DQS#. During WRITE commands, the data is sampled at both edges of CK. |
| DQSx, DQSx# | Output | Data read strobes: DQSx and DQSx# are the differential data read strobes. During READs, they are transmitted by the RLDRAM and edge-aligned with data. DQSx# is ideally 180 degrees out of phase with DQSx. DQS0 and DQS0# are aligned with DQ0–DQ7. DQS1 and DQS1# are aligned with DQ8–DQ15. DQS2 and DQS2# are aligned with DQ16–DQ23. DQS3 and DQS3# are aligned with DQ24–DQ31. |
| DVLD | Output | Data valid: The DVLD indicates valid output data. DVLD is edge-aligned with DQSx and DQSx#. |
| DM0, DM1 | Input | Input data mask: DM0 and DM1 are the input mask signal for WRITE data. The first half of the input data burst is masked when DM0 is sampled HIGH along with the WRITE command. The second half of the input data burst is masked when DM1 is sampled HIGH along with the WRITE command. |
| TMS<br>TDI | Input | IEEE 1149.1 test inputs: JEDEC-standard 1.8V I/O levels. These balls may be left as no connect if the JTAG function is not used in the circuit. |
| TCK | Input | IEEE 1149.1 clock input: JEDEC-standard 1.8V I/O levels. This ball must be tied to Vss if the JTAG function is not used in the circuit. |
| TDO | Output | IEEE 1149.1 test output: JEDEC-standard 1.8V I/O level. |
| VREF | Input | Input reference voltage: Nominally VDDQ/2. Provides a reference voltage for the input buffers. |
| VEXT | Supply | Power supply: 2.5V nominal. See Table 19 on page 35 for range. |
| VDD | Supply | Power supply: 1.8V nominal. See Table 19 on page 35 for range. |
| VDDQ | Supply | Power supply: Isolated Output Buffer Supply. Nominally, 1.8V. See Table 19 on page 35 for range. |
| Vss | Supply | Power supply: GND. |
| VssQ | Supply | Power supply: Isolated Output Buffer Supply. GND. |
| NF | – | No function: These balls may be connected to ground. |

# Commands

According to the functional signal description, the following command sequences are possible. All input states or sequences not shown are illegal or reserved. All command and address inputs must meet setup and hold times around the rising edge of CK.

**Table 5: Address Widths at Different Burst Lengths**

| Burst Length | x32 | x16 |
|---|---|---|
| BL = 2 | 18:0 | 19:0 |
| BL = 4 | 17:0 | 18:0 |

**Table 6: Command Table**
Note 1

| Operation | CS# | AS# | WE# | REF# | A[19:0][2, 3] | B[2:0] | DM[1:0] |
|---|---|---|---|---|---|---|---|
| READ cycle | L | L | H | H | VALID | VALID | X |
| WRITE cycle | L | L | L | H | VALID | VALID | VALID |
| NOP: no operation | L | H | H | H | X | X | X |
| DESELECT | H | X | X | X | X | X | X |
| AUTO REFRESH | L | H | H | L | X | VALID | X |
| MRS: mode register set[4] | L | L | L | L | VALID | X | X |

Notes: 1. X represents a "Don't Care"
H represents a logic HIGH
L represents a logic LOW
A represents a valid address
BA represents a valid bank address.
2. In the x32 configuration A19 is not used.
3. See above table; address widths at different burst lengths.
4. Only A(17:0) are used for the MRS command.

**Table 7: Description of Commands**

| Command | Description |
|---|---|
| DESEL/NOP[1] | The NOP command is used to perform a no operation to the RLDRAM, which essentially deselects the chip. Use the NOP command to prevent unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. Output values depend on command history. |
| MRS | The mode register is set via the address inputs A(17:0). See Figure 9 on page 15 for further information. The MRS command can only be issued when all banks are idle and no bursts are in progress. |
| READ | The READ command is used to initiate a burst read access to a bank. The value on the BA(2:0) inputs selects the bank, and the address provided on inputs A(19:0) selects the data location within the bank. |
| WRITE | The WRITE command is used to initiate a burst write access to a bank. The value on the BA(2:0) inputs selects the bank, and the address provided on inputs A(19:0) selects the data location within the bank. Input data appearing on the DQs is written to the memory array subject to the DMx input logic level appearing coincident with the WRITE command. If the DM0 signal is registered LOW, the first half of the burst WRITE data will be written to memory, if registered HIGH, the corresponding data inputs will be ignored (i.e., this part of the data word will not be written). If the DM1 signal is registered LOW, the second half of the burst WRITE data will be written to memory, if registered HIGH, the corresponding data inputs will be ignored (i.e., this part of the data word will not be written). |
| AREF | The AREF is used during normal operation of the RLDRAM to refresh the memory content of a bank. The command is nonpersistent, so it must be issued each time a refresh is required. The value on the BA(2:0) inputs selects the bank. The refresh address is generated by an internal refresh controller, effectively making each address bit a "Don't Care" during the AREF command. The RLDRAM requires 64K cycles at an average periodic interval of 0.49µs [2](MAX). To improve efficiency, eight AREF commands (one for each bank) can be posted to the RLDRAM at periodic intervals of 3.9µs.[3] |

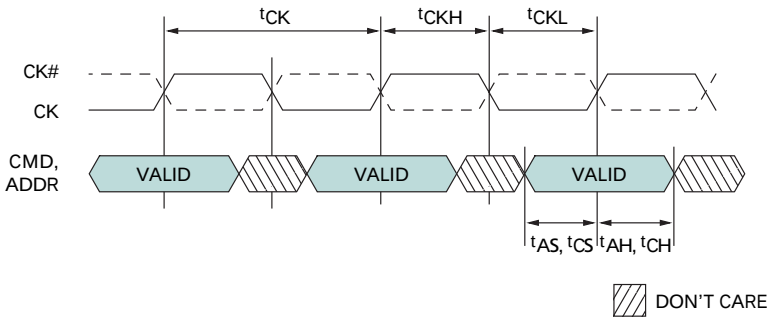
Notes: 1. When the chip is deselected, internal NOP commands are generated and no commands are accepted.
2. Actual refresh is 32ms/8K/8 = 0.488µs.
3. Actual refresh is 32ms/8k = 3.90µs.

**Table 8: AC Electrical Characteristics**
Note 1

| Description | Symbol | -33 | | -4 | | -5 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| **Clock** | | | | | | | | | |
| Clock cycle time | $^{t}$CK | 3.3 | | 4.0 | | 5.0 | | ns | 2 |
| System frequency | $^{f}$CK | | 300 | | 250 | | 200 | MHz | |
| Clock HIGH time | $^{t}$CKH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | $^{t}$CK | |
| Clock LOW time | $^{t}$CKL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | $^{t}$CK | |
| Mode register set cycle time to any command | $^{t}$MRSC | 4 | | 4 | | 4 | | $^{t}$CK | |
| **Setup Times**[3] | | | | | | | | | |
| Address/command and input setup time | $^{t}$AS/$^{t}$CS | 1.0 | | 1.0 | | 1.0 | | ns | |
| Data-in and data mask to DK setup time | $^{t}$DS | 0.5 | | 0.5 | | 0.5 | | ns | |
| **Hold Times** | | | | | | | | | |
| Address/command and input hold time | $^{t}$AH/$^{t}$CH | 1.0 | | 1.0 | | 1.0 | | ns | |
| Data-in and data mask to DK hold time | $^{t}$DH | 0.5 | | 0.5 | | 0.5 | | ns | |
| **Data and Data Strobe** | | | | | | | | | |
| DQS, DQS# HIGH time | $^{t}$DQSH | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $^{t}$CK | |
| DQS, DQS# LOW time | $^{t}$DQSL | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $^{t}$CK | |
| Clock to DQS, DQS# | $^{t}$CKDQS | 2.4 | 3.9 | 2.4 | 3.9 | 2.4 | 3.9 | ns | |
| DQS to output valid | $^{t}$DQSQ | | 0.35 | | 0.35 | | 0.35 | ns | 4 |
| DQS to output High-Z | $^{t}$QSQHZ | | 0.4 | | 0.4 | | 0.4 | ns | |
| DQS to DVLD | $^{t}$QSVLD | -0.4 | 0.4 | -0.4 | 0.4 | -0.4 | 0.4 | ns | 5 |

Notes:
1. All timing parameters are measured relative to the crossing point of CK/CK# and to the crossing point with VREF of the command and address signals.
2. CK/CK# input slew rate must be >1V/ns (>2V/ns if measured differentially).
3. The signal input slew rate must be >1V/ns.
4. Parameter only valid within one DQS/DQ group, e.g., DQS0, DQS0#, and DQ0–DQ7; DQS1, DQS1#, and DQ8–DQ15.
5. The rising and falling edges of DVLD are referenced to falling edges of DQS.

**Figure 4: Clock Command/Address Timings**



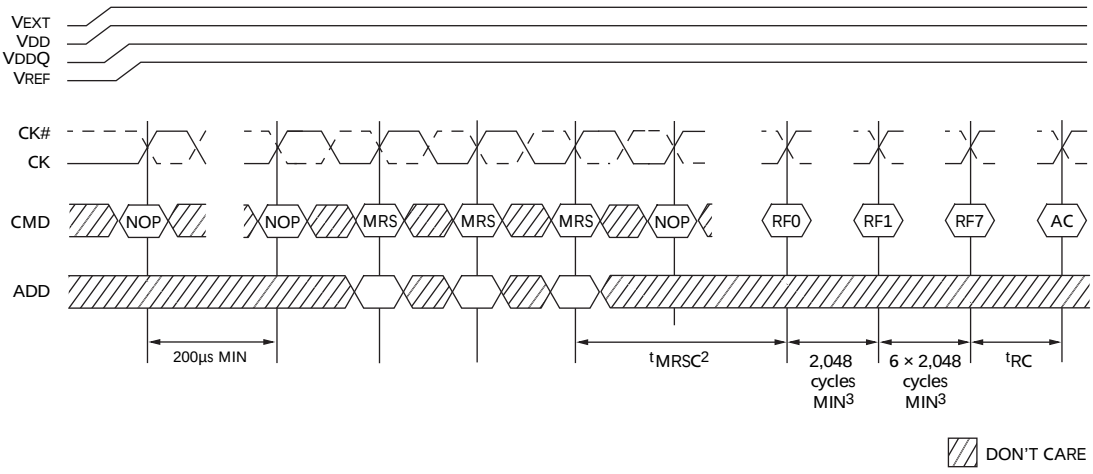
# Initialization

The RLDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operations or permanent damage to the device.

The following sequence is used for Power-Up:

1. Apply power (VEXT, VDD, VDDQ, VREF) and start clock as soon as the supply voltages are stable. Apply VDD and VEXT before or at the same time as VDDQ. Apply VDDQ before or at the same time as VREF. Although there is no timing relation between VEXT and VDD, the chip starts the power-up sequence only after both voltages are at their nominal levels. The pad supply must not be applied before the core supplies. CK/CK# must meet VID(DC) prior to being applied. Maintain all remaining balls in NOP conditions.
2. Maintain stable conditions for 200µs (MIN).
3. Issue three MODE REGISTER Set commands: two dummies plus one valid MRS. It is recommended that the dummy MRS commands are the same value as the desired MRS.
4. $^{t}$MRSC after the valid MRS, issue eight AUTO REFRESH commands, one on each bank and separated by 2,048 cycles. Initial bank refresh order does not matter.
5. After $^{t}$RC, the chip is ready for normal operation.

**Figure 5: Power-Up Sequence**

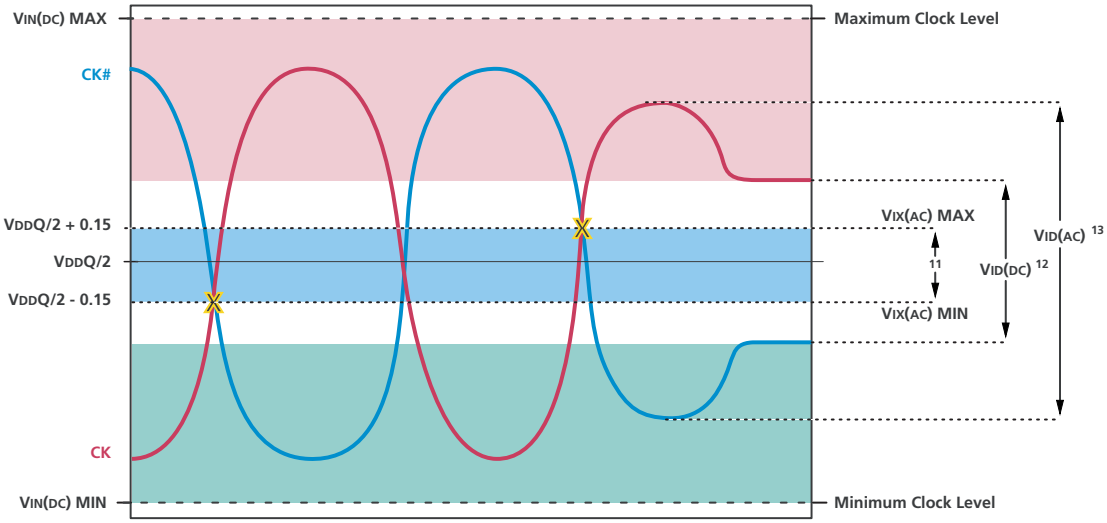



Notes: 1. MRS: MRS command
RFx: REFRESH Bank *x*
AC: any command.
2. During $^{t}$MRSC, NOP command must be given on the rising edge of CK.
3. When the RLDRAM is powered up with the matched impedance mode inactive, the 2,048 cycles between the eight REFRESH commands are not required. These cycles are necessary in order to calibrate the output drivers.

**Table 9: Clock Input Operating Conditions**
Notes 1–8

| Parameter/Condition | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Clock input voltage level; CK and CK# | VIN(DC) | -0.3 | VDDQ + 0.3 | V | |
| Clock input differential voltage; CK and CK# | VID(DC) | 0.3 | VDDQ + 0.6 | V | 9 |
| Clock input differential voltage; CK and CK# | VID(AC) | 0.6 | VDDQ + 0.6 | V | 9 |
| Clock input crossing point voltage; CK and CK# | VIX(AC) | VDDQ/2 - 0.15 | VDDQ/2 + 0.15 | V | 10 |

**Figure 6: Clock Input**

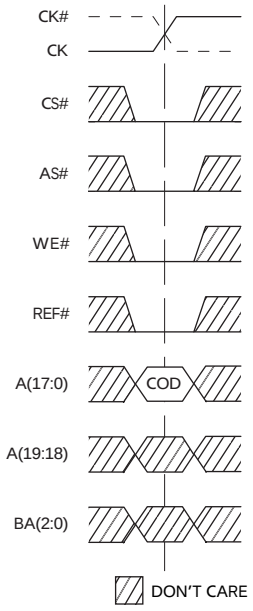



Notes:
1. DQSx and DQSx# have the same requirements as CK and CK#.
2. All voltages referenced to VSS.
3. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
4. Outputs (except for IDD measurements) measured with equivalent load.
5. AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/CK#), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is ≥1V/ns in the range between VIL(AC) and VIH(AC).
6. The AC and DC input level specifications are as defined in the HSTL Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
7. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signals other than CK/CK# is VREF.
8. CK and CK# input slew rate must be ≥1V/ns (≥2V/ns if measured differentially).
9. VID is the magnitude of the difference between the input level on CK and the input level on CK#.
10. The value of VIX is expected to equal VDDQ/2 of the transmitting device and must track variations in the DC level of the same.
11. CK and CK# must cross within this region.
12. CK and CK# must meet at least VID(DC) MIN when static and centered around VDDQ/2.
13. Minimum peak-to-peak swing.

# Mode Register Set Command (MRS)

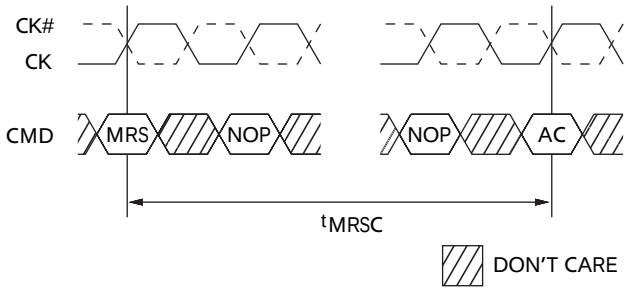
The mode register stores the data for controlling the operating modes of the memory. It programs the RLDRAM configuration, burst length, and I/O options. During a MODE REGISTER SET command, the address inputs A(17:0) are sampled and stored in the mode register. $^{t}$MRSC must be met before any command can be issued to the RLDRAM. The mode register may be set at any time during device operation. However, any pending operations are not guaranteed to successfully complete.

**Figure 7: Mode Register Set**



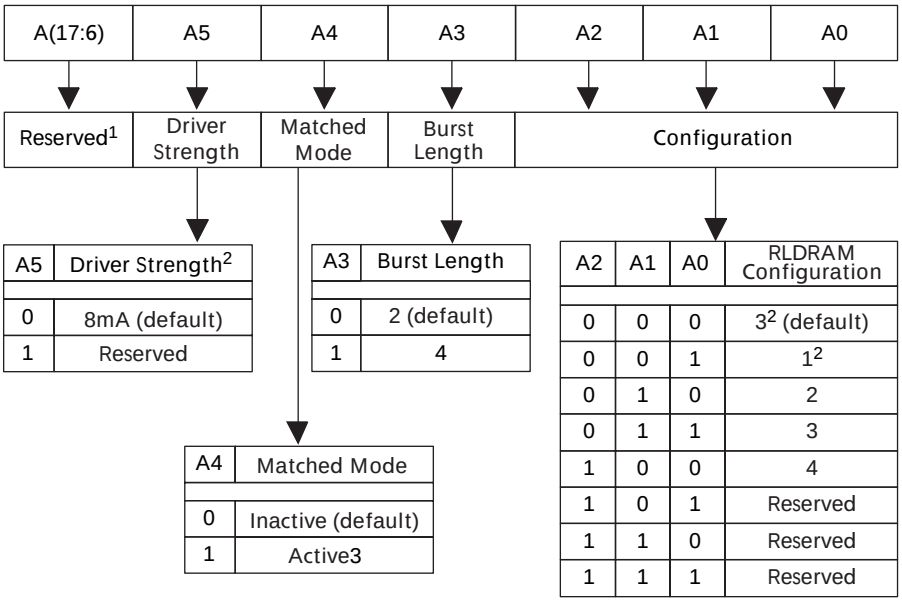

Note: COD: code to be loaded into the register

**Figure 8: Mode Register Set Timing**




Note: MRS: MRS command
AC: any command.

**Figure 9: Mode Register Bit Map**




Notes: 1. Bits A(17:6) *must* be set to zero.
2. HSTL-compliant current specification.
3. Automatic I/O impedance calibration is activated in matched mode.

# Configuration Table

The table below shows the different RLDRAM configurations that can be programmed into the mode register for different operating frequencies. The READ and WRITE latency ($^{t}$RL and $^{t}$WL) values, along with the row cycle times ($^{t}$RC), are shown in clock cycles, as well as in nanoseconds. The shaded areas correspond to configurations that are not allowed.

**Table 10: RLDRAM Configuration Table**

| Frequency | Symbol | Configuration | | | | Units |
|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | |
| | $^{t}$RC | 5 | 6 | 7 | 8 | Cycles |
| | $^{t}$RL | 5 | 5 | 5 | 6 | Cycles |
| | $^{t}$WL (BL = 2) | 2 | 2 | 2 | 3 | Cycles |
| | $^{t}$WL (BL = 4) | 1 | 1 | 1 | 2 | Cycles |
| 300 MHz | $^{t}$RC | | | | 26.7 | ns |
| | $^{t}$RL | | | | 20.0 | ns |
| | $^{t}$WL (BL = 2) | | | | 10.0 | ns |
| | $^{t}$WL (BL = 4) | | | | 6.7 | ns |
| 250 MHz | $^{t}$RC | | | 28.0 | 32.0 | ns |
| | $^{t}$RL | | | 20.0 | 24.0 | ns |
| | $^{t}$WL (BL = 2) | | | 8.0 | 12.0 | ns |
| | $^{t}$WL (BL = 4) | | | 4.0 | 8.0 | ns |
| 200 MHz | $^{t}$RC | 25.0 | 30.0 | 35.0 | 40.0 | ns |
| | $^{t}$RL | 25.0 | 25.0 | 25.0 | 30.0 | ns |
| | $^{t}$WL (BL = 2) | 10.0 | 10.0 | 10.0 | 15.0 | ns |
| | $^{t}$WL (BL = 4) | 5.0 | 5.0 | 5.0 | 10.0 | ns |

# Write Basic Information

Write accesses are initiated with a WRITE command, as shown in the Figure 10. Row and bank addresses are provided together with the WRITE command.

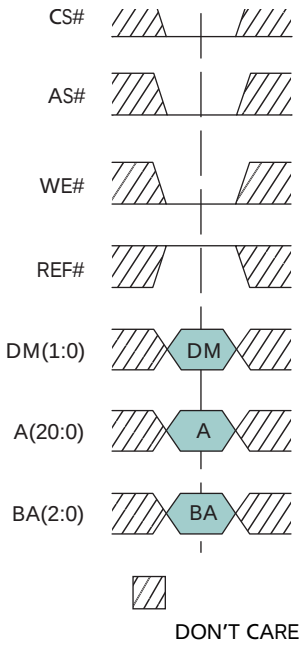
During WRITE commands, data will be registered at both edges of CK according to the programmed burst length (BL). The first valid data will be registered with the first rising CK edge WL cycles after the WRITE command has been issued.

Any WRITE burst may be followed by a subsequent READ command. Figure 16 on page 20 illustrates the timing requirements for a WRITE followed by a READ for burst of four.

Setup and hold times for incoming DQ relative to the CK edges are specified as $^{t}$DS and $^{t}$DH.

The first or second part of the incoming data burst is masked if the corresponding DMx signal is sampled HIGH along with the WRITE command. The setup and hold times for data mask are the same as for address and command.

**Figure 10: WRITE Command**




Note: A: address
BA: bank address
DM: data mask.

**Figure 11: Basic WRITE Burst Timing**

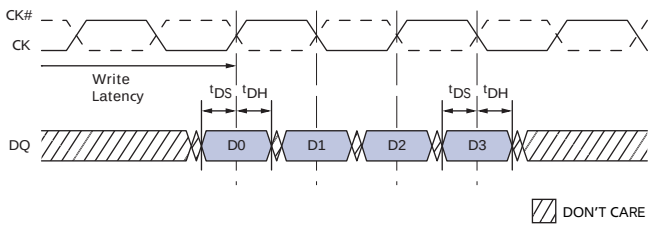


**Table 11: Timing Parameters**

| Symbol | -33 | -4 | -5 | Units |
|---|---|---|---|---|
| | Min/Max | Min/Max | Min/Max | |
| $^{t}$DS | 0.5 | 0.5 | 0.5 | ns |
| $^{t}$DH | 0.5 | 0.5 | 0.5 | ns |

**Figure 12: WRITE Burst Basic Sequence: BL = 2; WL = 3**

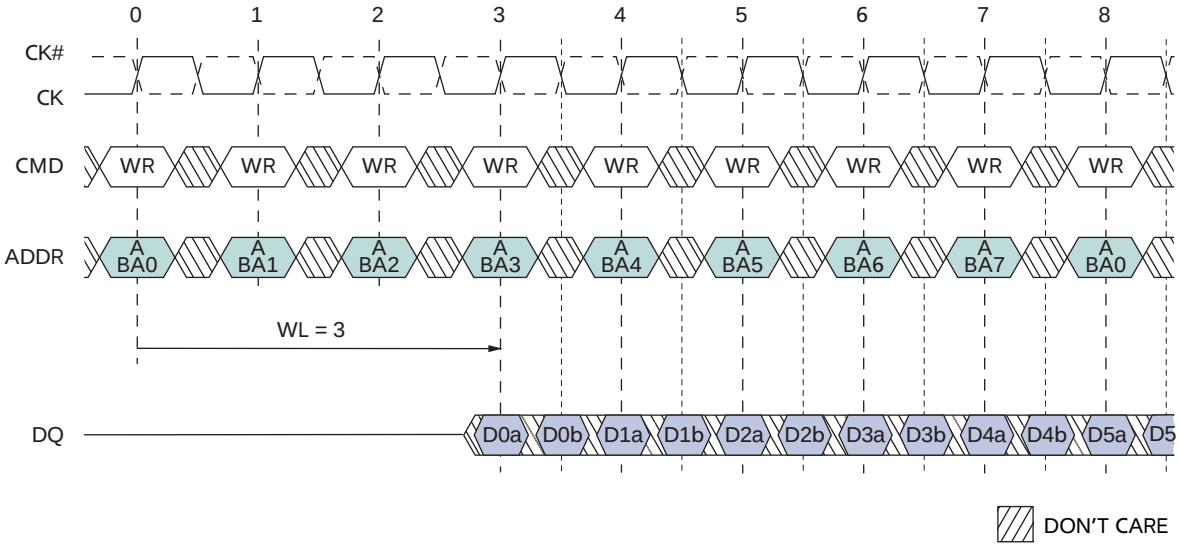
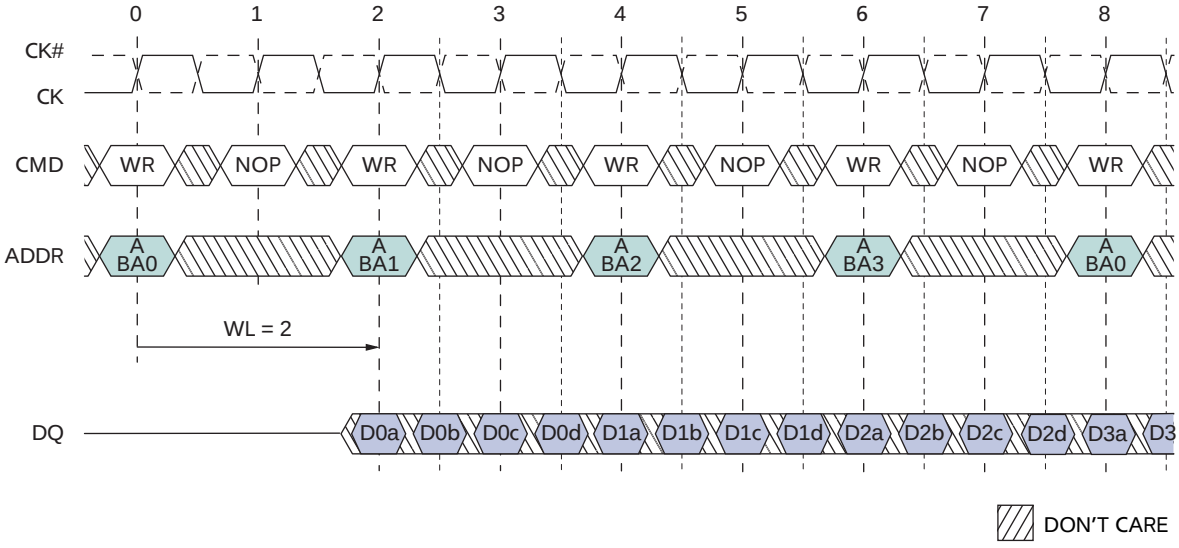
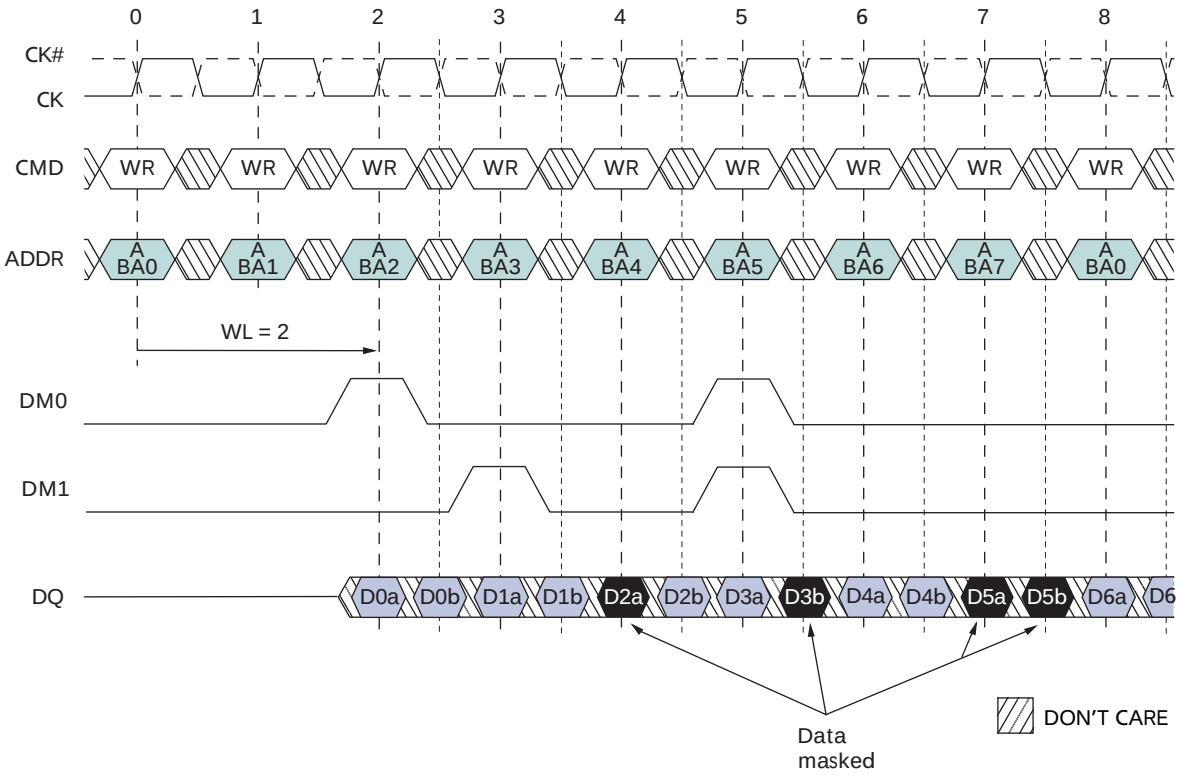



**Figure 13: WRITE Burst Basic Sequence: BL = 4; WL = 2**




Notes: 1. A/BA*x*: address A of bank *x*
WR: WRITE
D*xy*: data *y* to bank *x*
WL: WRITE latency.
2. Any free bank may be used in any given CMD. The sequence shown is only one example of a bank sequence.

**Figure 14: WRITE Data Mask Timing: BL = 2; WL = 2**




Notes: 1. A/BA*x*: address A of bank *x*
WR: WRITE
D*xy*: data *y* to bank *x*
WL: WRITE latency.
2. Any free bank may be used in any given CMD. The sequence shown is only one example of a bank sequence.

**Figure 15: Write Data Mask Timing: BL = 4; WL = 1**

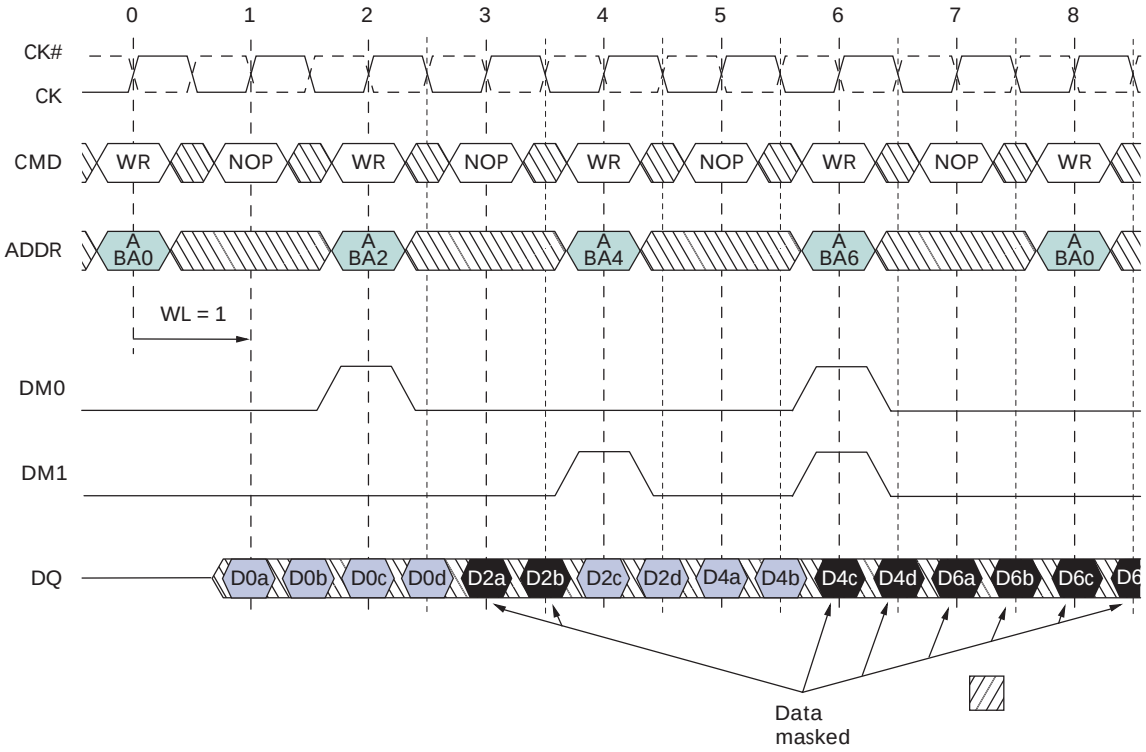
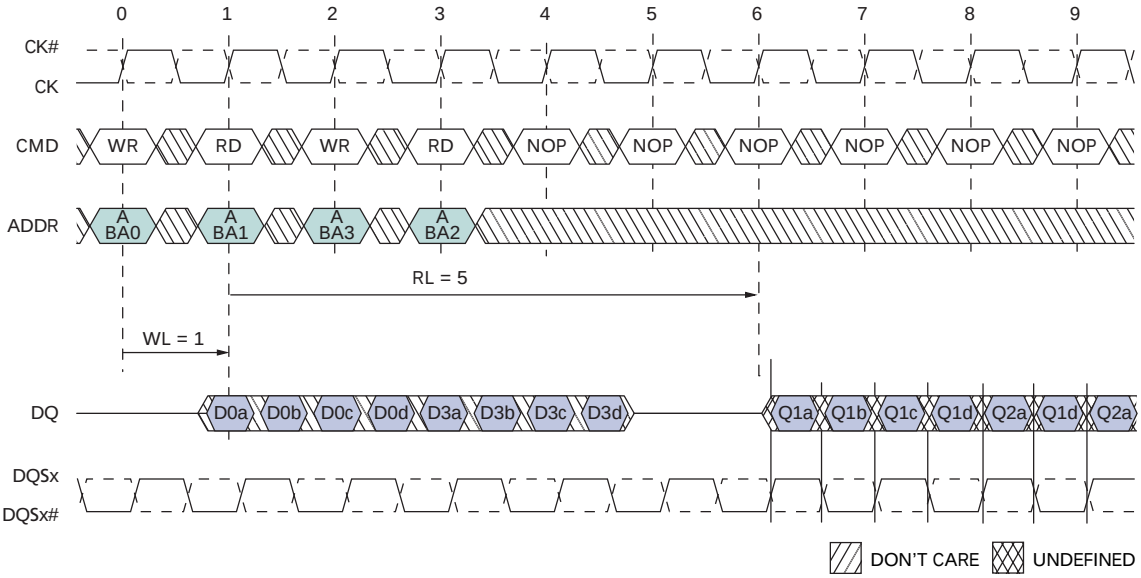



**Figure 16: WRITE followed by READ: BL = 4; RL = 5; WL = 1**




Note: A/BA*x*: address A of bank *x*
WR: WRITE
D*xy*: data *y* to bank *x*
WL: WRITE latency
RD: READ
Q*xy*: data *y* from bank *x*
RL: READ latency.

# Read Basic Information

Read accesses are initiated with a READ command, as shown in Figure 17. Row and bank addresses are provided with the READ command.

During READ bursts, the memory device drives the read data edge-aligned with the DQS signal. After a programmable READ latency, data is available at the outputs. The data valid signal indicates that valid data will be present in the next half clock cycle.

The skew between DQS and the crossing point of CK is specified as $^{t}$CKDQS. $^{t}$DQSQ is the skew between DQS and the last valid data edge considered over all the data generated at the DQ signals. $^{t}$DQSQ is derived at each DQS clock edge and is not cumulative over time.

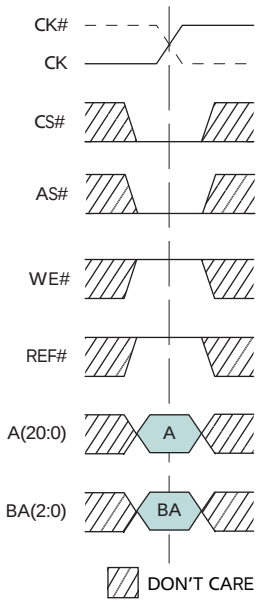
After completion of a burst, assuming no other commands have been initiated, output data (DQ) will go to High-Z. Back-to-back READ commands are possible, producing a continuous flow of output data.

The data valid window is derived from each DQS transition and is defined as:

MIN ($^{t}$CKH, $^{t}$CKL) - 2 $^{t}$DQSQ(MAX)

Any READ burst may be followed by a subsequent WRITE command. Figures 21–24 on page 24–25 illustrate the timing requirements for a READ followed by a WRITE. Depending on the programmed READ latency, a READ-to-WRITE delay occurs in order to prevent bus contention. Some systems having long line lengths or severe skews may need additional idle cycles inserted.

**Figure 17: READ Command**




Note: A: address
BA: bank address.

**Figure 18: Basic READ Burst Timing**

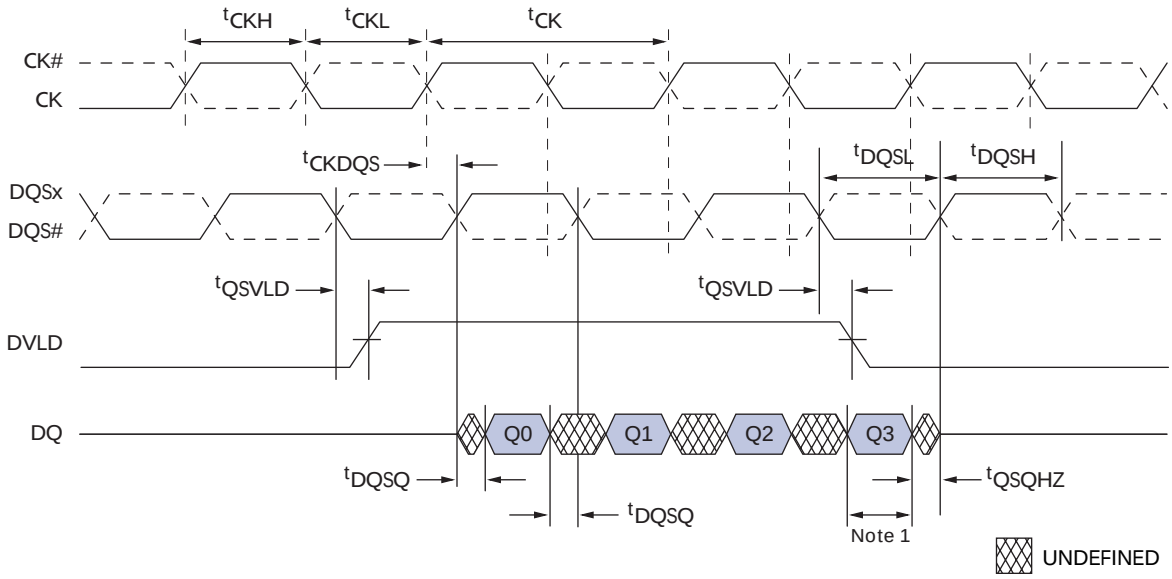



**Table 12: Timing Parameters**

| Symbol | -33 | | -4 | | -5 | | Units |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| tCK | 3.3 | | 4.0 | | 5.0 | | ns |
| tCKH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK |
| tCKL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK |
| tCKDQS | 2.4 | 3.9 | 2.4 | 3.9 | 2.4 | 3.9 | ns |
| tDQSQ | | 0.35 | | 0.35 | | 0.35 | ns |
| tQSQHZ | | 0.4 | | 0.4 | | 0.4 | ns |
| tQSVLD | -0.4 | 0.4 | -0.4 | 0.4 | -0.4 | 0.4 | ns |
| tDQSH | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK |
| tDQSL | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK |

Note: Minimum data valid window can be expressed as MIN (tCKH, tCKL) - 2 × tDQSQ (MAX).

**Figure 19: READ Burst: BL = 2; RL = 5**

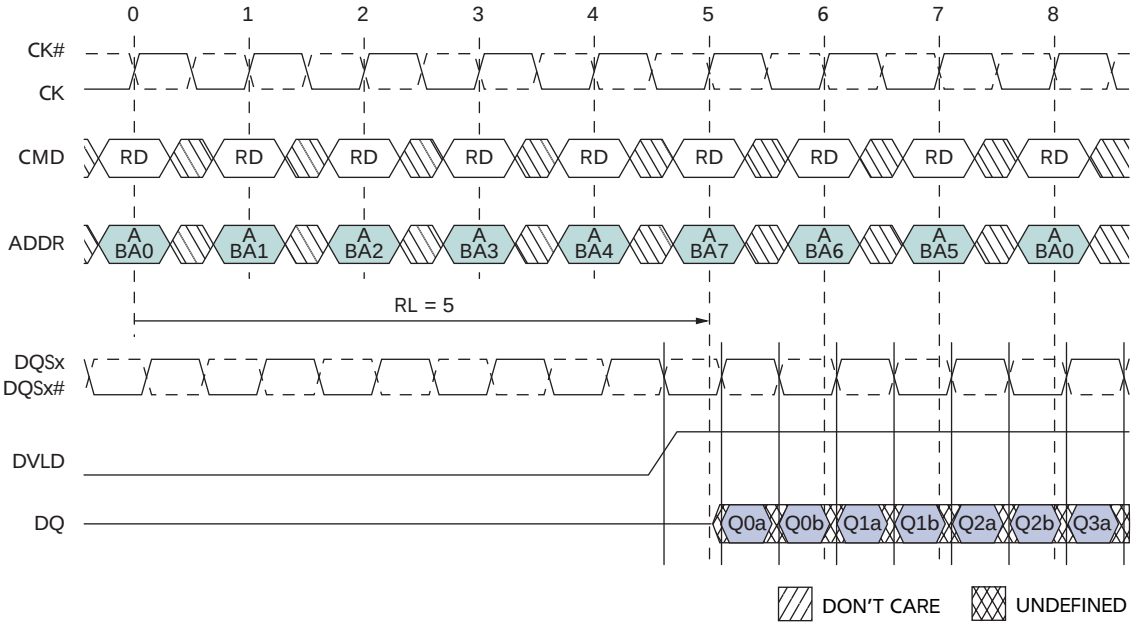
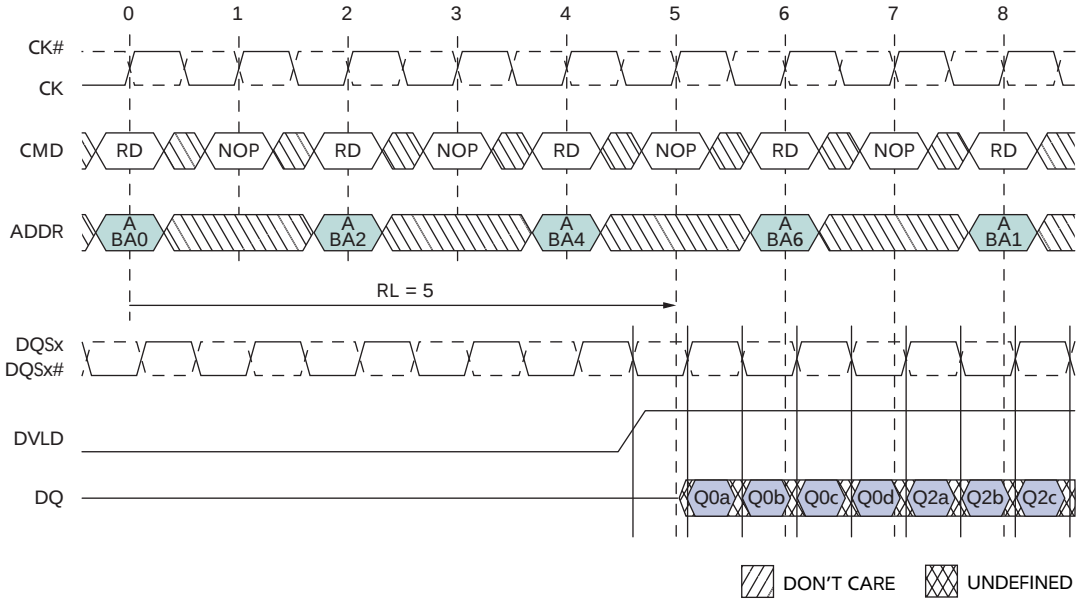



**Figure 20: READ Burst: BL = 4; RL = 5**




Note: A/BA*x*: address A of bank *x*
D*xy*: data *y* to bank *x*
RC: row cycle time
RL: READ latency.

**Figure 21: READ followed by WRITE: BL = 2; RL = 5; WL = 2**

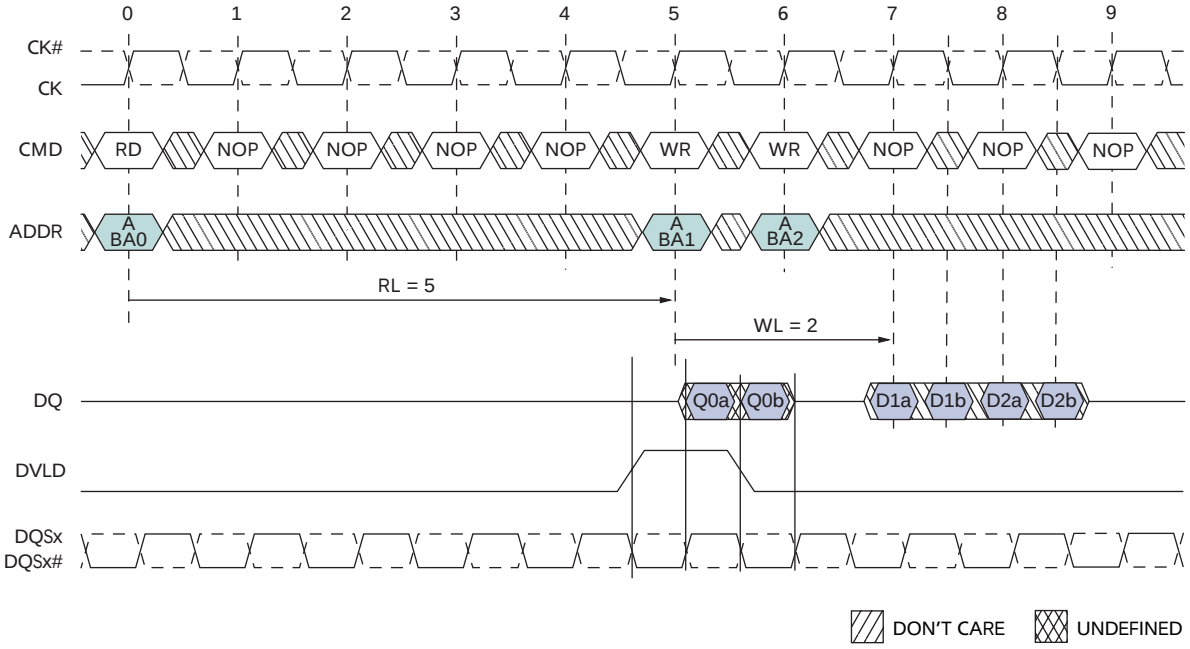
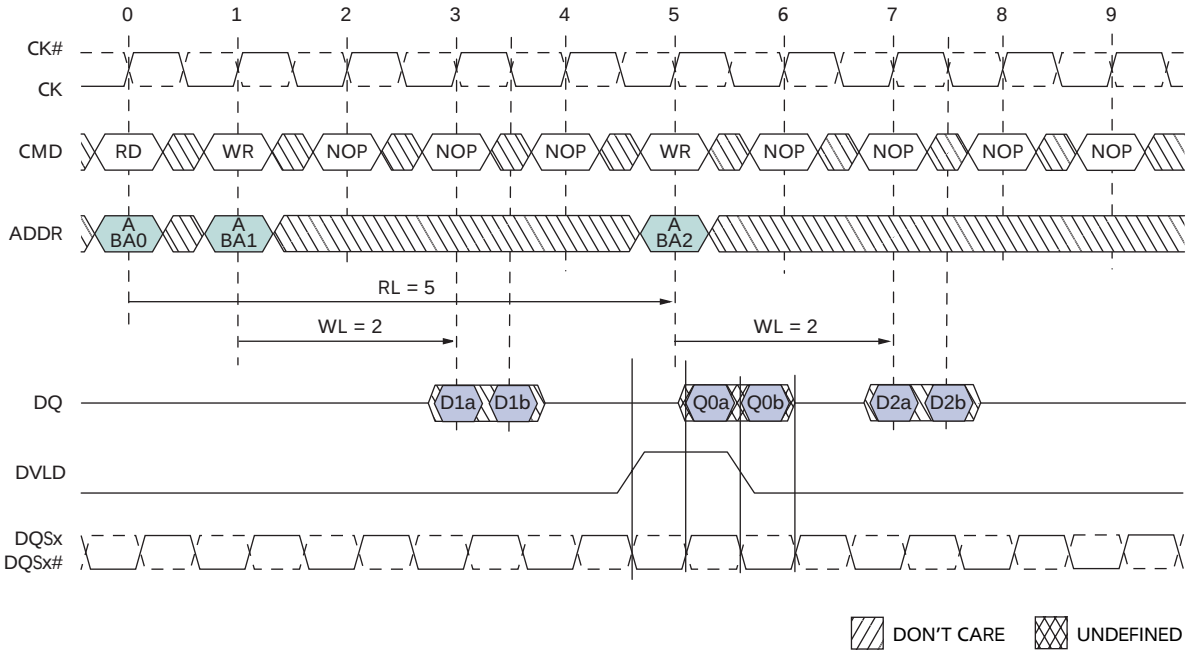



**Figure 22: READ followed by WRITE: BL = 2; RL = 5; WL = 2 – Interleaved Data**




Note: A/BA*x*: address A of bank *x*
D*xy*: data *y* to bank *x*
RD: READ
RL: READ latency
WL: WRITE latency.

**Figure 23: READ followed by WRITE: BL = 4; RL = 5; WL = 1**

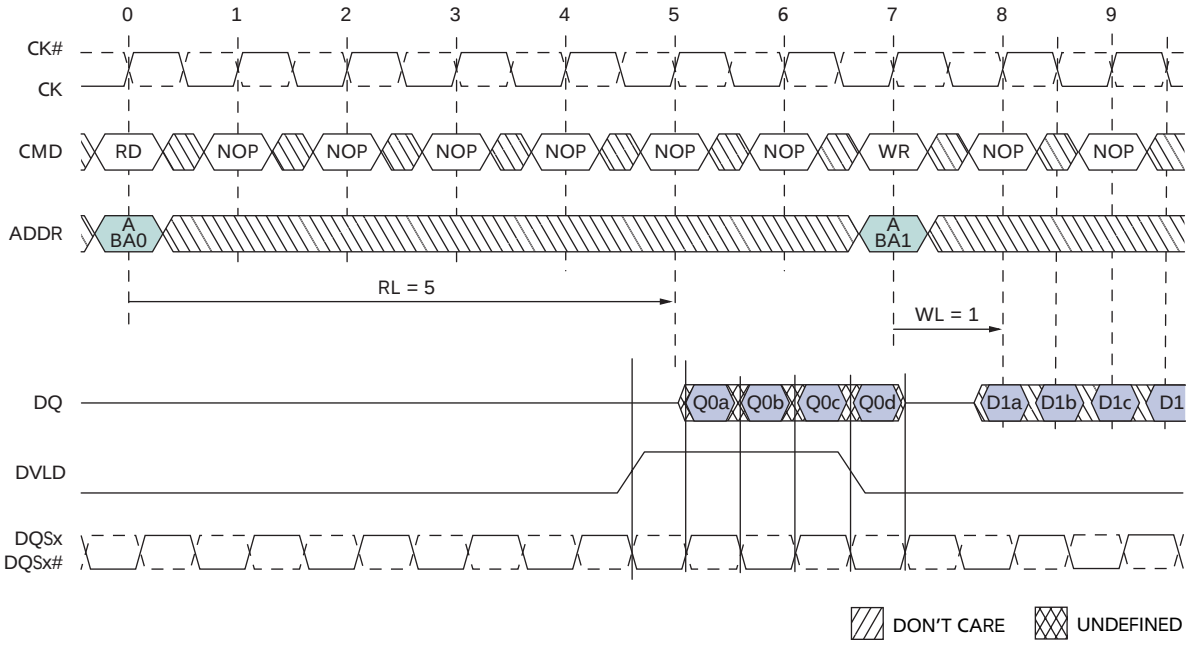
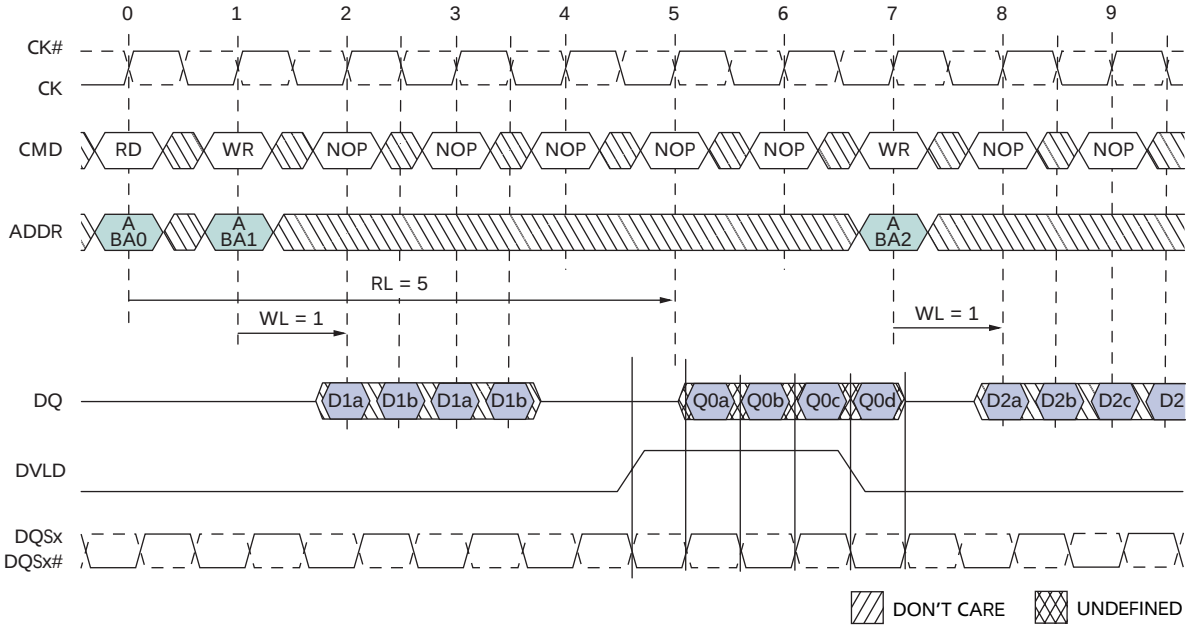



**Figure 24: READ followed by WRITE: BL = 4; RL = 5; WL = 1 – Interleaved Data**



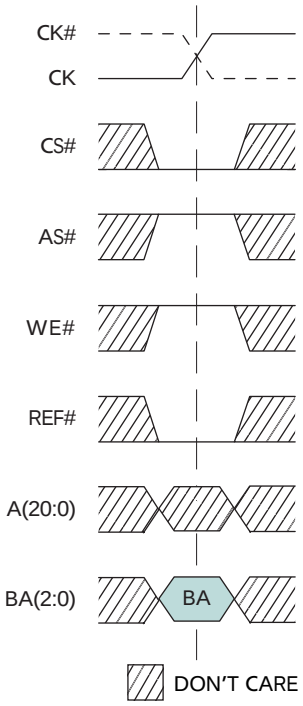

Note: A/BA*x*: address A of bank *x*
D*xy*: data *y* to bank *x*
RD: READ
RL: READ latency
WL: WRITE latency.

# AUTO REFRESH Command (AREF)

AREF is used to perform a REFRESH cycle on 1 row in a specific bank. The row addresses are generated by an internal refresh counter for each bank; external address balls are "DON'T CARE." The delay between the AREF command and a subsequent command to the same bank must be at least $^{t}$RC.

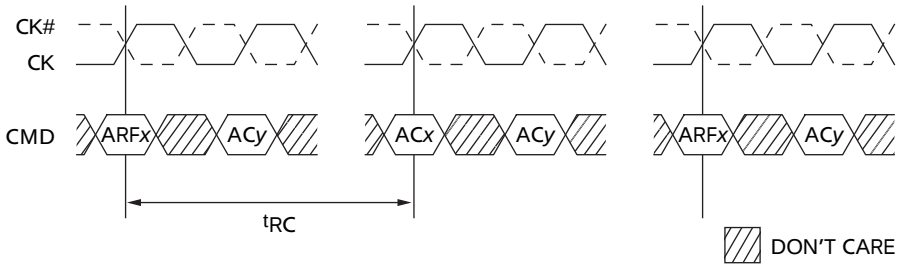
Within a period of 32ms ($^{t}$REF), the entire memory must be refreshed. Figure 25 illustrates an example of a continuous refresh sequence. Other refresh strategies, such as burst refresh, are also possible.

**Figure 25: AUTO REFRESH Command**




Note: BA: Bank address.

**Figure 26: AUTO REFRESH Cycle**




Notes: 1. ACx: any command on bank *x*
ARFx: auto refresh bank *x*
ACy: any command on different bank.
2. $^{t}$RC is configuration-dependent. Refer to Table 10 on page 16.

# IEEE 1149.1 Serial Boundary Scan (JTAG)

The RLDRAM incorporates a serial boundary scan Test Access Port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the RLDRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 1.8V I/O logic levels.

The RLDRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

# Disabling The JTAG Feature

It is possible to operate the RLDRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to VDD through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

# Test Access Port (TAP)

## Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

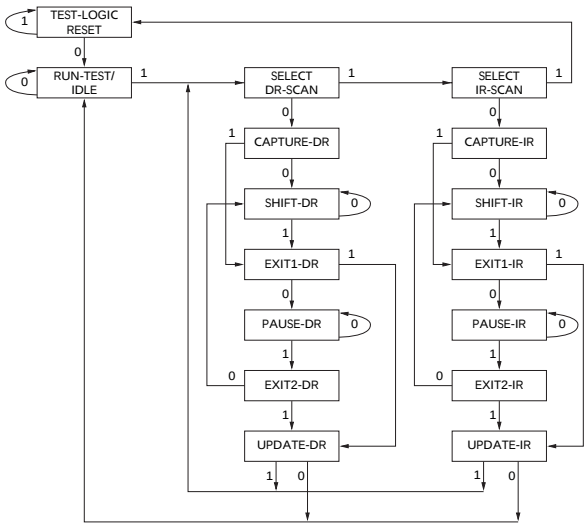
## Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

## Test Data-in (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 27 on page 28. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Figure 28 on page 29.)

**Figure 27: TAP Controller State Diagram**




Note: The 0/1 next to each state represents the value of TMS at the rising edge of $^{t}$CK.

## Test Data-out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. (See Figure 27.) The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Figure 28 on page 29.)

## Performing A Tap RESET

A RESET is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the RLDRAM and may be performed while the RLDRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

## Tap Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the RLDRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

## Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls, as shown in Figure 28. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

## Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the RLDRAM with minimal delay. The bypass register is set LOW (VSS) when the BYPASS instruction is executed.

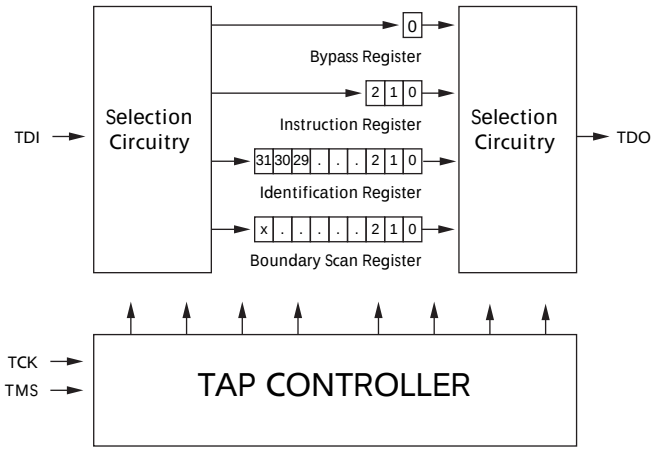
## Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the RLDRAM. Several no connect (NC) balls are also included in the scan register to reserve pins. The RLDRAM has a 104-bit register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRE-LOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables (see page 34) show the order in which the bits are connected. Each bit corresponds to one of the balls on the RLDRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

**Figure 28: TAP Controller Block Diagram**




Note: x = 103 for all configurations.

## Identification (Id) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hard-wired into the RLDRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Table 15 on page 33.

# Tap Instruction Set

## Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table (see page 33). Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this RLDRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the RLDRAM and cannot preload the I/O buffers. The RLDRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

## EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all zeros. EXTEST is not implemented in the TAP controller, hence this device is not IEEE 1149.1 compliant.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the RLDRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. EXTEST does not place the RLDRAM outputs in a High-Z state.

## IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

## SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 50 MHz, while the RLDRAM clock operates significantly faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the RLDRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time ($^{t}$CS plus $^{t}$CH). The RLDRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRE-LOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

## BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

## Reserved for Future Use

The remaining 22 instructions are not implemented but are reserved for future use. Do not use these instructions.

**Figure 29: TAP Timing**

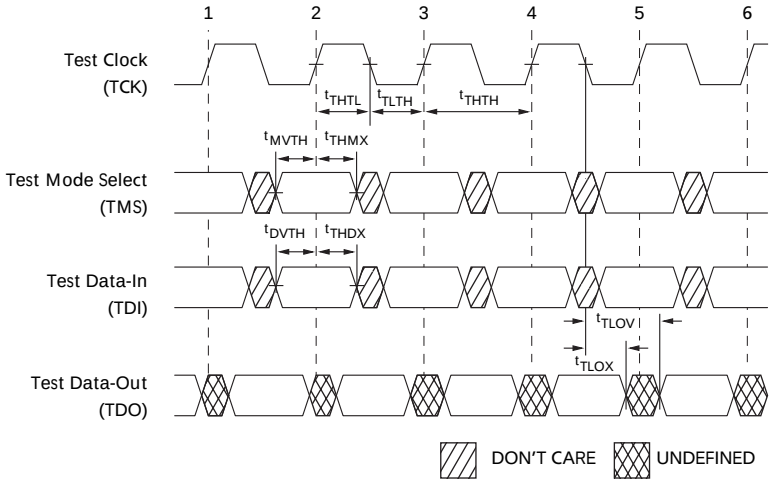


**Table 13: TAP AC Electrical Characteristics**

Note 1; +0°C ≤ $T_C$ ≤ +95°C; +1.7V ≤ VDD ≤ +1.95V

| Description | Symbol | Min | Max | Units |
|---|---|---|---|---|
| **Clock** | | | | |
| Clock cycle time | $^{t}$THTH | 20 | | ns |
| Clock frequency | $^{f}$TF | | 50 | MHz |
| Clock HIGH time | $^{t}$THTL | 10 | | ns |
| Clock LOW time | $^{t}$TLTH | 10 | | ns |
| **Output Times** | | | | |
| TCK LOW to TDO unknown | $^{t}$TLOX | 0 | | ns |
| TCK LOW to TDO valid | $^{t}$TLOV | | 10 | ns |
| TDI valid to TCK HIGH | $^{t}$DVTH | 5 | | ns |
| TCK HIGH to TDI invalid | $^{t}$THDX | 5 | | ns |
| **Setup Times** | | | | |
| TMS setup | $^{t}$MVTH | 5 | | ns |
| Capture setup | $^{t}$CS | 5 | | ns |
| **Hold Times** | | | | |
| TMS hold | $^{t}$THMX | 5 | | ns |
| Capture hold | $^{t}$CH | 5 | | ns |

Notes: 1. $^{t}$CS and $^{t}$CH refer to the setup and hold time requirements of latching data from the boundary scan register

**Table 14: TAP DC Electrical Characteristics and Operating Conditions**

+0°C ≤ $T_C$ ≤ 95°C; +1.7V ≤ VDD ≤ +1.95V, unless otherwise noted

| Description | Conditions | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Input high (Logic 1) voltage | | VIH | VREF + 0.15 | VDD + 0.3 | V | 1, 2 |
| Input low (Logic 0) voltage | | VIL | VSSQ - 0.3 | VREF - 0.15 | V | 1, 2 |
| Input leakage current | 0V ≤ VIN ≤ VDD | ILI | -5.0 | 5.0 | µA | |
| Output leakage current | Output disabled, 0V ≤ VIN ≤ VDD | ILO | -5.0 | 5.0 | µA | |
| Output low voltage | IOLC = 100µA | VOL1 | | 0.2 | V | 1 |
| Output low voltage | IOLT = 2mA | VOL2 | | 0.4 | V | 1 |
| Output high voltage | \|IOHC\| = 100µA | VOH1 | VDDQ - 0.2 | | V | 1 |
| Output high voltage | \|IOHT\| = 2mA | VOH2 | VDDQ - 0.4 | | V | 1 |

Notes: 1. All voltages referenced to VSS (GND).
2. Overshoot: VIH(AC) ≤ VDD + 0.7V for t ≤ $^{t}$CK/2.
Undershoot: VIL(AC) ≤ -0.5V for t ≤ $^{t}$CK/2.
During normal operation, VDDQ must not exceed VDD.

**Table 15: Identification Register Definitions**

| Instruction Field | All Devices | Description |
|---|---|---|
| REVISION NUMBER (31:28) | 00ab | ab = 10 for x32, 01 for x16 |
| DEVICE ID (27:12) | 0000000010100111 | This represents the part number |
| MICRON JEDEC ID CODE (11:1) | 00000101100 | Allows unique identification of RLDRAM vendor |
| ID Register Presence Indicator (0) | 1 | Indicates the presence of an ID register |

**Table 16: Scan Register Sizes**

| Register Name | Bit Size |
|---|---|
| Instruction | 8 |
| Bypass | 1 |
| ID | 32 |
| Boundary Scan | 104 |

**Table 17: Instruction Codes**

| Instruction | Code | Description |
|---|---|---|
| EXTEST | 0000 0000 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction is not 1149.1-compliant. This operation does not affect RLDRAM operations. |
| SAMPLE/PRELOAD | 0000 0101 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant. |
| IDCODE | 0010 0001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect RLDRAM operations. |
| BYPASS | 1111 1111 | Places the bypass register between TDI and TDO. This operation does not affect RLDRAM operations. |

**Table 18: Boundary Scan (Exit) Order**
Note 1

| Bit# | FBGA Ball | Bit# | FBGA Ball | Bit# | FBGA Ball |
|---|---|---|---|---|---|
| 1 | K1 | 36 | R11 | 71 | C11 |
| 2 | K2 | 37 | P11 | 72 | C11 |
| 3 | L2 | 38 | P11 | 73 | C10 |
| 4 | L1 | 39 | P10 | 74 | C10 |
| 5 | M1 | 40 | P10 | 75 | B11 |
| 6 | M3 | 41 | N11 | 76 | B11 |
| 7 | M2 | 42 | N11 | 77 | B10 |
| 8 | N1 | 43 | N10 | 78 | B10 |
| 9 | N3 | 44 | N10 | 79 | B3 |
| 10 | N3 | 45 | N12 | 80 | B3 |
| 11 | N2 | 46 | M11 | 81 | B2 |
| 12 | N2 | 47 | M10 | 82 | B2 |
| 13 | P3 | 48 | M12 | 83 | C3 |
| 14 | P3 | 49 | L12 | 84 | C3 |
| 15 | P2 | 50 | L11 | 85 | C2 |
| 16 | P2 | 51 | K11 | 86 | C2 |
| 17 | R2 | 52 | K12 | 87 | D3 |
| 18 | R3 | 53 | J12 | 88 | D2 |
| 19 | T2 | 54 | J11 | 89 | E2 |
| 20 | T2 | 55 | H11 | 90 | E2 |
| 21 | T3 | 56 | H12 | 91 | E3 |
| 22 | T3 | 57 | G12 | 92 | E3 |
| 23 | U2 | 58 | G10 | 93 | F2 |
| 24 | U2 | 59 | G11 | 94 | F2 |
| 25 | U3 | 60 | F12 | 95 | F3 |
| 26 | U3 | 61 | F10 | 96 | F3 |
| 27 | U10 | 62 | F10 | 97 | F1 |
| 28 | U10 | 63 | F11 | 98 | G2 |
| 29 | U11 | 64 | F11 | 99 | G3 |
| 30 | U11 | 65 | E10 | 100 | G1 |
| 31 | T10 | 66 | E10 | 101 | H1 |
| 32 | T10 | 67 | E11 | 102 | H2 |
| 33 | T11 | 68 | E11 | 103 | J2 |
| 34 | T11 | 69 | D11 | 104 | J1 |
| 35 | R10 | 70 | D10 | | |

Notes: 1. Any unused pins that are in the order will read as a logic “0.”

# Electrical Characteristics

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Figure 30: Absolute Maximum Ratings**

| Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|
| Storage temperature | -55 | +150 | °C | |
| I/O voltage | -0.3V | VDDQ + 0.3 | V | |
| Voltage on VEXT supply relative to Vss | -0.3 | +2.8 | V | |
| Voltage on VDD supply relative to Vss | -0.3 | +2.1 | V | |
| Voltage on VDDQ supply relative to Vss | -0.3 | +2.1 | V | |
| Junction temperature | 110 | | °C | 1 |

Notes: 1. Junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow.

# Recommended DC Operation Ranges

All values are recommended operating conditions unless otherwise noted. External on board (PCB) capacitance values are required as follows:

- VDDQ: 2 × 0.1µF/device
- VDD: 2 × 0.1µF/device
- VREF: 0.1µF/device
- VEXT : 0.1µF/device

**Table 19: DC Electrical Characteristics and Operating Conditions**
0°C ≤ $T_C$ ≤ +95°C; +1.7V ≤ VDD ≤ +1.95V unless otherwise noted

| Descriptions | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Supply voltage | VEXT | 2.38 | 2.63 | V | 1 |
| Supply voltage | VDD | 1.7 | 1.95 | V | 1 |
| Isolated output buffer supply | VDDQ | 1.7 | VDD | V | 1, 2 |
| Reference voltage | VREF | 0.49 × VDDQ | 0.51 × VDDQ | V | 1, 3, 4 |

Notes: 1. All voltages referenced to Vss (GND).
2. During normal operation, VDDQ must not exceed VDD.
3. Typically the value of VREF is expected to be 0.5x VDDQ of the transmitting device. VREF is expected to track variations in VDDQ.
4. Peak to peak AC noise on VREF must not exceed 2% VREF(DC).

**Table 20: DC Electrical Characteristics and Operating Conditions**

0°C ≤ $T_C$ ≤ +95°C; +1.7V ≤ VDD ≤ +1.95V unless otherwise noted

| Description | Conditions | Symbol | MIn | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Input high (Logic 1) voltage<br>Input low (Logic 0) voltage<br>Output high voltage<br>Output low voltage | Matched impedance mode | VIH | VREF + 0.15 | VDDQ + 0.3 | V | 1, 2 |
| | Matched impedance mode | VIL | VssQ - 0.3 | VREF - 0.15 | V | 1, 2 |
| | Matched impedance mode | VOH | VDDQ | | V | 1, 3, 4 |
| | Matched impedance mode | VOL | | 0 | V | 1, 3, 4 |
| Input high (Logic 1) voltage<br>Input low (Logic 0) voltage<br>Output high voltage<br>Output low voltage | HSTL strong | VIH | VREF + 0.1 | VDDQ + 0.3 | V | 1, 2 |
| | HSTL strong | VIL | VssQ - 0.3 | VREF - 0.1 | V | 1, 2 |
| | HSTL strong | VOH | VDDQ - 0.4 | | V | 1, 3, 4 |
| | HSTL strong | VOL | | 0.4 | V | 1, 3, 4 |
| Clock input leakage current | | ILC | -5 | 5 | µA | |
| Input Leakage current | 0V ≤ VIN ≤ VDDQ | ILI | -5 | 5 | µA | |
| Output leakage current | | ILO | -5 | 5 | µA | |
| Reference voltage current | | IREF | -5 | 5 | µA | |

Notes:
1. All voltages referenced to Vss (GND).
2. Overshoot: VIH(AC) ≤ VDD + 0.7V for t ≤ $^tCK/2$
   Undershoot: VIL(AC) ≥ –0.5V for t ≤ $^tCK/2$
   During normal operation, VDDQ must not exceed VDD. Control input signals may not have pulse widths less than $^tCK/2$ or operate at frequencies exceeding $^tCK$ (MAX).
3. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
4. HSTL outputs meet JEDEC HSTL Class I and Class II standards.

**Table 21: Capacitance**

| Description | Conditions | Symbol | MIn | Max | Units |
|---|---|---|---|---|---|
| Address/Control input capacitance | $T_A$ = 25°C; f = 1 MHz | CI | 2.0 | 4.0 | pF |
| Input/Output capacitance (DQ) | | CO | 2.0 | 4.0 | pF |
| Clock capacitance | | CCK | 2.0 | 4.0 | pF |

**Table 22: AC Electrical Characteristics and Operating Conditions**

0°C ≤ $T_C$ ≤ +95°C; +1.7V ≤ VDD ≤ +1.95V unless otherwise noted

| Description | Conditions | Symbol | MIn | Max | Units |
|---|---|---|---|---|---|
| Input high (Logic 1) voltage<br>Input low (Logic 0) voltage | Matched impedance mode | VIH | VREF + 0.3 | VDDQ + 0.3 | V |
| | Matched impedance mode | VIL | VssQ - 0.3 | VREF - 0.3 | V |
| Input high (Logic 1) voltage<br>Input low (Logic 0) voltage | HSTL strong | VIH | VREF + 0.2 | VDDQ + 0.3 | V |
| | HSTL strong | VIL | VssQ - 0.3 | VREF - 0.2 | V |

**Figure 31: Output Test Conditions**

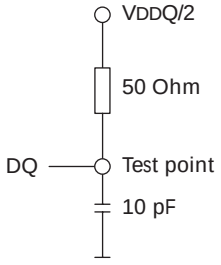


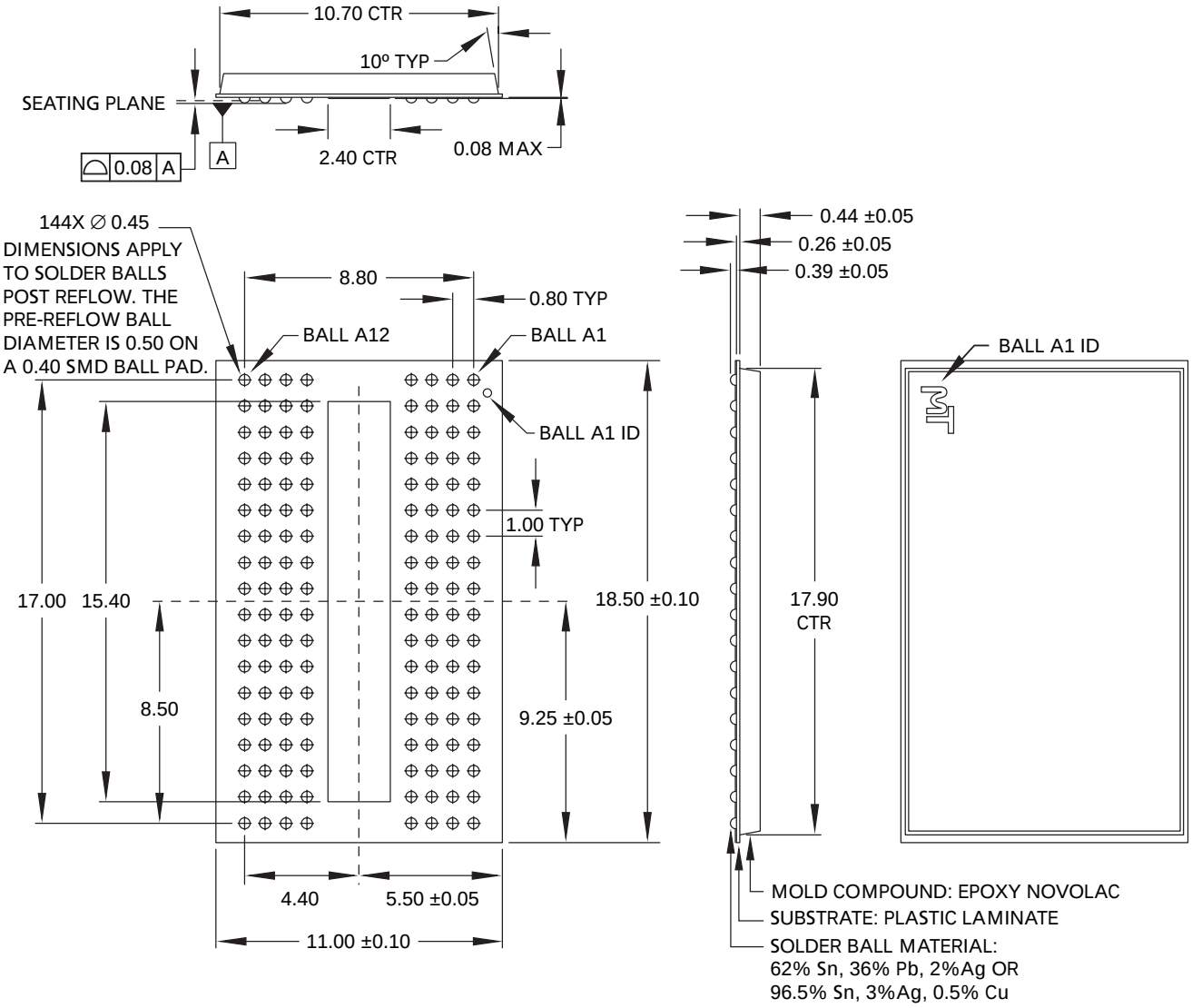
**Table 23: IDD Operating Conditions and Maximum Limits**

+0°C ≤ $T_C$ ≤ +95°C; VDD = MAX unless otherwise noted

| Description | Conditions | Symbol | Max | | | Units |
|---|---|---|---|---|---|---|
| | | | -33 | -4 | -5 | |
| Standby current | tCK = Idle<br>All banks idle, no inputs toggling | ISB1 (VDD) x32 | 59 | 59 | 59 | mA |
| | | ISB1 (VDD) x16 | 55 | 55 | 55 | |
| | | ISB1 (VEXT) | 12 | 12 | 12 | |
| Active standby current | tCK = MIN, CS# = 1<br>No commands, half address/data toggle up to once every 4 clock cycles | ISB2 (VDD) x32 | 280 | 271 | 228 | mA |
| | | ISB2 (VDD) x16 | 255 | 244 | 205 | |
| | | ISB2 (VEXT) | 12 | 12 | 12 | |
| Incremental current | BL = 2, tCK = MIN, tRC = MIN,<br>1 bank active, half address data toggles once per tRC, read followed by write sequence | IDD1 (VDD) x32 | 287 | 266 | 240 | mA |
| | | IDD1 (VDD) x16 | 263 | 243 | 221 | |
| | | IDD1 (VEXT) | 16 | 16 | 16 | |
| Incremental current | BL = 4, tCK = MIN, tRC = MIN,<br>1 bank active, half address/data toggle once per tRC, read followed by write sequence | IDD2 (VDD) x32 | 341 | 326 | 300 | mA |
| | | IDD2 (VDD) x16 | 285 | 273 | 250 | |
| | | IDD2 (VEXT) | 20 | 20 | 20 | |
| Burst refresh current | tCK = MIN, tRC = MIN<br>Cyclic bank refresh, data inputs are switching | IREF1 (VDD) x32 | 460 | 431 | 357 | mA |
| | | IREF1 (VDD) x16 | 451 | 419 | 347 | |
| | | IREF1 (VEXT) | 79 | 68 | 57 | |
| Distributed refresh current | tCK = MIN, tRC = MIN<br>Single bank refresh, half address/data toggle | IREF2 (VDD) x32 | 282 | 268 | 249 | mA |
| | | IREF2 (VDD) x16 | 265 | 254 | 231 | |
| | | IREF2 (VEXT) | 20 | 20 | 20 | |
| Operating supply current example | BL = 2, tCK = MIN, 8 bank cyclic access, half of address bits change every 4 clock cycles, continuous data | IDD2W(VDD) x32 | 807 | 706 | 598 | mA |
| | | IDD2W (VDD) x16 | 713 | 616 | 519 | |
| | | IDD2W(VEXT) | 46 | 40 | 34 | |
| Operating supply current example | BL = 4, tCK = MIN, 8 bank cyclic access, half of address bits change every 2 clocks, continuous data | IDD4W (VDD) x32 | 723 | 634 | 521 | mA |
| | | IDD4W (VDD) x16 | 549 | 476 | 392 | |
| | | IDD4W (VEXT) | 46 | 40 | 34 | |

# Package Dimensions

**Figure 32: 144-Ball µBGA**




Note: All dimensions in millimeters.

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