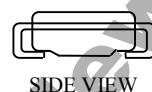
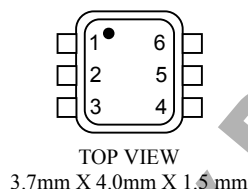


FEATURES

- Low impedance coupler to create large common-ground, multi-level MicroLAN networks
- Keeps inactive branches pulled high to 5V
- Simplifies network topology analysis by logically decoupling devices on active network segments
- Conditional search for fast-event signaling
- Auxiliary 1-Wire® line to connect a memory chip or to be used as digital input
- Programmable, general-purpose open-drain control output
- Communicates at 16.3kbits per second
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute traceability because no two parts are alike
- 8-bit family code specifies device communication requirements to bus master
- Built-in multidrop controller ensures compatibility with other MicroLAN products
- Operating temperature range from -40°C to +85°C
- Compact, low-cost 6-pin TSOC surface mount package

PIN ASSIGNMENT



6-PIN TSOC PACKAGE

PIN DESCRIPTION

Pin 1	GND
Pin 2	1-Wire in
Pin 3	Main 1-Wire out
Pin 4	Auxiliary 1-Wire out
Pin 5	Control Output
Pin 6	V _{DD}

ORDERING INFORMATION

DS2409P	6-pin TSOC package
DS2409P/T&R	Tape and Reel of DS2409P

DESCRIPTION

The MicroLAN coupler is an essential component to build and control 1-Wire MicroLAN networks with multi-level branching. In contrast to approaches that switch the ground line, the coupler maintains a common ground level for the whole network and keeps the inactive segments powered. This simplifies supplying central or local power for additional circuitry and prevents loss of status of parasitically powered devices. It also avoids disrupting communication caused by the parasitic power supply of 1-Wire devices after activating a branch. The coupler does not contain any user-programmable memory. To label a branch, one can connect any 1-Wire memory device to the auxiliary 1-Wire output of the coupler. Both the main and the auxiliary 1-Wire output are supported by a "smart-on" command. This command generates a reset/presence sequence on the selected output before the electronic switch closes the contact to the 1-Wire bus. This way the bus master can apply a ROM function command (optionally followed by a memory function) to the devices on the just activated segment with all other devices in the network.

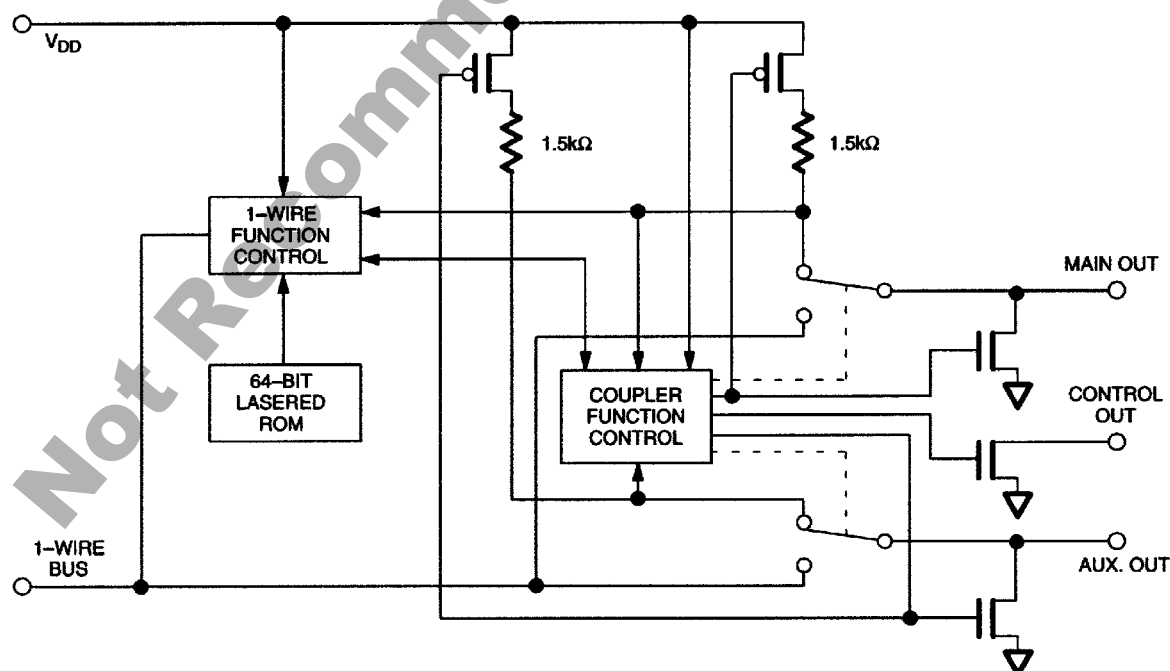
remaining deselected. This significantly speeds up the analysis of topology and population in a continuously changing network. The coupler also supports the bus master in detecting arrivals on the inactive segments of the network by responding to the conditional search command. The control output can be used to optically signal the on/off state of a branch or, together with the auxiliary output, for handshaking in dual-master applications. The network size can be maximized by using a DS2480 line driver at the bus master's serial interface. The DS2480 compensates for the rising ground level caused by the non-zero on-resistance of couplers in multi-level networks.

OVERVIEW

The DS2409 Coupler provides a means to create large MicroLAN networks with additional control capability provided by an open-drain N-channel MOSFET that can be remotely switched via communication over the 1-Wire bus (Figure 1). An auxiliary output can be used to label the branch by connecting a programmed 1-Wire memory chip or as digital input. The DS2409 contains a factory-lasered registration number that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit family code (1FH). The 64-bit ROM portion of the DS2409 not only creates an absolutely unique electronic identification for the device itself but also is a means to locate and address the device in order to exercise its control functions.

The DS2409 uses the standard Dallas Semiconductor 1-Wire protocol for data transfers (Figure 2), with all data being read and written least significant bit first. Communication to and from the DS2409 requires a single bi-directional line that is typically a port pin of a microcontroller. The 1-Wire bus master (microcontroller) must first issue one of five ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, or 5) Conditional Search ROM. These commands operate on the 64-bit lasered ROM portion of each device and can singulate a specific device if many are present on the 1-Wire line as well as indicate to the bus how many and what type of each device is present. After a ROM function command is successfully executed, the control functions of the device can be exercised via the 1-Wire bus.

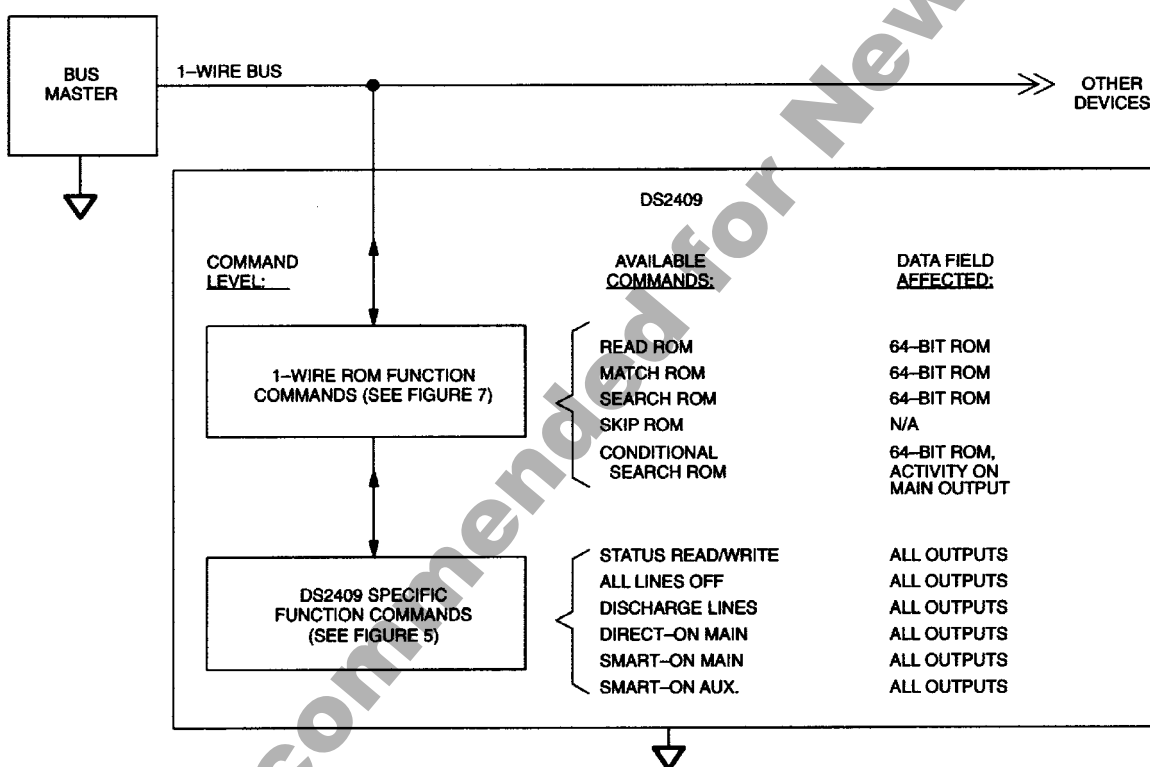
BLOCK DIAGRAM Figure 1



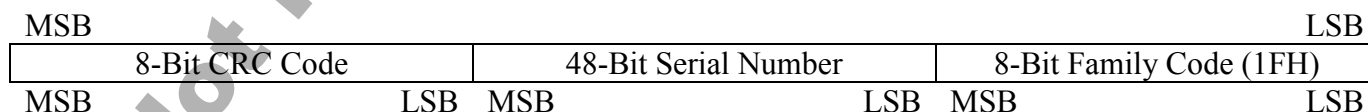
64-BIT LASERED ROM

Each DS2409 contains a unique ROM code that is 64 bits long. The first eight bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 3.) The 1-Wire CRC of the lasered ROM is generated using the polynomial $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas Semiconductor 1-Wire Cyclic Redundancy Check is available in the Book of DS19xx iButton® Standards. The 64-bit ROM and ROM Function Control section allow the DS2409 to operate as a 1-Wire device and follow the 1-Wire protocol detailed in the section “1-Wire Bus System”. The functions required to exercise the control functions of the DS2409 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM functions flow chart (Figure 7). The 1-Wire bus master must first provide one of the five ROM function commands. After a ROM function sequence has been successfully executed, the bus master may then provide any one of the function commands specific to the DS2409 (Figure 5).

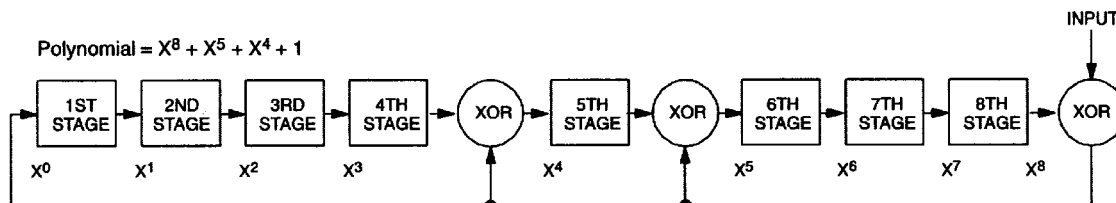
HIERARCHICAL STRUCTURE FOR 1-WIRE PROTOCOL Figure 2



64-BIT LASERED ROM Figure 3



1-WIRE CRC GENERATOR Figure 4



CONTROL FUNCTION COMMANDS

The “Control Function Flow Chart” (Figure 5) describes the protocols necessary for controlling the main and auxiliary output as well as the control output of the DS2409. The 1-Wire Function Control section and the Coupler Function Control section combine to interpret the commands issued by the bus master and create the correct control signals within the device. Depending on the complexity of function to be exercised, the 1-byte command code may require one or two more bytes being sent by the bus master. Switching one branch on implies that the other branch is automatically switched off. At power-on, both branches are switched off. Each command flow includes at least one byte of feedback information for the bus master to check if the command was understood and executed.

STATUS READ/WRITE [5Ah]

This command should be sent to the device after powering up unless the default settings are adequate for the application. Following the command code, the bus master has to send the status control byte. The bus master will then read the status info byte from the device. The confirmation byte is identical to the status info byte. Tables 1 and 2 show the bit assignments in both bytes.

At power-on the device will be in the auto-control mode and the control output will be assigned to the main output. The control output can be assigned to the auxiliary output by setting bit 6 of the status control byte to a 1. For manual operation of the control output one has to select manual mode (bit 5 = 1). The value of bit 7 of the status control byte will then determine the status of the control output. A 1 for bit 7 will make the transistor conducting, a 0 will turn it off (non-conducting). To change the status of the device, both bits 3 and 4 of the status control byte have to be 0. Otherwise the settings will remain unchanged. In any case, the status info byte will reflect the currently valid settings including the changes that might have been made with the status control byte.

The status info byte allows the bus master to verify the actual status of each output (STAT, active/inactive, on/off) and the static level at the main and auxiliary output (LEVL, 1 for normal, 0 in case of a short). If a 1-Wire output is inactive and a low-going edge is encountered during this time, the DS2409 will set the event flag (EVNT) the status info byte. Each output has its own event flag. The event flags are cleared with the All Lines Off command. Bit 7 of the status info byte tells if the device is auto-control mode or manual mode. Depending on the value of this bit, the information in bit 6 (CNTR. STAT) either reports the association of the control output to a particular output (auto-control mode) or the status of the transistor at the control output.

STATUS CONTROL BYTE Table 1

7	6	5	4	3	2	1	0
DATA X	CNTR. SEL.	MODE	R/ $\overline{W}$	R/ $\overline{W}$	X	X	X

0-2	X	don't care
3-4	R/ $\overline{W}$	Write control: both bits must be 0 to change the status.
5	MODE	control output mode selection: 0 = auto-control mode (default), 1 = manual mode
6	CNTR. SEL.	control output association (auto-control mode): 0 = main (default), 1 = auxiliary
7	DATA X	Value to be written to control output (manual mode only): don't care otherwise

STATUS INFO BYTE Table 2

7	6	5	4	3	2	1	0
MODE	CNTR. STAT	EVNT AUX.	EVNT MAIN	AUX. LEVL	AUX. STAT	MAIN LEVL	MAIN STAT

0	MAIN STAT	status of main output: 0 = active (connected to bus master), 1 = inactive
1	MAIN LEVL	voltage sensed at main output: 0 = low, 1 = high (see note)
2	AUX. STAT	status of auxiliary output: 0 = active (connected to bus master), 1 = inactive
3	AUX. LEVL	voltage sensed at auxiliary output: 0 = low, 1 = high (see note)
4	EVNT MAIN	event flag for main output: 0 = no event, 1 = negative edge sensed since inactive
5	EVNT AUX.	event flag for aux. Output: 0 = no event, 1 = negative edge sensed since inactive
6	CNTR. STAT	if auto-control mode: control output association, 0 = main, 1 = auxiliary if manual mode: 0 = output transistor off, 1 = output transistor on
7	MODE	control output mode: 0 = auto-control mode, 1 = manual mode

NOTE:

Data is valid only if the output is decoupled from the 1-Wire input.

ALL LINES OFF [66h]

This command is used to deactivate the currently active 1-Wire output and to clear both event flags or to end a discharge cycle initiated by the Discharge Lines command. Before issuing this command, one should read the status and check the event flags of both, the main and the auxiliary output. Otherwise one might inadvertently clear the event flag without having taken appropriate action. If the DS2409 is in auto-control mode, the transistor at the control output will be switched off (non-conducting). At power-on, the device will automatically perform the All Lines Off command. In contrast to a power-on cycle, the All Lines Off command does not clear the Mode and Control Select bits.

DISCHARGE LINES [99h]

There may be situations where one has to force a power-on reset for parasitically powered 1-Wire devices connected to the main or auxiliary output of the DS2409. For this purpose, the Discharge Lines command has been implemented. This command first deactivates the output lines and then turns on the pulldown transistors of both, the main and the auxiliary outputs. This state will be maintained until the bus master accesses the coupler again and issues a different control function command. The duration of the discharge time should be 100ms minimum and is controlled solely by the bus master.

Although any of the other control function commands will end the discharge cycle, it is recommended to use the All Lines Off or Status Read/Write command to do so. This will allow the discharged lines to fully recharge and prevent a sudden voltage droop on the active part of the network in case of a Direct-On Main command. This precaution is not necessary with the Smart-On command.

DIRECT-ON MAIN [A5h]

The Direct-On Main command is typically used to activate the main 1-Wire output to subsequently issue a reset pulse and access a device residing on the segment of the MicroLAN connected to the Main output of the DS2409. If this command is received, the DS2409 will automatically set the auxiliary output to inactive. Depending on the currently valid device status settings, the transistor at the control output may change state (see Status Read/Write command).

SMART-ON MAIN [CCh]

When analyzing huge MicroLAN networks for changes in population it may be useful to limit the number of devices participating in a Search ROM command. The smaller the number of participants, the faster the responding devices are identified. The DS2409 supports the bus master in this process with the Smart-On Main command. As a preparation for the subsequent steps, the first action of the Smart-On Main command is deactivating the main output.

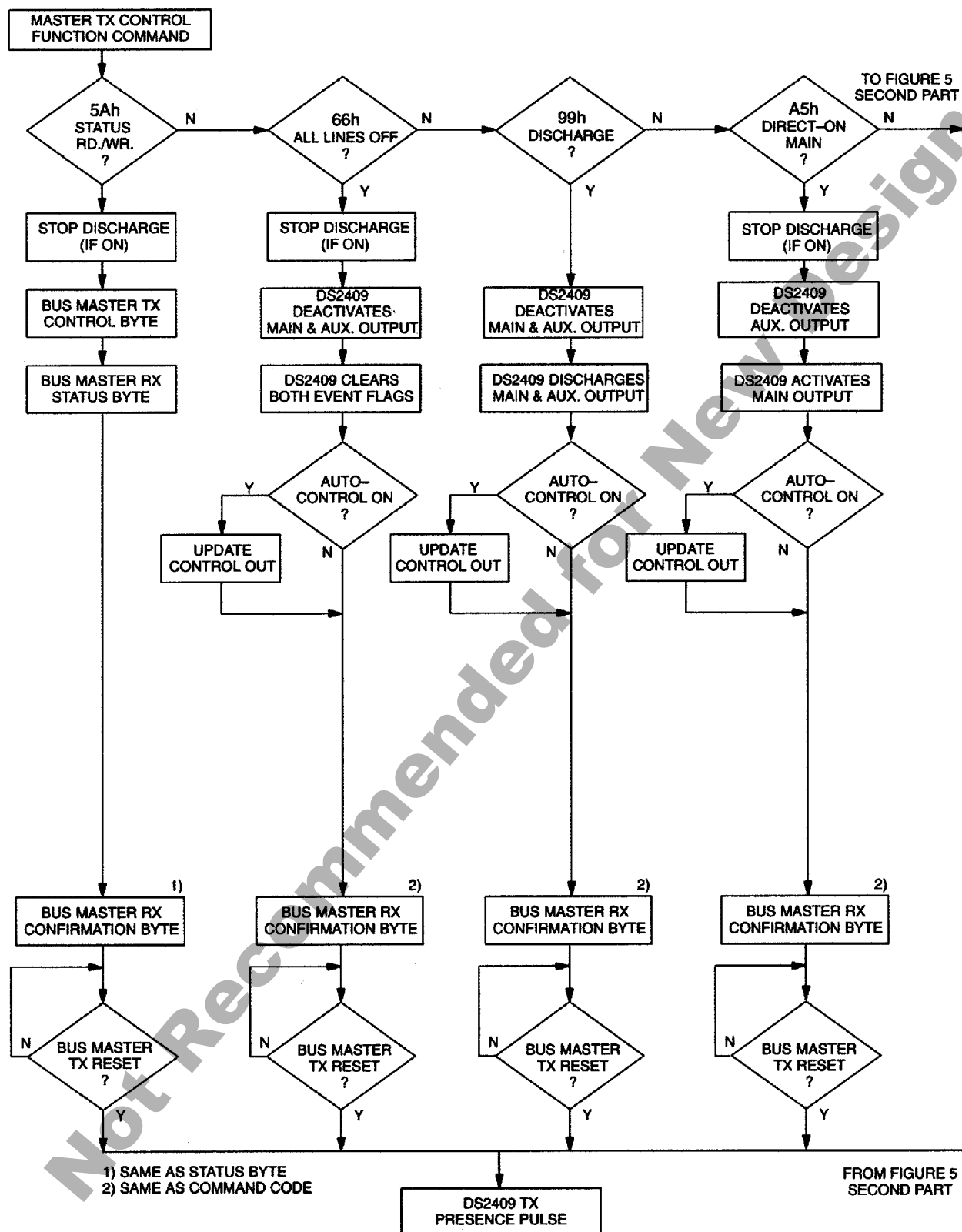
Compared to the Direct-On Main command, the Smart-On Main requires the bus master to follow the function command with 16 more time slots. The first 8 time slots (reset stimulus) are translated by the DS2409 as a reset low time on the Main 1-Wire output. Now, the bus master reads the reset response byte. This generates the reset high time where devices connected to the Main 1-Wire output may assert their presence pulse. If a presence pulse was found, several of the most significant bits of the reset response byte will be zeros. After these 16 time slots are completed the Main 1-Wire output will be activated (= through-connected to the 1-Wire input of the DS2409). Now, only the devices on the newly activated segment of the MicroLAN are ready to receive a ROM function command optionally followed by a memory function command. All other devices in the network will remain silent until the next reset pulse is issued.

As with the Direct-On command, the Smart-On Main command will automatically set the auxiliary output to inactive. Depending on the currently valid device status settings, the transistor at the control output may change state (see Status Read/Write command). If the Smart-On Main command is terminated by a 1-Wire reset pulse while receiving the reset stimulus, the DS2409 will immediately turn off the pulldown transistor and let the output line go high.

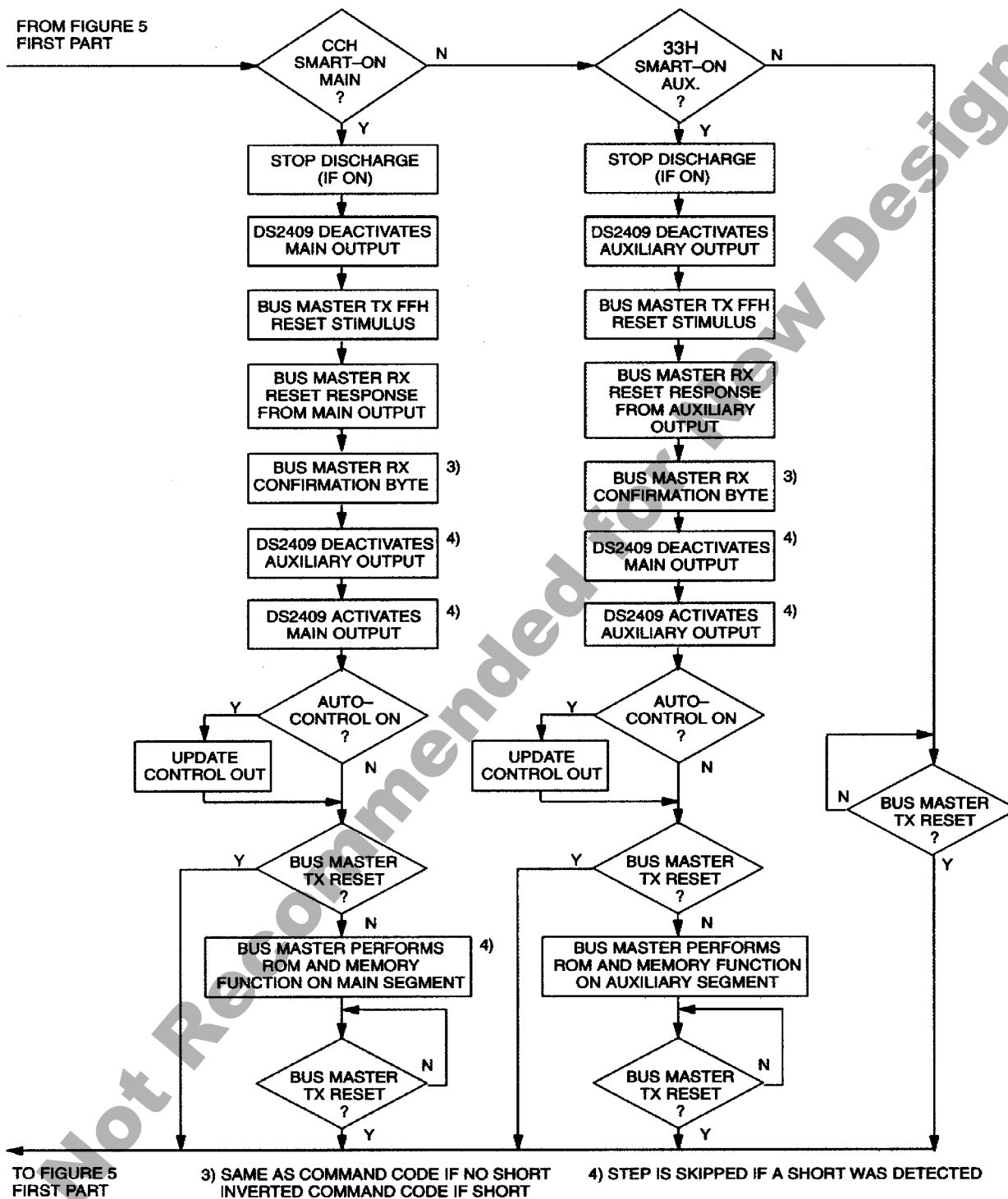
SMART-ON AUXILIARY [33h]

This command works essentially the same way as the Smart-On Main command, but it affects the auxiliary 1-Wire output. After the reset response byte is received by the bus master, the auxiliary output is activated and the main output becomes inactive. Depending on the currently valid device status settings, the transistor at the control output may change state (see Status Read/Write command).

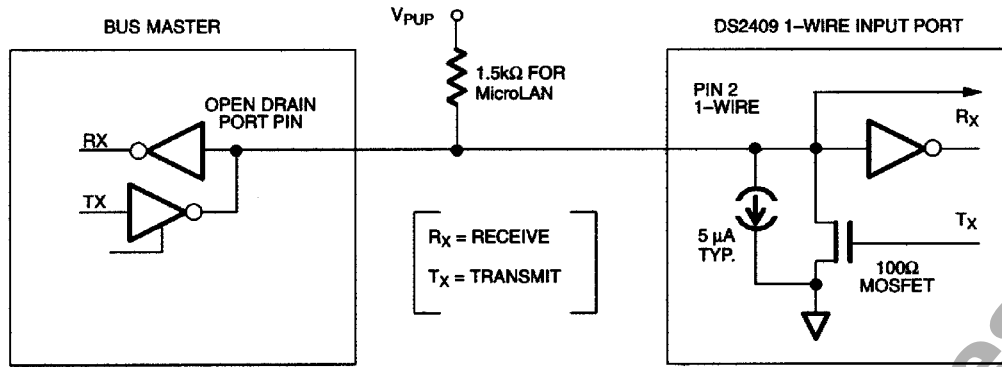
FUNCTION COMMAND FLOW CHART Figure 5



FUNCTION COMMAND FLOW CHART Figure 5 (cont'd)



HARDWARE CONFIGURATION Figure 6



1-WIRE BUS SYSTEM

The 1-Wire bus is a system which has a single bus master and one or more slaves. In all instances the DS2409 behaves as a slave. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). A 1-Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx iButton Standards.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or 3-state outputs. The 1-Wire input of the DS2409 is open drain with an internal circuit equivalent to that shown in Figure 6. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 16.3kbits per second and requires a pullup resistor of approximately 1.5kΩ or a DS2480 driver for MicroLAN applications.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120μs, one or more of the devices on the bus may be reset. The DS2409 may perform a power-on reset cycle and deactivate both 1-Wire outputs if the 1-Wire input is low for minimum 8ms. A low time of 12ms or more will always cause a power-on reset cycle.

Transaction Sequence

The protocol for accessing the DS2409 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Control Function Command

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS2409 is on the bus and is ready to operate. For more details, see the “1-Wire Signaling” section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the five ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 7):

Read ROM [33h]

This command allows the bus master to read the DS2409's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2409 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number will usually result in a mismatch of the CRC.

Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2409 on a multidrop bus. Only the DS2409 that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with single or multiple devices on the bus.

Skip ROM [CCh]

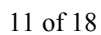
This command can save time in a single drop bus system by allowing the bus master to access the control functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx iButton Standards for a comprehensive discussion of a search ROM, including an actual example.

Conditional Search ROM [ECh]

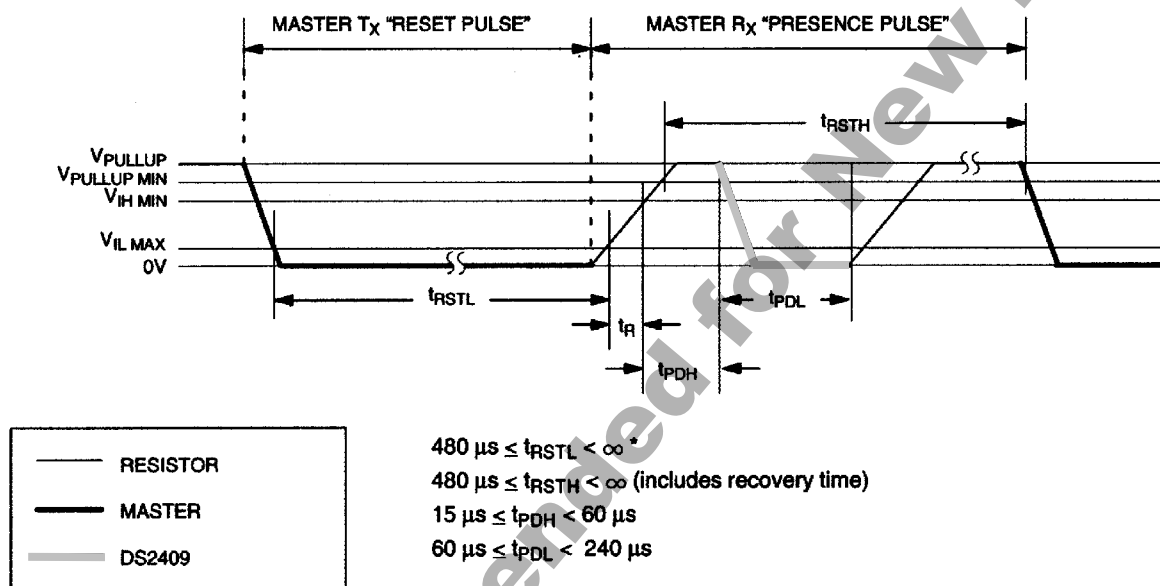
This ROM command works exactly as the normal ROM Search, but it will identify only devices that encounter certain conditions. The DS2409 will respond to this command only if the event flag for the main output is set (see Status Read/Write command). The event flag is cleared with the All Lines Off command.



1-WIRE SIGNALING

The DS2409 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1 and Read Data. All these signals except presence pulse are initiated by the bus master. The initialization sequence required to begin any communication with the DS2409 is shown in Figure 8. A reset pulse followed by a presence pulse indicates the DS2409 is ready to send or receive data given the correct ROM command and control function command. The bus master transmits (TX) a reset pulse (t_{RSTL} , minimum 480 μ s). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pullup resistor. After detecting the rising edge on the data line, the DS2409 waits (t_{PDH} , 15 μ s to 60 μ s) and then transmits the presence pulse (t_{PDL} , 60 μ s to 240 μ s).

INITIALIZATION PROCEDURE “RESET AND PRESENCE PULSES” Figure 8



*In order not to mask interrupt signaling by other devices on the 1-Wire bus, $t_{RSTL} + t_R$ should always be less than 960 μ s.

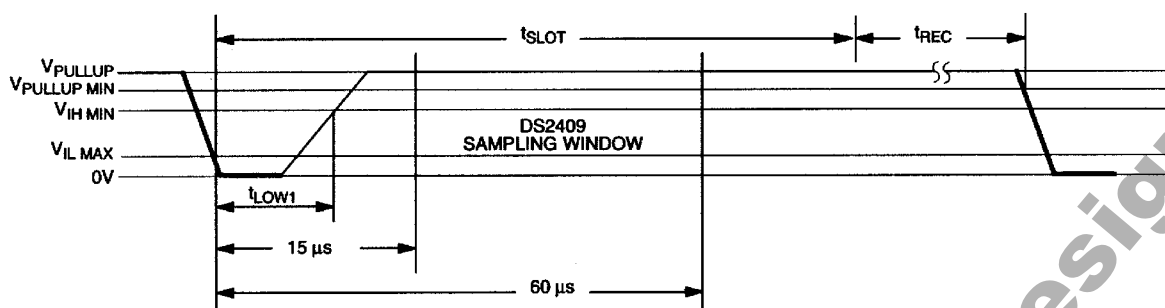
**The slew rate of the Presence Pulse is actively limited by the DS2409 to 1V/ μ s typically to minimize ringing. The slope of all other edges is controlled by the 1-Wire bus driver at the host.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 9. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2409 to the master by triggering a delay circuit in the DS2409. During write time slots, the delay circuit determines when the DS2409 will sample the data line. For a read data time slot, if a “0” is to be transmitted, the delay circuit determines how long the DS2409 will hold the data line low overriding the 1 generated by the master. If the data bit is a “1”, the device will leave the read data time slot unchanged.

READ/WRITE TIMING DIAGRAM Figure 9

Write—one Time Slot

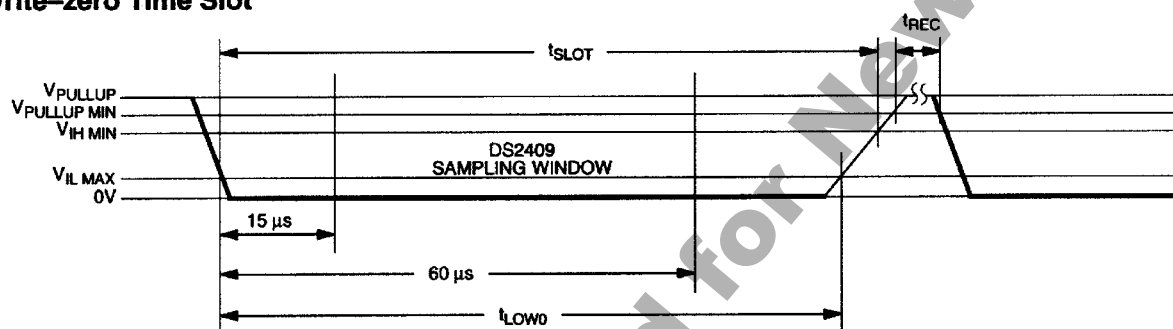


$$60\ \mu s \leq t_{SLOT} < 120\ \mu s$$

$$1\ \mu s \leq t_{LOW1} < 15\ \mu s$$

$$1\ \mu s \leq t_{REC} < \infty$$

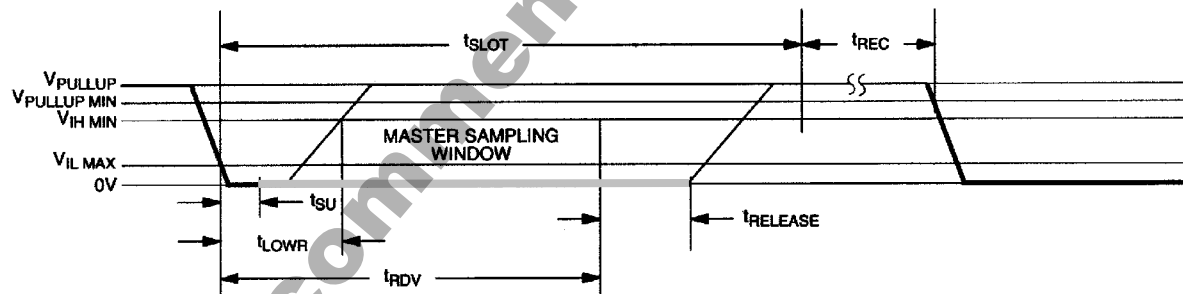
Write—zero Time Slot



$$60\ \mu s \leq t_{LOW0} < t_{SLOT} < 120\ \mu s$$

$$1\ \mu s \leq t_{REC} < \infty$$

Read—data Time Slot



$$60\ \mu s \leq t_{SLOT} < 120\ \mu s$$

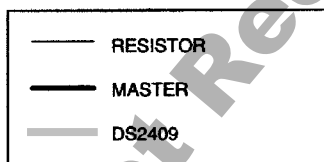
$$1\ \mu s \leq t_{LOW1} < 15\ \mu s$$

$$0 \leq t_{RELEASE} < 45\ \mu s$$

$$1\ \mu s \leq t_{REC} < \infty$$

$$t_{RDV} = 15\ \mu s$$

$$t_{SU} < 1\ \mu s$$



USAGE EXAMPLE

Configuration: A bus master controls a MicroLAN consisting of a trunk with many DS2409s that create branches. Each of the DS2409s has a DS2430A connected to its auxiliary output to label its physical location in the network (see Figure 10). iButton devices are constantly arriving at or departing from the branches.

Task: Identify one branch where an iButton has arrived and get the branch's physical location. Determine the population on that particular branch.

STEP	MASTER MODE	DATA (LSB FIRST)	COMMENTS
1	TX	Reset	Reset pulse (480µs to 960µs)
2	RX	Presence	Presence pulse
3	TX	ECh	Issue "conditional search ROM" command
4	RX/RX/TX	for each of the 64 ROM bits	Identify and access one of the qualifying devices
5	TX	33h	Issue Smart-On Auxiliary command
6	TX	FFh	Send reset stimulus
7	RX	<data byte>*	Get reset response byte with presence info
8	RX	33h	Get confirmation byte
9	TX	CCh	Issue "skip ROM" command
10	TX	F0h	Issue "read memory" command
11	RX	<32 data bytes>	Get branch location information (DS2430A)
12	TX	Reset	Reset pulse
13	RX	Presence	Presence pulse
14	TX	55h	Issue "Match ROM" command
15	TX	<8 byte ROM ID>	Access the previously identified coupler
16	TX	CCh	Issue Smart-On Main command
17	TX	FFh	Send reset stimulus
18	RX	<data byte>*	Get reset response byte with presence info
19	RX	CCh	Get confirmation byte
20	TX	F0h	Issue "search ROM" command
21	RX/RX/TX	for each of the 64 ROM bits	Identify one of the devices connected
22	TX	Reset	Reset pulse
23	RX	Presence	Presence pulse
24	TX	55h	Issue "Match ROM" command
25	TX	<8 byte ROM ID>	Access the previously identified coupler
26	TX	66h	Send all lines off command
27	RX	66h	Get confirmation byte
28	TX	Reset	Reset pulse
29	RX	Presence	Presence pulse
repeat steps 12 to 21 for each of the remaining devices on the branch of the identified coupler			

* 00h or 01h if presence pulse, FFh if no presence pulse

NOTE:

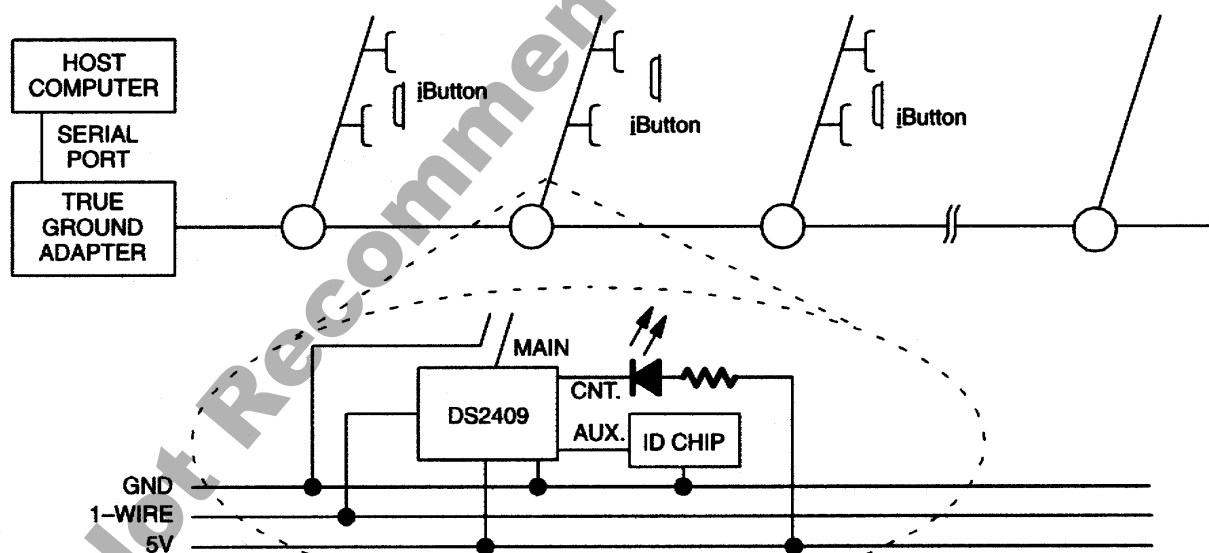
The sequence of steps 12 to 21 logically decouples all other devices residing on the trunk from responding to the search ROM command. The All Lines Off command is required to clear the event flag that made the device respond to the conditional search command.

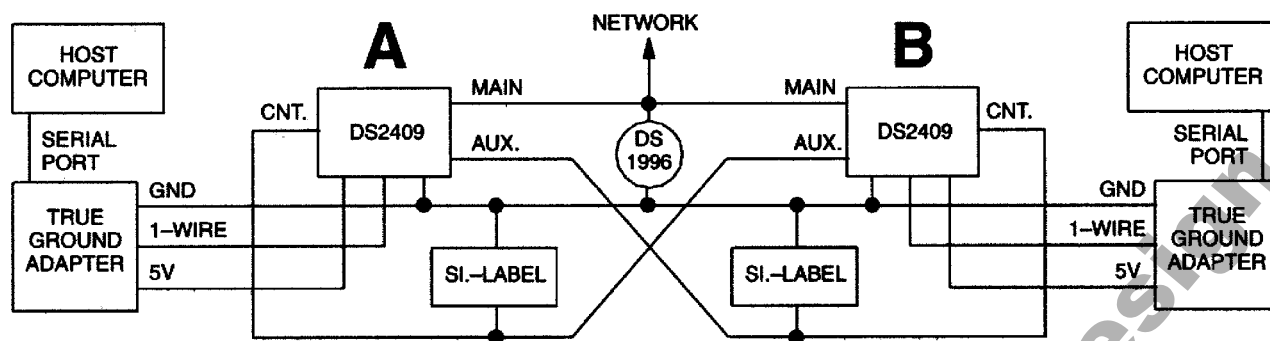
APPLICATION EXAMPLES

Figures 10 and 11 show two application examples of the DS2409 MicroLAN Coupler. A single trunk with branches is the typical topology of an access control system with the iButtons being the electronic keys required for admittance. The host computer runs a program that scans the devices on the trunk for events (conditional search). When somebody touches the probe with an iButton, this will set the event flag of the main line and the coupler will respond. The ID chip represents the DS2430A that labels the access point. The 64-bit ROM ID of the arriving iButton is the key for the entrance. In a real access control application, the LED will be replaced by a solenoid that opens the lock under software control (manual mode). The same network topology could be used for an inventory control system with the branches representing individual shelves of a rack. The iButtons would be electronic tags mounted on objects sitting on the shelves. The LED would guide the warehouse worker in placing the objects onto the right shelf.

The dual-master system realizes a master to master communication path via the 1-Wire bus. The DS1996 Memory iButton serves as a temporary storage for the data packets to be exchanged. When idle, both main outputs as well as the auxiliary outputs are inactive. To access the Memory iButton, the host A first switches on the control output, thereby pulling the auxiliary line of the coupler at the B side low. This tells host B that it is not allowed to activate the main output of coupler B. Now, host A activates the main output of coupler A and writes data to the Memory iButton. After the writing is complete, host A deactivates the main output of coupler A and switches off the control output. Host B, meanwhile, has been polling the logic level at the auxiliary line of coupler B and realizes that host A has finished the access. Now, host B follows the same procedure and accesses the memory to read the data, etc. The memory iButton may be replaced by a MicroLAN network. The Silicon Label stores information telling the hosts that these particular couplers access the same network and that the control and auxiliary outputs are cross-coupled for handshaking.

MicroLAN TRUNK WITH BRANCHES Figure 10



DUAL MASTER SYSTEM Figure 11

ABSOLUTE MAXIMUM RATINGS*

Voltage on Data to Ground	-0.5V to +7.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C, $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 (1-Wire In)	V_{IH1}	2.2		V_{DD}	V	1
Logic 0 (1-Wire In)	V_{IL1}	-0.3		+0.8	V	1
Output Logic Low @ 4 mA (1-Wire In)	V_{OL1}			0.4	V	1
Output Logic High (1-Wire In)	V_{OH1}			V_{PUP}	V	1, 3
Input Load Current (1-Wire In)	I_{L1}		5		μA	4
Logic 1 (Main Out)	V_{IHM}	2.2			V	1
Logic 0 (Main Out)	V_{ILM}	-0.3		+0.8	V	1
Output Sink Current @ 0.4V (Main Out)	I_{SM}		10		mA	1, 8
Logic 1 (Aux. Out)	V_{IHA}	2.2			V	1
Logic 0 (Aux. Out)	V_{ILA}	-0.3		+0.8	V	1
Output Sink Current @ 0.4V (Aux. Out)	I_{SA}		10		mA	1
Output Leakage (Control Output)	I_{LOC}			1	μA	
Current @ 0.4V (Control Output)	I_{OLC}		10		mA	
Operating Current	I_{DD}			50	μA	2
Quiescent Current	I_{DDQ}			25	μA	2

CAPACITANCE ($t_A = 25^\circ C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance 1-Wire In	C_{IN1}			50	pF	
Capacitance Main Out	C_{INM}			50	pF	
Capacitance Aux. Out	C_{INA}			50	pF	

RESISTANCES (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
1-Wire In to Main ON Res.	Z_{MON}		10	20	Ω	
1-Wire In to Aux. ON Res.	Z_{AON}		15	30	Ω	
Main and Aux. Pullup Res.	R_{PU}		1.5		k Ω	

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C, $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	μs	
Write 1 Low Time	t_{LOW1}	1		15	μs	10
Write 0 Low Time	t_{LOW0}	60		120	μs	
Read Low Time	t_{LOWR}	1		15	μs	10
Read Data Valid	t_{RDV}		15		μs	9
Release Time	$t_{RELEASE}$	0	15	45	μs	
Read Data Setup	t_{SU}			1	μs	6
Recovery Time	t_{REC}	1			μs	
Reset Time High	t_{RSTH}	480			μs	5
Reset Time Low	t_{RSTL}	480		960	μs	7
Presence Detect High	t_{PDH}	15		60	μs	
Presence Detect Low	t_{PDL}	60		240	μs	

NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{PUP} = external pullup voltage.
4. Input load is to ground.
5. An additional reset or communication sequence cannot begin until the reset high time has expired.
6. Read data setup time refers to the time the bus master must pull the I/O line low to read a bit. Data is guaranteed to be valid within 1 μs of this falling edge.
7. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 μs , to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses. The DS2409 may perform a power-on reset cycle and deactivate both 1-Wire outputs if the 1-Wire input is low for minimum 8 ms. A low time of 12 ms or more will always cause a power-on reset cycle.
8. The main output has a slew rate controlled output. The indicated current is a DC value. The sink current typically reaches 80% of its DC value 1 μs after turning on the transistor.
9. The optimal sampling point for the master is as close as possible to the end time of the 15 μs t_{RDV} period without exceeding t_{RDV} . For the case of a Read-One Time Slot, this maximizes the amount of time for the pull-up resistor to recover to a high level. For a Read-Zero Time Slot, it ensures that a read will occur before the fastest 1-Wire device(s) release the line.
10. The duration of the low pulse sent by the master should be a minimum of 1 μs with a maximum value as short as possible to allow time for the pull-up resistor to recover the line to a high level before the 1-Wire device samples in the case of a Write-One Time or before the master samples in the case of a Read-One Time.