ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089

NTE3093
Optoisolator
NPN Split Darlington Output

Description:

The NTE3093 coupler uses a light emitting diode (LED) and an integrated high gain photon detector to provide 3000V DC electrical insulation, 500V/µs common mode transient immunity and extremely high current transfer ratio between inut and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired, the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

Features:

- High Current Transfer Ratio
- Low Input Current Requirement
- TTL Compatible Output
- 3000V DC Withstand Test Voltage
- High Common Mode Rejection
- Base Access Allows Gain Bandwidth Adjustment
- High Output Current
- DC to 1Mbit/s Operation

Absolute Maximum Ratings: (T_A = +25°C unless otherwise specified)

Input Diode

Reverse Voltage, V_R 5V
Peak Current (50% Duty Cycle,1ms Pulse Width), I_F 40mA
Peak Transient Current (≤ 1µs Pulse Width, 300pps), I_F 20mA
Power Dissipation, P_D 35mW
Derate Linearly Above 50°C . . . . 0.7mW/°C

Output Transistor

Current (Pin6), I_O 60mA
Derate Linearly Above 25°C . . . . 0.7mA/°C
Emitter–Base Reverse Voltage (Pin5–7) 0.5V
Supply Voltage (Pin8–5), V_{CC} . . . . –0.5 to 18V
Output Voltage (Pin6–5), V_O . . . . –0.5 to 18V
Power Dissipation, P_D 35mW
Derate Linearly Above 50°C . . . . 0.7mW/°C

Total Device

Operating Temperature Range, T_{opr} . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . –55° to +125°C
Lead Temperature (During Soldering, 1.6mm below seating plane, 10sec Max), T_L . . . . . . +260°C

Note 1. The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degredation which may be induced by ESD.

Electrical Characteristics: (T_A = 0° to +70°C, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Transfer Ratio	CTR	I_F = 0.5mA, V_O = 0.4V, V_{CC} = 4.5V, Note 3, Note 4	400	800	–	%
		I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V, Note 3, Note 4	500	900	–	%
Logic Low Output Voltage	V_{OL}	I_F = 1.6mA, I_O = 6.4mA, V_{CC} = 4.5V, Note 4	–	0.1	0.4	V
		I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V, Note 4	–	0.1	0.4	V
		I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V, Note 4	–	0.2	0.4	V
Logic High Output Current	I_{OH}	I_F = 0, V_O = V_{CC} = 18V, Note 4	–	0.05	100	μA
Logic Low Supply Current	I_{CCL}	I_F = 1.6mA, V_O = Open, V_{CC} = 5V, Note 4	–	0.2	–	mA
Logic High Supply Current	I_{CCH}	I_F = 0mA, V_O = Open, V_{CC} = 5V, Note 4	–	10	–	nA
Input Forward Voltage	V_F	I_F = 1.6mA, T_A = +25°C	–	1.4	1.7	V
Input Reverse Breakdown Voltage	$V_{(BR)R}$	I_F = 10μA, T_A = +25°C	5	–	–	V
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	I_F = 1.6mA	–	–1.8	–	mV/°C
Input Capacitance	C_{IN}	f = 1MHz, V_F = 0	–	60	–	pF
Input–Output Insulation Leakage Currnt	I_{IO}	45% Relative Humidity, T_A = +25°C, t = 5s, V_{IO} = 3KVdc, Note 5	–	–	1.0	μA
Resistance	R_{IO}	V_{IO} = 500Vdc, Note 5	–	10^{11}	–	Ω
Capacitance	C_{IO}	f = 1MHz, Note 5	–	0.6	–	pF

Note 2. All typicals at T_A = +25°C, V_{CC} = 5V unless otherwise specified.

Note 3. DC Current Transfer Ratio is defined as the ratio of output collector current (I_O) to the forward LED input current (I_F) times 100%.

Note 4. Pin7 Open.

Note 5. Device considered a two–terminal device (Pins 1, 2, 3 and 4 shorted together and Pins 5, 6, 7 and 8 shorted together).

Switching Characteristics: (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time	t_{PHL}	I_F = 0.5mA, R_L = 4.7kΩ, Note 3, Note 6	–	5	25	μs
		I_F = 12mA, R_L = 270Ω, Note 3, Note 6	–	0.2	1.0	μs
	t_{PLH}	I_F = 0.5mA, R_L = 4.7kΩ, Note 3, Note 6	–	5	60	μs
		I_F = 12mA, R_L = 270Ω, Note 3, Note 6	–	1	7	μs
Common Mode Transient Immunity	CM_H	I_F = 0, R_L = 2.2kΩ, R_{CC} = 0, $\lvert V_{CM}\rvert$ = $10V_{P-P}$, Note 7, Note 8	–	500	–	V/μs
	CM_L	I_F = 1.6mA, R_L = 2.2kΩ, R_{CC} = 0, $\lvert V_{CM}\rvert$ = $10V_{P-P}$, Note 7, Note 8	–	–500	–	V/μs

Note 3. DC Current Transfer Ratio is defined as the ratio of output collector current (I_O) to the forward LED input current (I_F) times 100%.

Note 6. Use of a resistor between Pin5 and Pin7 will decrease gain abd delay time.

Note 7. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dv cm/dt on the leading edge of the common mode pulse (V_{CM}) to assure that the output will remain in a Logic High state (i.e. V_O 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dc cm/dt on the trailing edge of the common mode pulse signal (V_{CM}) to assure that the output will remain in a Logic Low state (i.e. V_O 0.8V).

Note 8. In applications where dV/dt may exceed 50,000V/μs (such as static discharge) a series resistor (R_{CC}) should be included to protect the detector IC from destructively high surge currents. The recommended value is:

$$R_{CC} = \frac{1V}{0.15\ I_F\ (mA)}\ k\Omega$$

Pin Connection Diagram