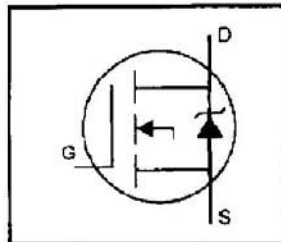


IRF840LCPbF

HEXFET® Power MOSFET

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V V_{GS} Rating
- Reduced C_{iss} , C_{oss} , C_{rss}
- Extremely High Frequency Operation
- Repetitive Avalanche Rated
- Lead-Free



$$V_{DS} = 500V$$

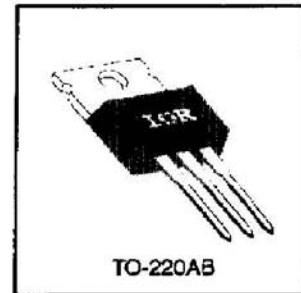
$$R_{DS(on)} = 0.85\Omega$$

$$I_D = 8.0A$$

Description

This new series of Low Charge HEXFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new Low Charge MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristic of HEXFETs offer the designer a new standard in power transistors for switching applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	8.0	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	5.1	
I_{DM}	Pulsed Drain Current $\textcircled{1}$	28	
$P_D @ T_C = 25^\circ C$	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	-30	V
E_{AS}	Single Pulse Avalanche Energy $\textcircled{2}$	510	mJ
A_R	Avalanche Current $\textcircled{3}$	8.0	A
E_{AR}	Repetitive Avalanche Energy $\textcircled{2}$	13	mJ
dv/dt	Peak Diode Recovery dv/dt $\textcircled{4}$	3.5	V/ns
T_J	Operating Junction and	-55 to +150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw	10 lbf-in (1.1 N-m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	500	—	—	V	$V_{GS}=0V$, $I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	—	0.63	—	V/°C	Reference to 25°C , $I_D=1mA$
$R_{DS(on)}$	—	—	0.85	Ω	$V_{GS}=10V$, $I_D=4.8A$ ①
$V_{GS(th)}$	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
g_{fs}	4.0	—	—	S	$V_{DS}=50V$, $I_D=4.8A$ ②
I_{DSS}	—	—	25	μA	$V_{DS}=500V$, $V_{GS}=0V$
I_{GSS}	—	—	250	μA	$V_{DS}=400V$, $V_{GS}=0V$, $T_J=125^\circ\text{C}$
	—	—	100	nA	$V_{GS}=20V$
	—	—	-100	nA	$V_{GS}=-20V$
Q_g	—	—	39	nC	$I_D=8.0A$
Q_{gs}	—	—	10	nC	$V_{DS}=400V$
Q_{gd}	—	—	19	nC	$V_{GS}=10V$ See Fig. 5 and 13 ③
$t_{(on)}$	—	12	—	ns	$V_{DD}=250V$
t_r	—	25	—	ns	$I_D=8.0A$
$t_{(off)}$	—	27	—	ns	$R_G=9.1\Omega$
t_f	—	19	—	ns	$R_D=30\Omega$ See Figure 10 ④
L_D	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	—	7.5	—	nH	
C_{iss}	—	1100	—	pF	$V_{GS}=0V$
C_{oss}	—	170	—	pF	$V_{DS}=25V$
C_{rss}	—	18	—	pF	$f=1.0MHz$ See Figure 5

Source-Drain Ratings and Characteristics

Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	—	—	8.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	—	—	28	A	
V_{SD}	—	—	2.0	V	$T_J=25^\circ\text{C}$, $I_S=8.0A$, $V_{GS}=0V$ ④
t_{rr}	—	490	740	ns	$T_J=25^\circ\text{C}$, $I_F=8.0A$
Q_{rr}	—	3.0	4.5	μC	$di/dt=100A/\mu s$ ③
t_{on}	—	—	—	—	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)

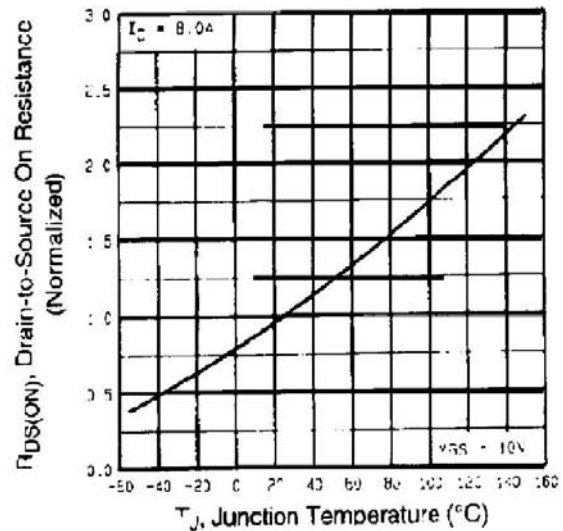
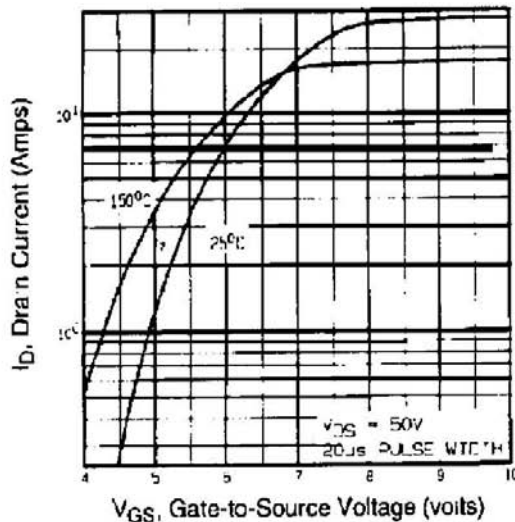
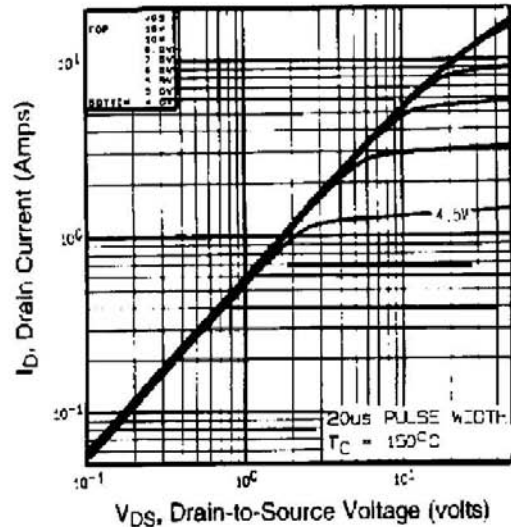
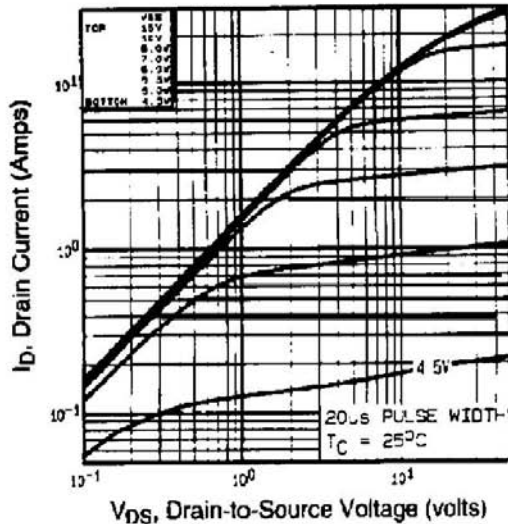
Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② $V_{DD}=50V$, starting $T_J=25^\circ\text{C}$, $L=14mH$, $R_G=25\Omega$, $I_{AS}=8.0A$ (See Figure 12)

③ $I_{SDS}=8.0A$, $di/dt \leq 100A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.



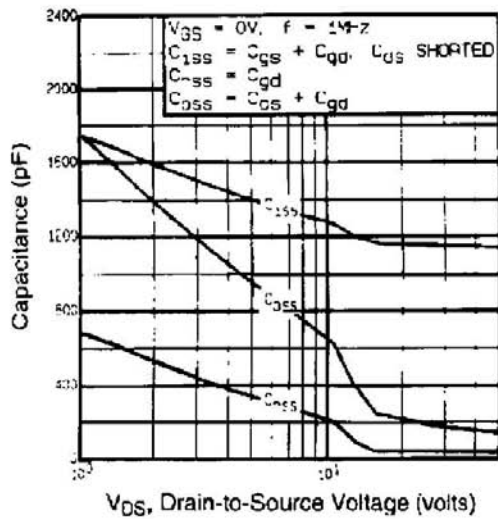


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

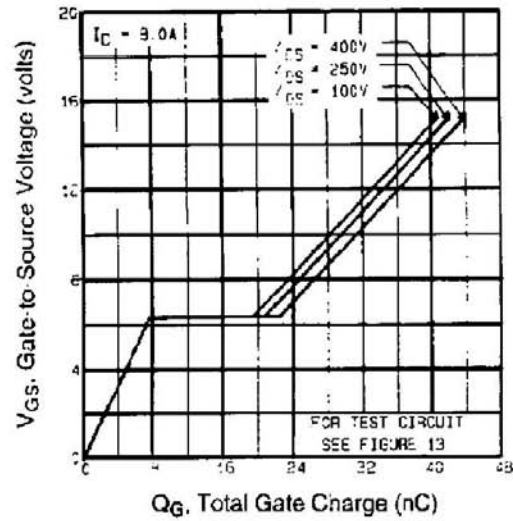


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

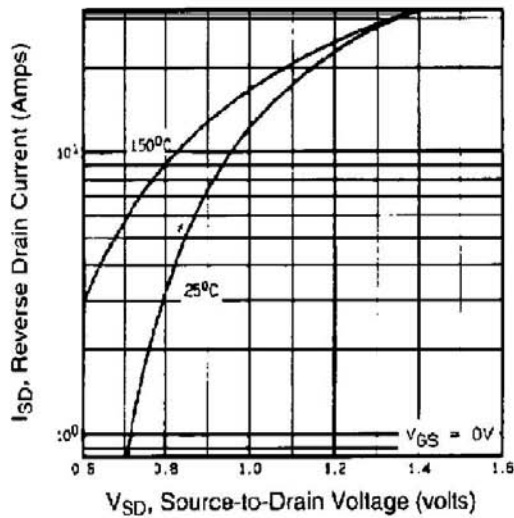


Fig 7. Typical Source-Drain Diode Forward Voltage

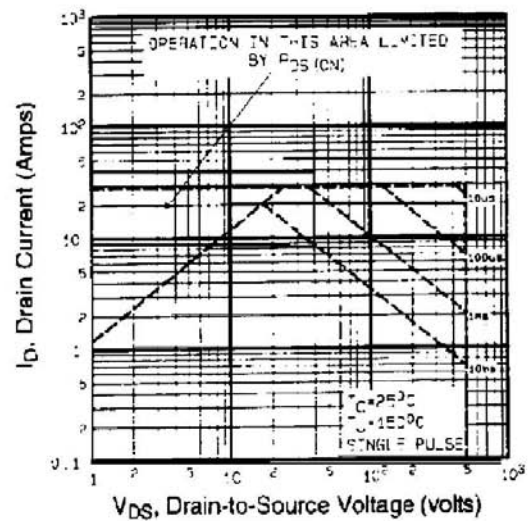


Fig 8. Maximum Safe Operating Area

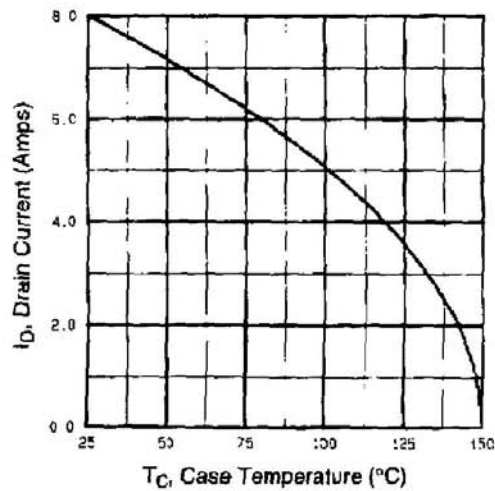


Fig 9. Maximum Drain Current Vs. Case Temperature

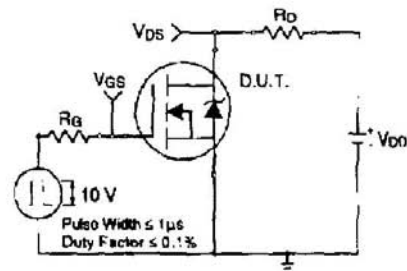


Fig 10a. Switching Time Test Circuit

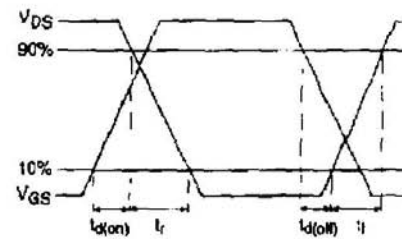


Fig 10b. Switching Time Waveforms

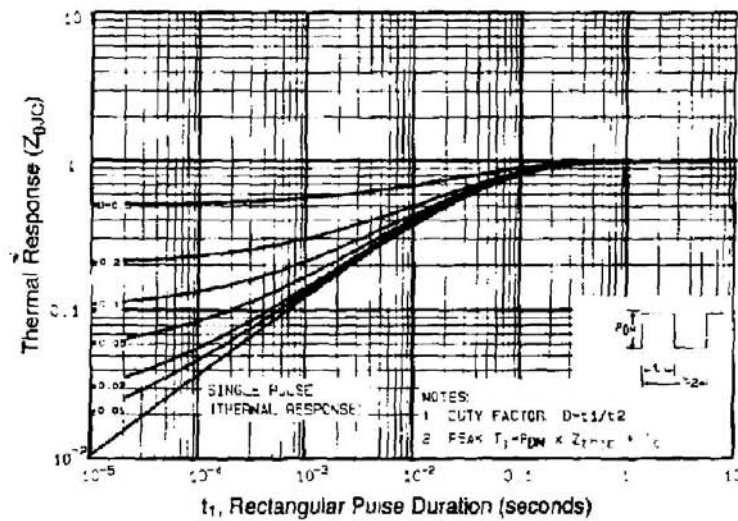


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

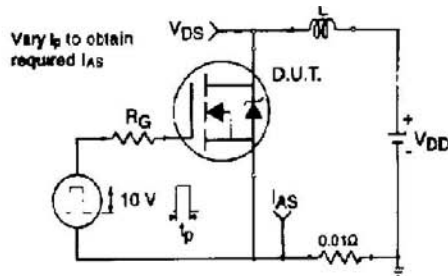


Fig 12a. Unclamped Inductive Test Circuit

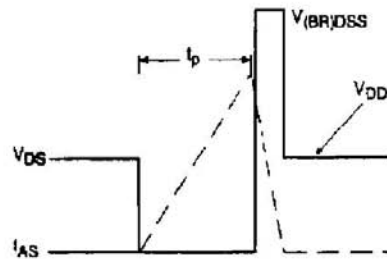


Fig 12b. Unclamped Inductive Waveforms

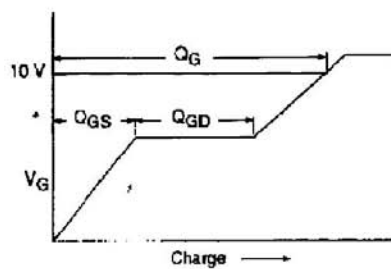


Fig 13a. Basic Gate Charge Waveform

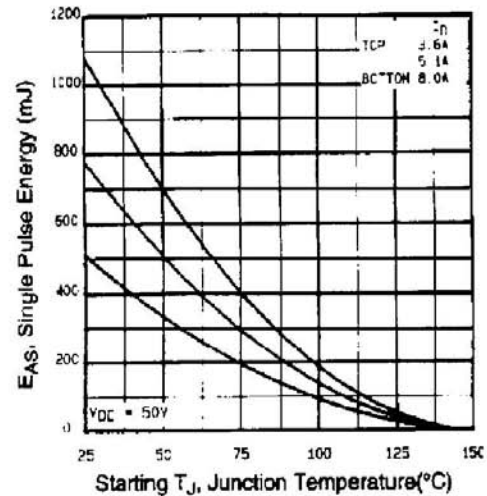


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

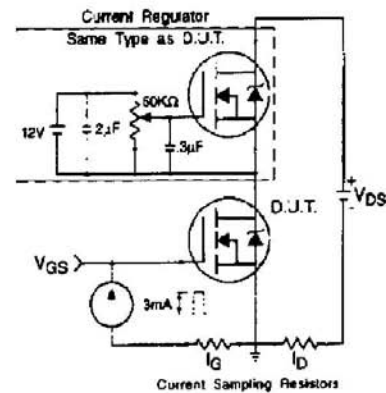


Fig 13b. Gate Charge Test Circuit

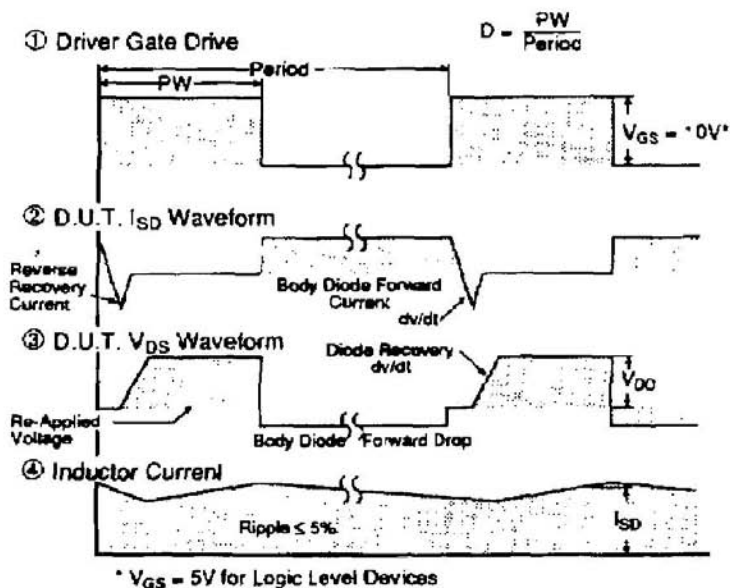
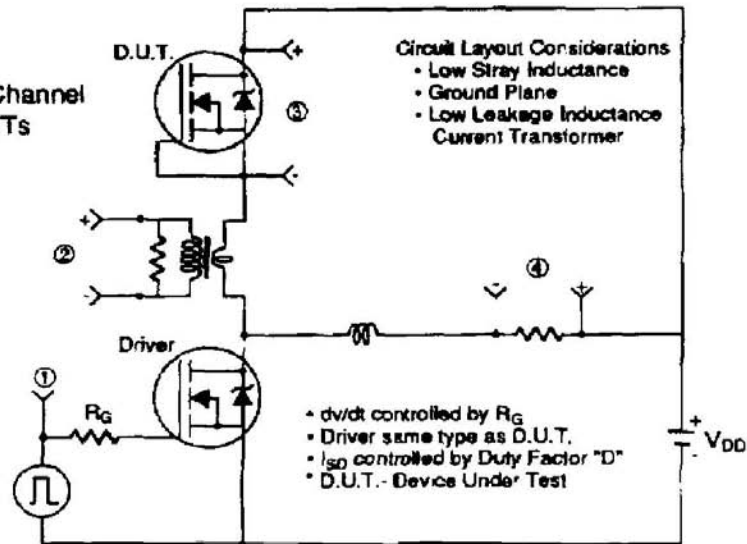
Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit

Appendix B: Package Outline Mechanical Drawing

Appendix A

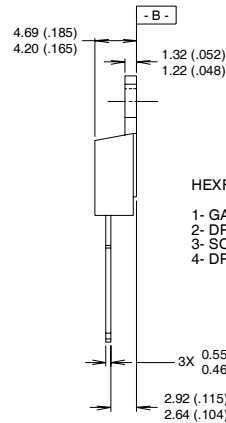
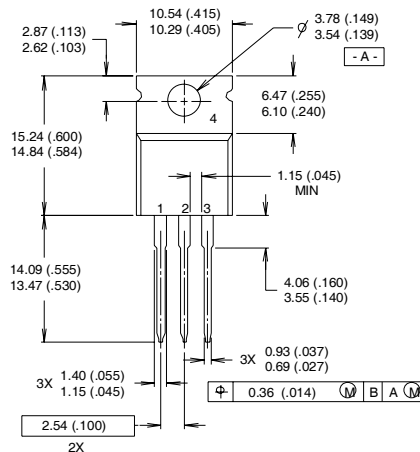
Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs



TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS	
HEXFET	IGBTs, CoPACK
1- GATE	1- GATE
2- DRAIN	2- COLLECTOR
3- SOURCE	3- EMITTER
4- DRAIN	4- COLLECTOR

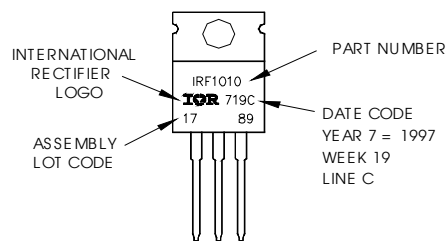
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line
position indicates "Lead-Free"



Data and specifications subject to change without notice.

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