3 V, Parallel Input
Micropower 10- and 12-Bit DACs

AD7392/AD7393

FEATURES

Micropower: 100 μA
0.1 μA typical power shutdown
Single-supply 2.7 V to 5.5 V operation
AD7392: 12-bit resolution
AD7393: 10-bit resolution
0.9 LSB differential nonlinearity error

APPLICATIONS

Automotive 0.5 V to 4.5 V output span voltage
Portable communications
Digitally controlled calibration
PC peripherals

GENERAL DESCRIPTION

The AD7392/AD7393 family of 10- and 12-bit voltage output digital-to-analog converters is designed to operate from a single 3 V supply. Built using a CBCMOS process, these monolithic DACs offer low cost and ease of use in single-supply 3 V systems. Operation is guaranteed over the supply voltage range of 2.7 V to 5.5 V, making this device ideal for battery-operated applications.

The full-scale voltage output is determined by the external reference input voltage applied. The rail-to-rail REF_{IN} to DAC_{OUT} allows a full-scale voltage equal to the positive supply V_{DD} or any value in between. The voltage outputs are capable of sourcing 5 mA.

A 12-bit-wide data latch loads with a 45 ns write time, eliminating wait states when interfacing to the fastest processors. Additionally, an asynchronous $\overline{RS}$ input sets the output to zero scale at power-on or upon user demand.
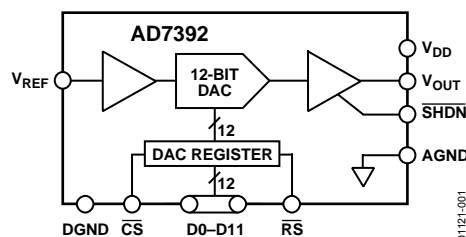
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

Both parts are offered with similar pinouts, which allows users to select the amount of resolution appropriate for their applications without changing the circuit card.

The AD7392/AD7393 are specified for operation over the extended industrial temperature range (−40°C to +85°C). The AD7393AR is specified for the automotive temperature range (−40°C to +125°C). The AD7392/AD7393 are available in 20-lead PDIP and SOIC packages.

For serial data input, 8-lead packaged versions, see the AD7390 and AD7391.

TABLE OF CONTENTS

REVISION HISTORY

6/04—Changed from Rev. A to Rev. B
Removed TSSOP...Universal
Changes to Ordering Guide 16

3/99—Changed from Rev. 0 to Rev. A

11/96—Revision 0: Initial Version

SPECIFICATIONS

AD7392 ELECTRICAL CHARACTERISTICS

At V_{RE} = 2.5 V, 240°C < T_A < 185°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	3 V ± 10%	5 V ± 6 10%	Unit
STATIC PERFORMANCE					
Resolution[1]	N		12	12	Bits
Relative Accuracy[2]	INL	T_A = +25°C	±1.8	±1.8	LSB max
		T_A = −40°C°, 185°C	±3	±3	LSB max
Differential Nonlinearity	DNL	T_A = +25°C, Monotonic	±0.9	±0.9	LSB max
		Monotonic	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 0x000, T_A = +25°C, +85°C	4.0	4.0	mV max
		Data = 0x000, T_A = −40°C	8.0	8.0	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = +25°C, +85°C, Data = 0xFFF	±8	±8	mV max
		T_A = −40°C, Data = 0xFFF	±20	±20	mV max
Full-Scale Tempco[3]	TCV_{FS}		28	28	ppm/°C typ
REFERENCE INPUT					
V_{REF} Range	V_{REF}		0/V_{DD}	0/V_{DD}	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Current (Source)	I_{OUT}	Data = 0x800, Δ V_{OUT} = 5 LSB	1	1	mA typ
Output Current (Sink)	I_{OUT}	Data = 0x800, Δ V_{OU} = 5 LSB	3	3	mA typ
Capacitive Load	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V max
Logic Input High Voltage	V_{IH}		V_{DD} − 0.6	V_{DD} − 0.6	V min
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 5]					
Chip Select Write Width	t_{CS}		45	45	ns min
Data Setup	t_{DS}		30	15	ns min
Data Hold	t_{DH}		20	5	ns min
Reset Pulse Width	t_{RS}		40	30	ns min
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 0x000 to 0xFFF to 0x000	0.05	0.05	V/µs typ
Settling Time[6]	t_S	To ±0.1% of Full Scale	70	60	µs typ
Shutdown Recovery Time	t_{SDR}			80	µs typ
DAC Glitch	Q	Code 0x7FF to 0x800 to 0x7FF	65	65	nV/s typ
Digital Feedthrough	Q		15	15	nV/s typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V dc + 1 V p-p, Data = 0x000, f = 100 kHz	−63	−63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7/5.5	2.7/5.5	V min/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, No Load	55/100	55/100	µA typ/max
Shutdown Supply Current	I_{DD-SD}	$\overline{SHDN}$ = 0, V_{IL} = 0 V, No Load	0.1/1.5	0.1/1.5	µA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load	300	500	µW max
Power Supply Sensitivity	PSS	Δ V_{DD} = ±5%	0.006	0.006	%/% max

[1] One LSB = V_{REF}/4096 V for the 12-bit AD7392.
[2] The first two codes (0x000, 0x001) are excluded from the linearity error measurement.
[3] These parameters are guaranteed by design and not subject to production testing.
[4] Typicals represent average readings measured at 25°C.
[5] All input control signals are specified with t_R = t_F = 2 ns (10% to 90% of 13 V) and timed from a voltage level of 1.6 V.
[6] The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

AD7393 ELECTRICAL CHARACTERISTICS

At $V_{REF\ IN}$ = 2.5 V, −40°C < T_A < 185°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	3 V ± 10%	5 V ± 10%	Unit
STATIC PERFORMANCE					
Resolution[1]	N		10	10	Bits
Relative Accuracy[2]	INL	T_A = +25°C	±1.75	±1.75	LSB max
		T_A = −40°C, +85°C, +125°C	±2.0	±2.0	LSB max
Differential Nonlinearity	DNL	Monotonic	±0.8	±0.8	LSB max
Zero-Scale Error	V_{ZSE}	Data = 0x000	9.0	9.0	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = +25°C, +85°C, +125°C, Data = 0x3FF	±32	±32	mV max
		T_A = −40°C, Data = 0x3FF	±42	±42	mV max
Full-Scale Tempco[3]	TCV_{FS}		28	28	ppm/°C typ
REFERENCE INPUT					
$V_{REF\ IN}$ Range	V_{REF}		0/V_{DD}	0/V_{DD}	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current (Source)	I_{OUT}	Data = 0x200, Δ V_{OUT} = 5 LSB	1	1	mA typ
Output Current (Sink)	I_{OUT}	Data = 0x200, Δ V_{OUT} = 5 LSB	3	3	mA typ
Capacitive Load	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V max
Logic Input High Voltage	V_{IH}		V_{DD} − 0.6	V_{DD} − 0.6	V min
Input Leakage Current	I_{IL}		10	10	μA max
Input Capacitance	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 5]					
Chip Select Write Width	t_{CS}		45	45	ns
Data Setup	t_{DS}		30	15	ns
Data Hold	t_{DH}		20	5	ns
Reset Pulse Width	t_{RS}		40	30	ns
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 0x000 to 0x3FF to 0x000	0.05	0.05	V/μs typ
Settling Time[6]	t_S	To ±0.1% of Full Scale	70	60	μs typ
Shutdown Recovery Time	t_{SDR}			80	μs typ
DAC Glitch	Q	Code 0x7FF to 0x800 to 0x7FF	65	65	nV/s typ
Digital Feedthrough	Q		15	15	nV/s typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V dc 11 V p-p, Data = 0x000, f = 100 kHz	−63	−63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL < ± 1 LSB	2.7/5.5	2.7/5.5	V min/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, No Load, T_A = +25°C	55	55	μA typ
		V_{IL} = 0 V, No Load	100	100	μA max
Shutdown Supply Current	$I_{DD−SD}$	$\overline{SHDN}$ = 0, V_{IL} = 0 V, No Load	0.1/1.5	0.1/1.5	μA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load	300	500	μW max
Power Supply Sensitivity	PSS	Δ V_{DD} = ±5%	0.006	0.006	%/% max

[1] One LSB = V_{REF}/1024 V for the 10-bit AD7393.
[2] The first two codes (0x000, 0x001) are excluded from the linearity error measurement.
[3] These parameters are guaranteed by design and not subject to production testing.
[4] Typicals represent average readings measured at 25° C.
[5] All input control signals are specified with t_R = t_F = 2 ns (10% to 90% of 13 V) and timed from a voltage level of 1.6 V.
[6] The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.
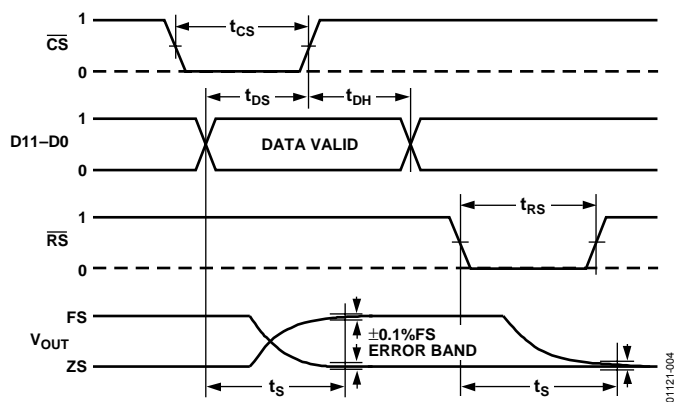
TIMING DIAGRAM

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V, +8 V
V_{REF} to GND	−0.3 V, V_{DD}
Logic Inputs to GND	−0.3 V, +V
V_{OUT} to GND	−0.3 V, V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND	50 mA
DGND to AGND	−0.3 V, +2 V
Package Power Dissipation	$(T_J\ max − T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}	
20-Lead PDIP Package (N 20)	57°C/W
20-Lead SOIC Package (R-20)	60°C/W
20-Lead Thin-Shrink Surface-Mount (RU-20)	155°C/W
Maximum Junction Temperature (T_J max)	150°C
Operating Temperature Range	−40°C to +85°C
AD7393AR	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
N-20 (Soldering, 10 sec)	300°C
R-20 (Vapor Phase, 60 sec)	215°C
RU-20 (Infrared, 15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

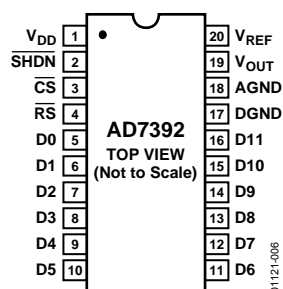# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 3. AD7392 Pin Configuration, Top View (Not to Scale)

NC = NO CONNECT

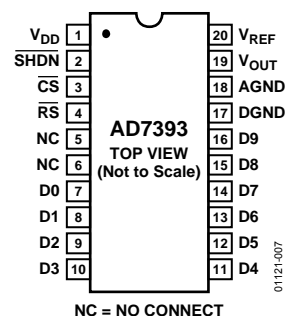Figure 4. AD7393 Pin Configuration, Top View (Not to Scale)

Table 4. AD7392 Pin Descriptions

Pin No.	Mnemonic	Function
1	V_{DD}	Positive Power Supply Input. The specified range of operation is 2.7 V to 5.5 V.
2	$\overline{SHDN}$	Power Shutdown Active Low Input. DAC register contents are saved as long as power stays on the V_{DD} pin. When $\overline{SHDN} = 0$, $\overline{CS}$ strobes write new data into the DAC register.
3	$\overline{CS}$	Chip Select Latch Enable, Active Low.
4	$\overline{RS}$	Asynchronous Active Low Input. Resets the DAC register to 0.
5 to 16	D0 to D11	Parallel Input Data Bits. D11 is the MSB; D0 is the LSB.
17	DGND	Digital Ground.
18	AGND	Analog Ground.
19	V_{OUT}	DAC Voltage Output.
20	V_{REF}	DAC Reference Input Pin. Establishes the DAC full-scale voltage.

Table 5. AD7393 Pin Descriptions

| Pin No.	Mnemonic	Function
1	V_{DD}	Positive Power Supply Input. The specified range of operation is 2.7 V to 5.5 V.
2	$\overline{SHDN}$	Power Shutdown Active Low Input. DAC register contents are saved as long as power stays on the V_{DD} pin. When $\overline{SHDN} = 0$, $\overline{CS}$ strobes write new data into the DAC register.
3	$\overline{CS}$	Chip Select Latch Enable, Active Low.
4	$\overline{RS}$	Asynchronous Active Low Input. Resets the DAC register to 0.
5, 6	NC	No Connect.
7 to 16	D0–D9	Parallel Input Data Bits. D9 is the MSB; D0 is the LSB.
17	DGND	Digital Ground.
18	AGND	Analog Ground.
19	V_{OUT}	DAC Voltage Output.
20	V_{REF}	DAC Reference Input Pin. Establishes the DAC full-scale voltage.

TYPICAL PERFORMANCE CHARACTERISTICS
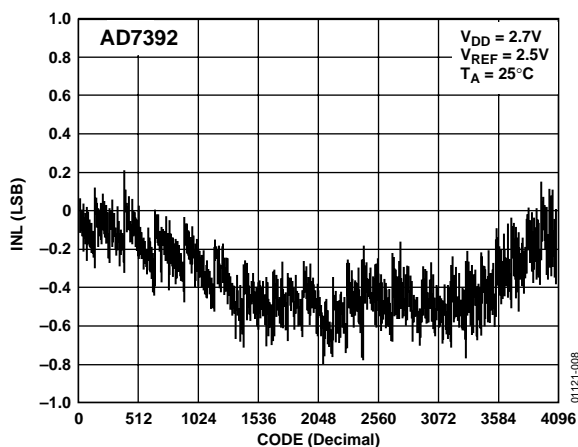
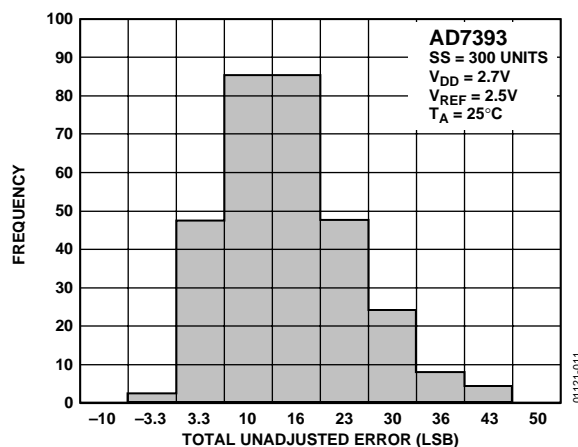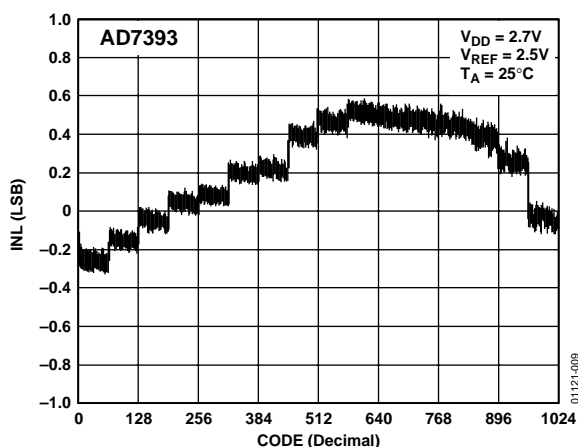Figure 5. AD7392 Integral Nonlinearity Error vs. Code

Figure 6. AD7393 Integral Nonlinearity Error vs. Code

Figure 7. AD7392 Total Unadjusted Error Histogram
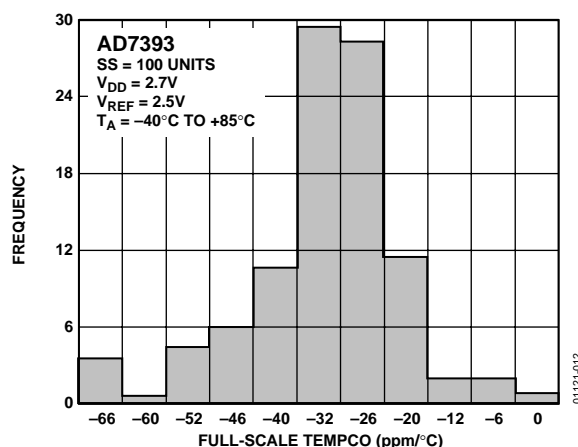

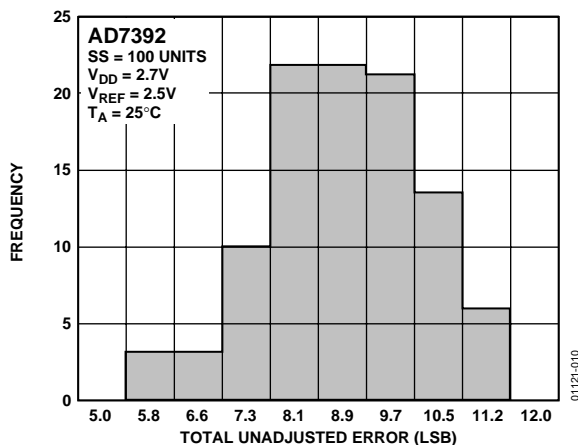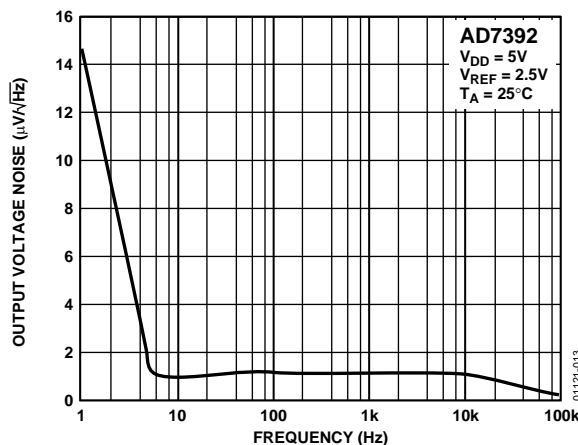Figure 8. AD7393 Total Unadjusted Error Histogram

Figure 9. AD7393 Full-Scale Output Tempco Histogram

Figure 10. Voltage Noise Density vs. Frequency
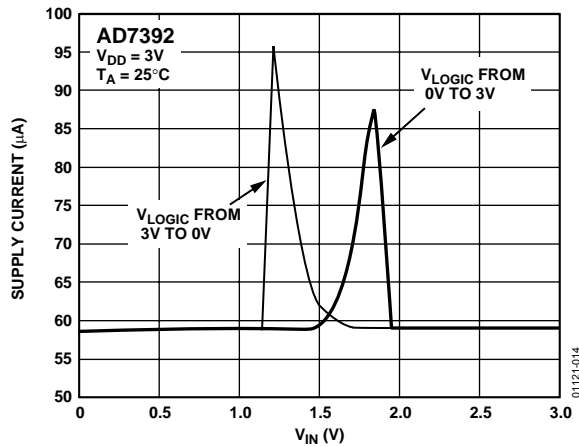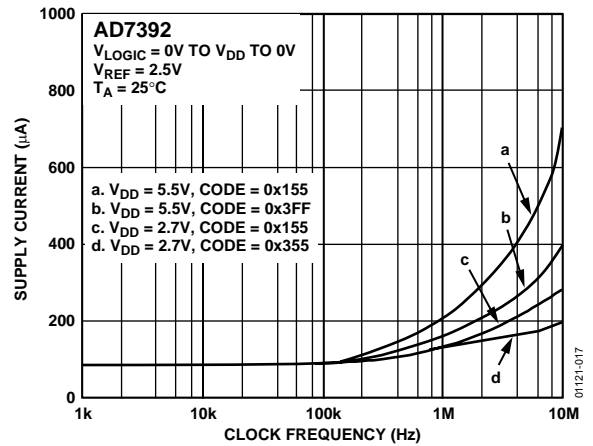
Figure 11. Supply Current vs. Logic Input Voltage

Figure 12. Logic Threshold vs. Supply Voltage

Figure 13. Supply Current vs. Temperature

Figure 14. Supply Current vs. Clock Frequency
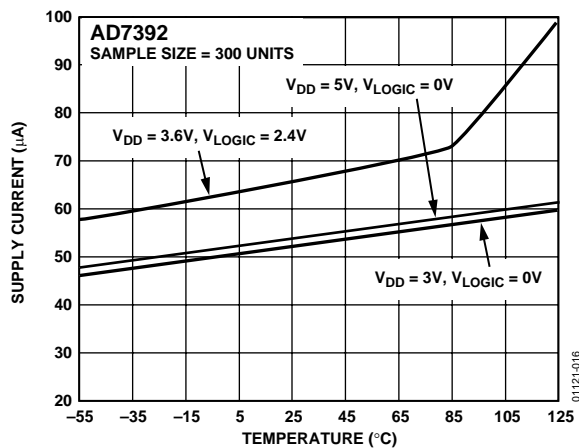

Figure 15. Power Supply Rejection vs. Frequency
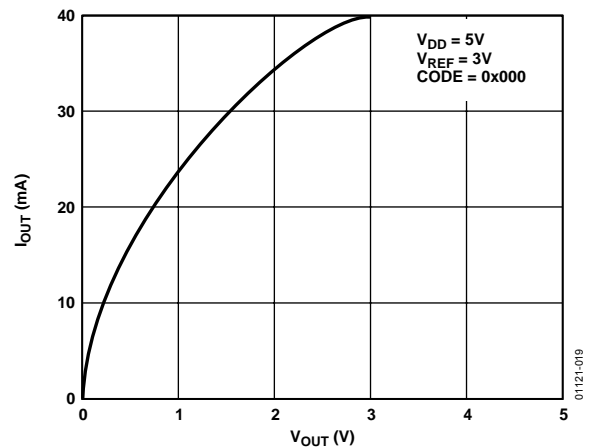
Figure 16. I_{OUT} at Zero Scale vs. V_{OUT}
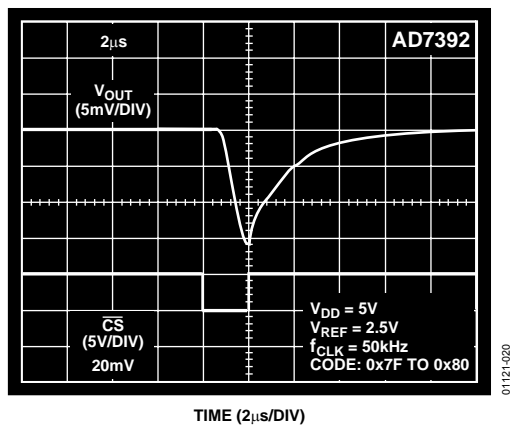
Figure 17. Midscale Transition Performance

Figure 18. Digital Feedthrough

Figure 19. Large Signal Settling Time

Figure 20. Reference Multiplying Bandwidth

Figure 21. INL Error vs. Reference Voltage
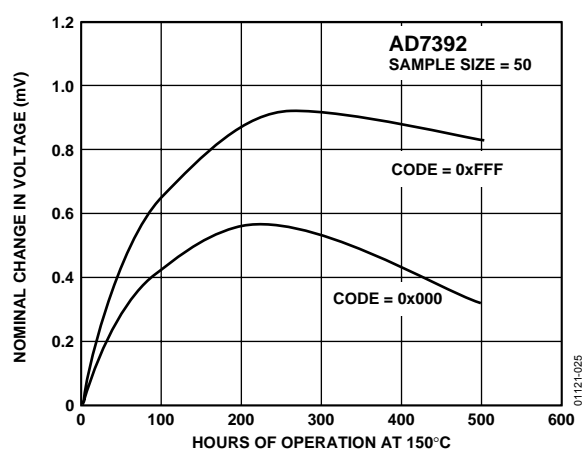
Figure 22. Long-Term Drift Accelerated by Burn-In
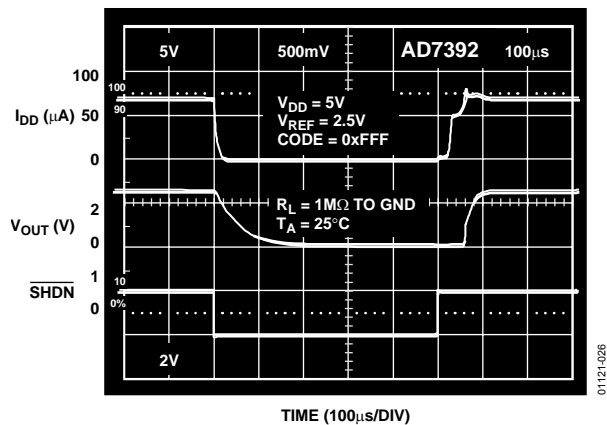
Figure 23. Shutdown Recovery Time

Figure 24. Shutdown Current vs. Temperature

Figure 25. AD7392 Differential Nonlinearity Error vs. Code
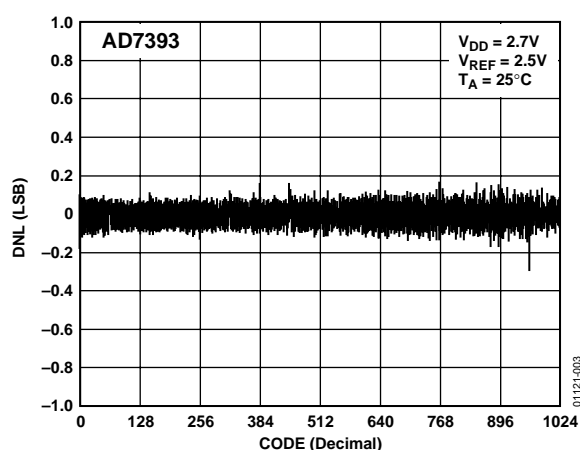
Figure 26. AD7393 Differential Nonlinearity Error vs. Code

OPERATION

The AD7392 and AD7393 comprise a set of pin-compatible, 2-bit/10-bit digital-to-analog converters. These single-supply operation devices consume less than 100 μA of current while operating from 2.7 V to 5.5 V power supplies, making them ideal for battery-operated applications. They contain a voltage-switched, 12-bit/10-bit, laser-trimmed digital-to-analog converter, rail-to-rail output op amps, and a parallel input DAC register. The external reference input has constant input resistance independent of the digital code setting of the DAC. In addition, the re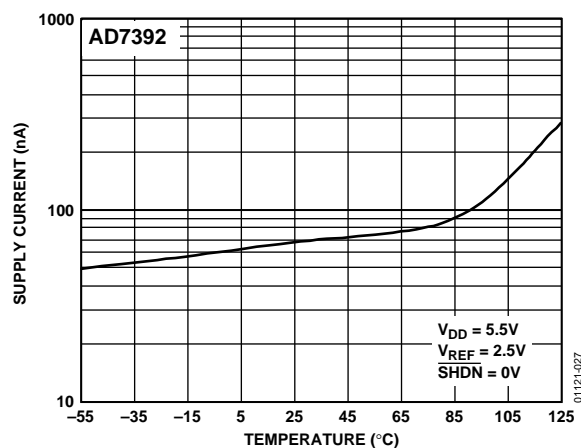ference input can be tied to the same supply voltage as V_{DD}, resulting in a maximum output voltage span of 0 V to V_{DD}. The parallel data interface consists of a $\overline{CS}$ write strobe and 12 data bits, D0–D11, for the AD7392 or 10 data bits, D0–D9, for the AD7393. An $\overline{RS}$ pin is available to reset the DAC register to zero scale. This function is useful for power-on reset or system failure recovery to a known state. Additional power savings are accomplished by activating the $\overline{SHDN}$ pin, resulting in a 1.5 μA maximum consumption sleep mode. While the supply voltage is on, data is retained in the DAC register to reset the DAC output when the part is taken out of shutdown ($\overline{SHDN}$ = 1).

D/A CONVERTER SECTION

The voltage switched R-2R DAC generates an output voltage that depends on the external reference voltage connected to the REF pin according to Equation 1:

$$V_{OUT} = V_{REF} \times \frac{D}{2^N} \tag{1}$$

where D is the decimal data-word loaded into the DAC register, and N is the number of bits of DAC resolution.

If the 10-bit AD7393 uses a 2.5 V reference, Equation 1 becomes

$$V_{OUT} = 2.5 \times \frac{D}{1024} \tag{2}$$

Using Equation 2, the nominal midscale voltage at V_{OUT} is 1.25 V for D = 512; full-scale voltage is 2.497 V. The LSB step size is $2.5 \times 1/1024 = 0.0024$ V.

If the 12-bit AD7392 uses a 5.0 V reference, Equation 1 becomes

$$V_{OUT} = V_{REF} \times \frac{D}{2^N} \tag{3}$$

Using Equation 3, the AD7392 provides a nominal midscale voltage of 2.50 V for D = 2048, and a full-scale V_{OUT} of 4.998 V. The LSB step size is $5.0 \times 1/4096 = 0.0012$ V.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. The op amp has a 60 μs typical settling time to 0.1% of full scale. There are slight differences in settling time for negative slewing signals versus positive. Also, negative transition settling time to within the last 6 LSBs of 0 V has an extended settling time. The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 27 shows an equivalent output schematic of the rail-to-rail amplifier with its N-channel pull-down FETs that pull an output load directly to GND. The output sourcing current is provided by a P-channel pull-up device that can source current to GND terminated loads.
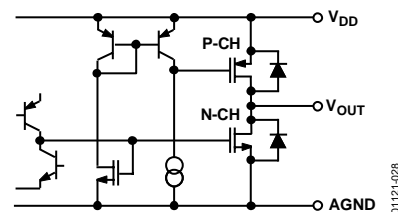

Figure 27. Equivalent Analog Output Circuit

The rail-to-rail output stage provides ±1 mA of output current. The N-channel output pull-down MOSFET, shown in Figure 27, has a 35 Ω on resistance that sets the sink current capability near ground. In addition to resistive load driving capability, the amplifier also has been carefully designed and characterized for up to 100 pF capacitive load driving capability.

REFERENCE INPUT

The reference input terminal has a constant input resistance independent of digital code, which results in reduced glitches on the external reference voltage source. The high 2.5 MΩ input resistance minimizes power dissipation within the AD7392/AD7393 D/A converters. The V_{REF} input accepts input voltages ranging from ground to the positive supply voltage V_{DD}. One of the simplest applications for saving an external reference voltage source is connecting the REF terminal to the positive V_{DD} supply. This connection results in a rail-to-rail voltage output span maximizing the programmed range. The reference input accepts ac signals as long as they stay within the 0 V < V_{REF} < V_{DD} supply voltage range. The reference bandwidth and integral nonlinearity error performance are plotted in the Typical Performance Characteristics section (Figure 20 and Figure 21). The ratiometric reference feature makes the AD7392/AD7393 an ideal companion to ratiometric analog-to-digital converters such as the AD7896.

POWER SUPPLY

The very low power consumption of the AD7392/AD7393 is a direct result of a circuit design that optimizes the CBCMOS process. By using the low power characteristics of CMOS for the logic and the low noise, tight-matching of the complementary bipolar transistors, excellent analog accuracy is achieved. One advantage of the rail-to-rail output amplifiers used in the AD7392/

AD7393 is the wide range of usable supply voltage. The part is fully specified and tested for operation from 2.7 V to 5.5 V.
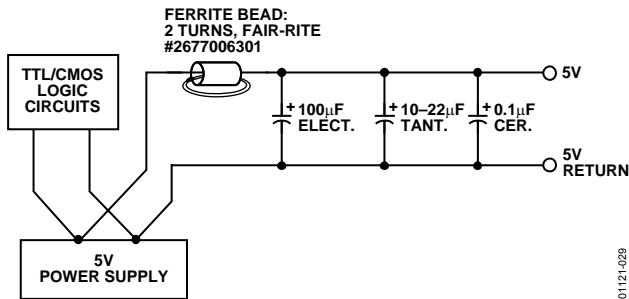

Figure 28. Use Separate Traces to Reduce Power Supply Noise

Whether or not a separate power supply trace is available, generous supply bypassing reduces supply line induced errors. Local supply bypassing, consisting of a 10 µF tantalum electrolytic in parallel with a 0.1 µF ceramic capacitor, is recommended for all applications (Figure 29).
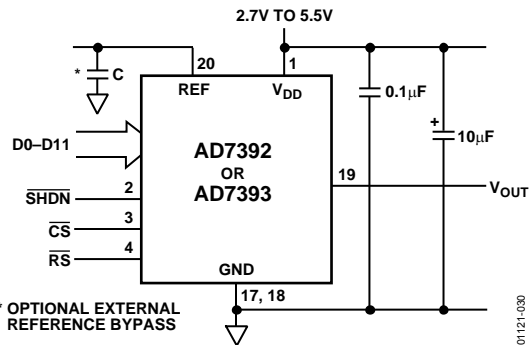

Figure 29. Recommended Supply Bypassing for the AD7392/AD7393

INPUT LOGIC LEVELS

All digital inputs are protected with a Zener-type ESD protection structure (Figure 30) that allows logic input voltages to exceed the V_{DD} supply voltage. This feature is useful if the user is driving one or more of the digital inputs with a 5 V CMOS logic input voltage level while operating the AD7392/ AD7393 on a 3 V power supply. If this interface is used, make sure that the V_{OL} of the 5 V CMOS meets the V_{IL} input requirement of the AD7392/ AD7393 operating at 3 V. See Figure 12 for a graph for digital logic input threshold versus operating V_{DD} supply voltage.
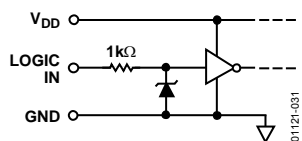

Figure 30. Equivalent Digital Input ESD Protection

To minimize power dissipation from input logic levels that are near the V_{IH} and V_{IL} logic input voltage specifications, a Schmitt-trigger design was used that minimizes the input buffer current consumption compared to traditional CMOS input stages. Figure 11 is a plot of supply current versus incremental input

voltage, showing that negligible current consumption takes place when logic levels are in their quiescent state. The normal crossover current still occurs during logic transitions. A secondary advantage of this Schmitt trigger is the prevention of false triggers that would occur with slow moving logic transitions when a standard CMOS logic interface or opto-isolators are used. Logic inputs D11–D0, $\overline{CS}$, $\overline{RS}$, and $\overline{SHDN}$ all contain the Schmitt-trigger circuits.

DIGITAL INTERFACE

The AD7392/AD7393 have a parallel data input. A functional block diagram of the digital section is shown in Figure 31, while Table 6 contains the truth table for the logic control inputs. The chip select ($\overline{CS}$) pin controls loading of data from the data inputs on Pins D11–D0. This active low input places the input register into a transparent state allowing the data inputs to directly change the DAC ladder values. When $\overline{CS}$ returns to logic high within the data setup-and-hold time specifications, the new value of data in the input register are latched. See Table 6 for a complete set of conditions.
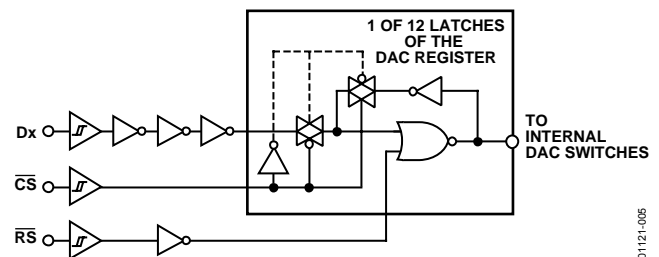
Figure 31. Digital Control Logic

Table 6. Control Logic Truth Table

$\overline{CS}$	$\overline{RS}$	DAC Register Function
H	H	Latched
L	H	Transparent
↑	H	Latched with New Data
X	L	Loaded with All Zeros
H	↑	Latched All Zeros

↑ = Positive logic transition.
X = Don't care.

RESET ($\overline{RS}$) PIN

Forcing the asynchronous $\overline{RS}$ pin low sets the DAC register to all 0s, so the DAC output voltage is 0 V. The reset function is useful for setting the DAC outputs to 0 at power-up or after a power supply interruption. Test systems and motor controllers are two of many applications that benefit from powering up to a known state. The external reset pulse can be generated by the microprocessor's power-on RESET signal, by an output from the microprocessor, or by an external resistor and capacitor. RESET has a Schmitt-trigger input, which results in a clean reset function when using external resistor/capacitor generated pulses. See Table 6.

POWER SHUTDOWN ($\overline{SHDN}$)

Maximum power savings can be achieved by using the power shutdown control function. This hardware-activated feature is controlled by the active low input $\overline{SHDN}$ pin. This pin has a Schmitt-trigger input that helps desensitize it to slowly changing inputs. Setting this pin to logic low reduces the internal consumption of the AD7392 or AD7393 to nanoamp levels, guaranteed to 1.5 µA maximum over the operating temperature range. If power is present at all times on the V_{DD} pin while in shutdown mode, the internal DAC register retains the last programmed data value. The digital interface is still active in shutdown so that code changes can be made that produce new DAC settings when the device is taken out of shutdown. This data is used when the part is returned to the normal active state by placing the DAC back to its programmed voltage setting. Figure 23 shows a plot of shutdown recovery time with both I_{DD} and V_{OUT} displayed. In the shutdown state, the DAC output amplifier exhibits an open-circuit high resistance state. Any load connected stabilizes at its termination voltage. If the power shutdown feature is not needed, the user should tie the $\overline{SHDN}$ pin to the V_{DD} voltage to disable this function.

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for the AD7392. As shown in Figure 32, the AD7392 has been designed to drive loads as low as 5 kΩ in parallel with 100 pF. The code table for this operation is shown in Table 7.

The circuit can be configured with an external reference plus power supply or powered from a single dedicated regulator or reference depending on the application performance requirements.
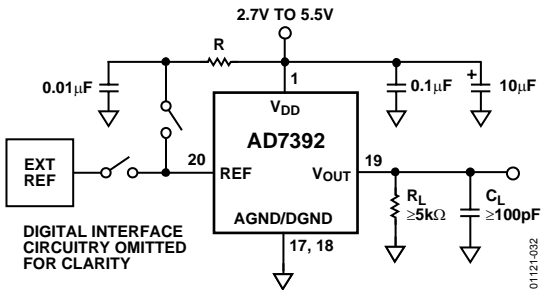
Figure 32. AD7392 Unipolar Output Operation

Table 7. Unipolar Code Table

DAC Register No.		
Hexadecimal	**Decimal**	**Output Voltage (V) V_{REF} = 2.5 V**
FFF	4095	2.4994
801	2049	1.2506
800	2048	1.2500
7FF	2047	1.2494
000	0	0

BIPOLAR OUTPUT OPERATION

Although the AD7393 is designed for single-supply operation, the output can be easily configured for bipolar operation. A typical circuit is shown in Figure 33. This circuit uses a clean, regulated 5 V supply for power, which also provides the circuit's reference voltage. Since the AD7393 output span swings from ground to very near 5 V, it is necessary to choose an external amplifier with a common-mode input voltage range that extends to its positive supply rail. The micropower consumption OP196 has been designed just for this purpose and results in only 50 μA of maximum current consumption. Connection of the two 470 kΩ resistors results in a differential amplifier mode of operation with a voltage gain of 2, which produces a circuit output span of 10 V, that is, −5 V to +5 V. As the DAC is programmed from zero-code 0x000 to midscale 0x200 to full scale 0x3FF, the circuit output voltage V_O is set at −5 V, 0 V, and +5 V (minus 1 LSB). The output voltage V_O is coded in offset binary according to Equation 4.

$$V_O = \left[\frac{D}{512} - 1 \right] \times 5 \qquad (4)$$

where D is the decimal code loaded in the AD7393 DAC register. Note that the LSB step size is 10/1024 = 10 mV. This circuit has been optimized for micropower consumption including the 470 kΩ gain setting resistors, which should have low temperature coefficients to maintain accuracy and matching (preferably the same resistor material, such as metal film).

If better stability is required, the power supply may be substituted with a precision reference voltage such as the low drop out REF195, which can easily supply the circuit's 162 μA of current, and still provide additional power for the load connected to V_O. The micropower REF195 is guaranteed to source 10 mA output drive current, but consumes only 50 μA internally.

If higher resolution is required, the AD7392 can be used with two additional bits of data inserted into the software coding, which results in a 2.5 mV LSB step size. Table 8 shows examples of nominal output voltages V_O provided by the bipolar operation circuit application.
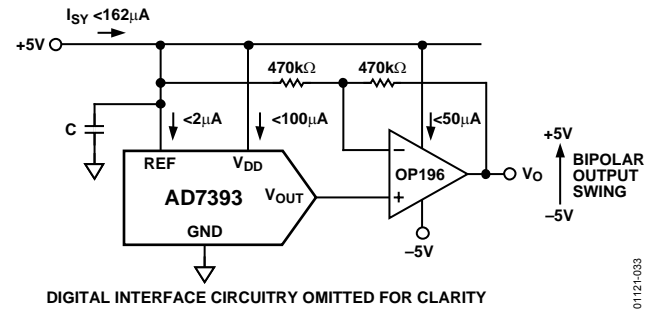
Figure 33. Bipolar Output Operation

Table 8. Bipolar Code Table

DAC Register No.		Analog Output Voltage (V)
Hexadecimal	Decimal	
3FF	1023	4.9902
201	513	0.0097
200	512	0.0000
1FF	511	−0.0097
000	0	−5.0000

OUTLINE DIMENSIONS

0.985 (25.02)
0.965 (24.51)
0.945 (24.00)

0.295 (7.49)
0.285 (7.24)
0.275 (6.99)

0.325 (8.26)
0.310 (7.87)
0.300 (7.62)

0.150 (3.81)
0.135 (3.43)
0.120 (3.05)

0.180 (4.57) MAX

0.015 (0.38) MIN

0.150 (3.81)
0.130 (3.30)
0.110 (2.79)

0.022 (0.56)
0.018 (0.46)
0.014 (0.36)

0.100 (2.54) BSC

0.060 (1.52)
0.050 (1.27)
0.045 (1.14)

SEATING PLANE

0.015 (0.38)
0.010 (0.25)
0.008 (0.20)

COMPLIANT TO JEDEC STANDARDS MO-095-AE
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 34. 20-Lead PDIP Package
(N-20)
Dimensions shown in inches and (mm)

13.00 (0.5118)
12.60 (0.4961)

7.60 (0.2992)
7.40 (0.2913)

10.65 (0.4193)
10.00 (0.3937)

2.65 (0.1043)
2.35 (0.0925)

0.75 (0.0295)
0.25 (0.0098) × 45°

0.30 (0.0118)
0.10 (0.0039)

COPLANARITY
0.10

1.27 (0.0500) BSC

0.51 (0.0201)
0.31 (0.0122)

SEATING PLANE

0.33 (0.0130)
0.20 (0.0079)

8°
0°

1.27 (0.0500)
0.40 (0.0157)

COMPLIANT TO JEDEC STANDARDS MS-013AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 35. 20-Lead SOIC Package
(R-20)
Dimensions shown in inches and (mm)

ORDERING GUIDE

Model	Resolution (Bit)	Temperature Range	Package Description	Package Option
AD7392AN	12	−40°C to +85°	20-Lead PDIP	N-20
AD7392AR	12	−40°C to +85°	20-Lead SOIC	R-20
AD7392AR-REEL	12	−40°C to +85°	20-Lead SOIC	R-20
AD7392ARZ[1]	12	−40°C to +85°	20-Lead SOIC	R-20
AD7392ARZ-REEL	12	−40°C to +85°	20-Lead SOIC	R-20
AD7393AR	10	−40°C to +85°	20-Lead SOIC	R-20

[1] Z = Pb-free part.

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