

# 74AC20

## Dual 4-Input NAND Gate

### Features

- $I_{CC}$  reduced by 50%
- Outputs source/sink 24mA

### General Description

The AC20 contains four, 4-input NAND gates.

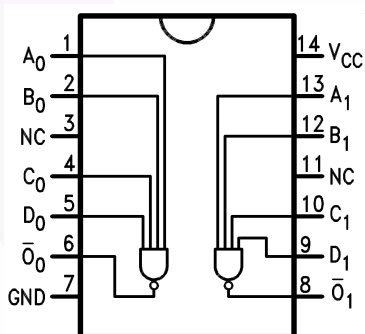
### Ordering Information

Order Number	Package Number	Package Description
74AC20SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC20SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC20MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC20PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

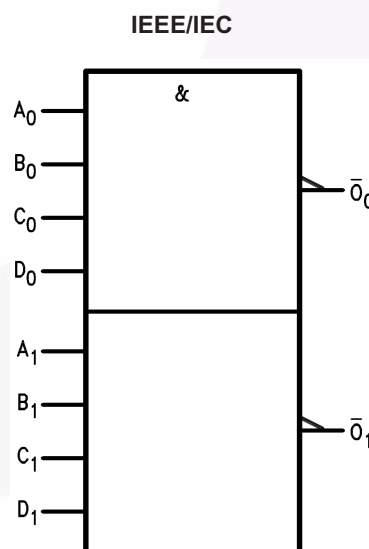
### Connection Diagram



### Pin Description

Pin Names	Description
$A_n, B_n, C_n, D_n$	Inputs
$\bar{O}_n$	Outputs

### Logic Symbol



## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	−0.5V to +7.0V
$I_{IK}$	DC Input Diode Current $V_I = -0.5V$	−20mA
	$V_I = V_{CC} + 0.5$	+20mA
$V_I$	DC Input Voltage	−0.5V to $V_{CC} + 0.5V$
$I_{OK}$	DC Output Diode Current $V_O = -0.5V$	−20mA
	$V_O = V_{CC} + 0.5V$	+20mA
$V_O$	DC Output Voltage	−0.5V to $V_{CC} + 0.5V$
$I_O$	DC Output Source or Sink Current	±50mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Output Pin	±50mA
$T_{STG}$	Storage Temperature	−65°C to +150°C
$T_J$	Junction Temperature	140°C

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	2.0V to 6.0V
$V_I$	Input Voltage	0V to $V_{CC}$
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	−40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate: $V_{IN}$ from 30% to 70% of $V_{CC}$ ; $V_{CC}$ @ 3.3V, 4.5V, 5.5V	125mV/ns

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	1.5	2.1	2.1		V
		4.5		2.25	3.15	3.15		
		5.5		2.75	3.85	3.85		
V <sub>IL</sub>	Maximum LOW Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	1.5	0.9	0.9		V
		4.5		2.25	1.35	1.35		
		5.5		2.75	1.65	1.65		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	3.0	I <sub>OUT</sub> = −50μA	2.99	2.9	2.9		V
		4.5		4.49	4.4	4.4		
		5.5		5.49	5.4	5.4		
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = −12mA		2.56	2.46		
		4.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = −24mA		3.86	3.76	
		5.5			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = −24mA <sup>(1)</sup>		4.86	
V <sub>OL</sub>	Maximum LOW Level Output Voltage	3.0	I <sub>OUT</sub> = 50μA	0.002		0.1	0.1	
		4.5		0.001	0.1	0.1		
		5.5		0.001	0.1	0.1		
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 12mA		0.36	0.44		
		4.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA		0.36	0.44	
		5.5			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA <sup>(1)</sup>		0.36	0.44
I <sub>IN</sub> <sup>(3)</sup>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND			±0.1	±1.0	μA
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(2)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75	mA	
I <sub>OHD</sub>		5.5	V <sub>OHD</sub> = 3.85V Min.			−75	mA	
I <sub>CC</sub> <sup>(3)</sup>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.0	20.0	μA	

## Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

**AC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V) <sup>(4)</sup>	$T_A = +25^{\circ}\text{C}$ , $C_L = 50\text{pF}$			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ , $C_L = 50\text{pF}$		Units
			Min.	Typ.	Max.	Min.	Max.	
$t_{PLH}$	Propagation Delay	3.3	2.0	6.0	8.5	1.5	10.0	ns
		5.0	1.5	5.0	7.0	1.0	8.0	
$t_{PHL}$	Propagation Delay	3.3	1.5	5.0	7.0	1.0	9.0	ns
		5.0	1.5	4.0	6.0	1.0	7.0	

**Note:**

4. Voltage range 3.3 is  $3.3\text{V} \pm 0.3\text{V}$ . Voltage range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ .

**Capacitance**

Symbol	Parameter	Conditions	Typ.	Units
$C_{IN}$	Input Capacitance	$V_{CC} = \text{OPEN}$	4.5	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CC} = 5.0\text{V}$	40.0	pF

## Physical Dimensions

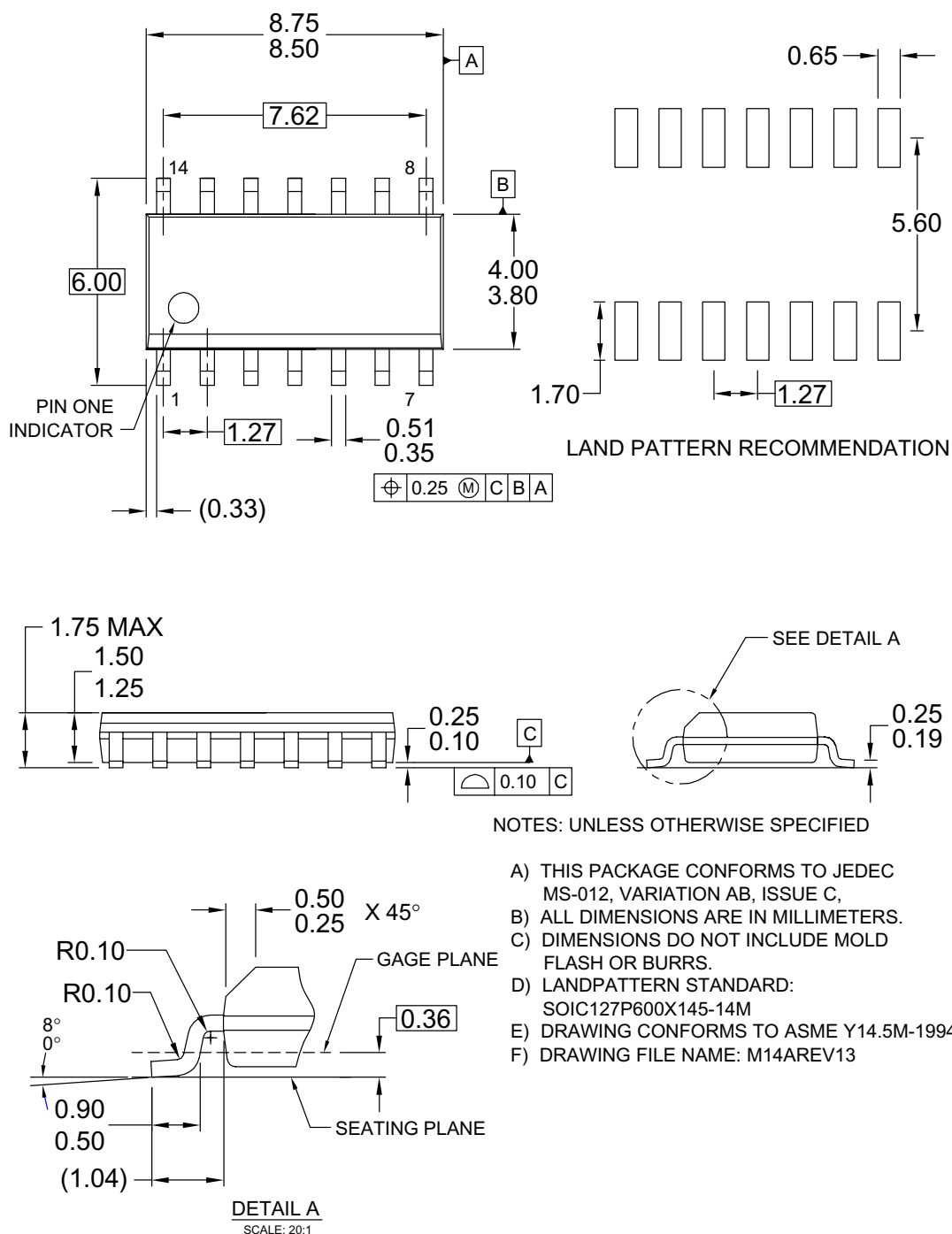


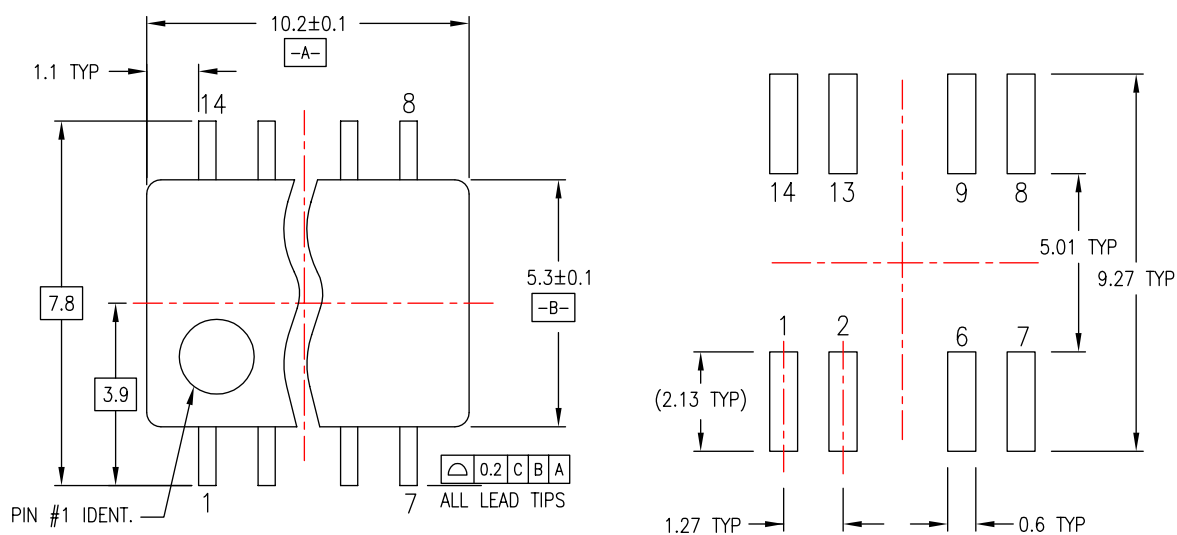
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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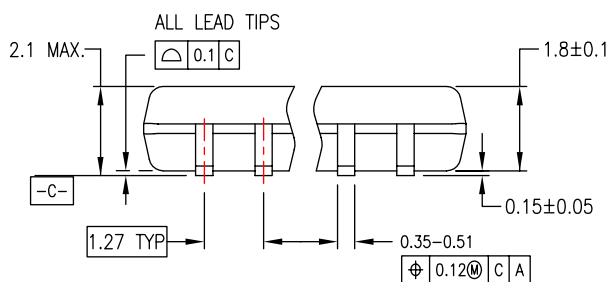
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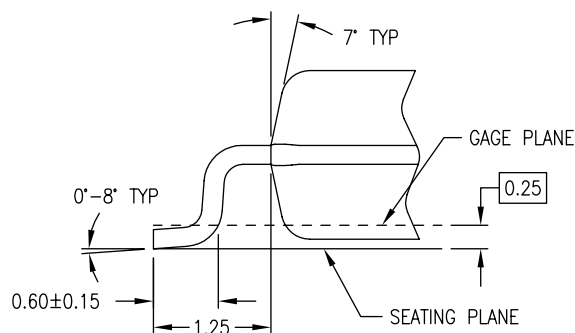
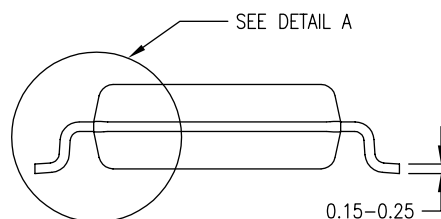
### Physical Dimensions (Continued)



## LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DREVC

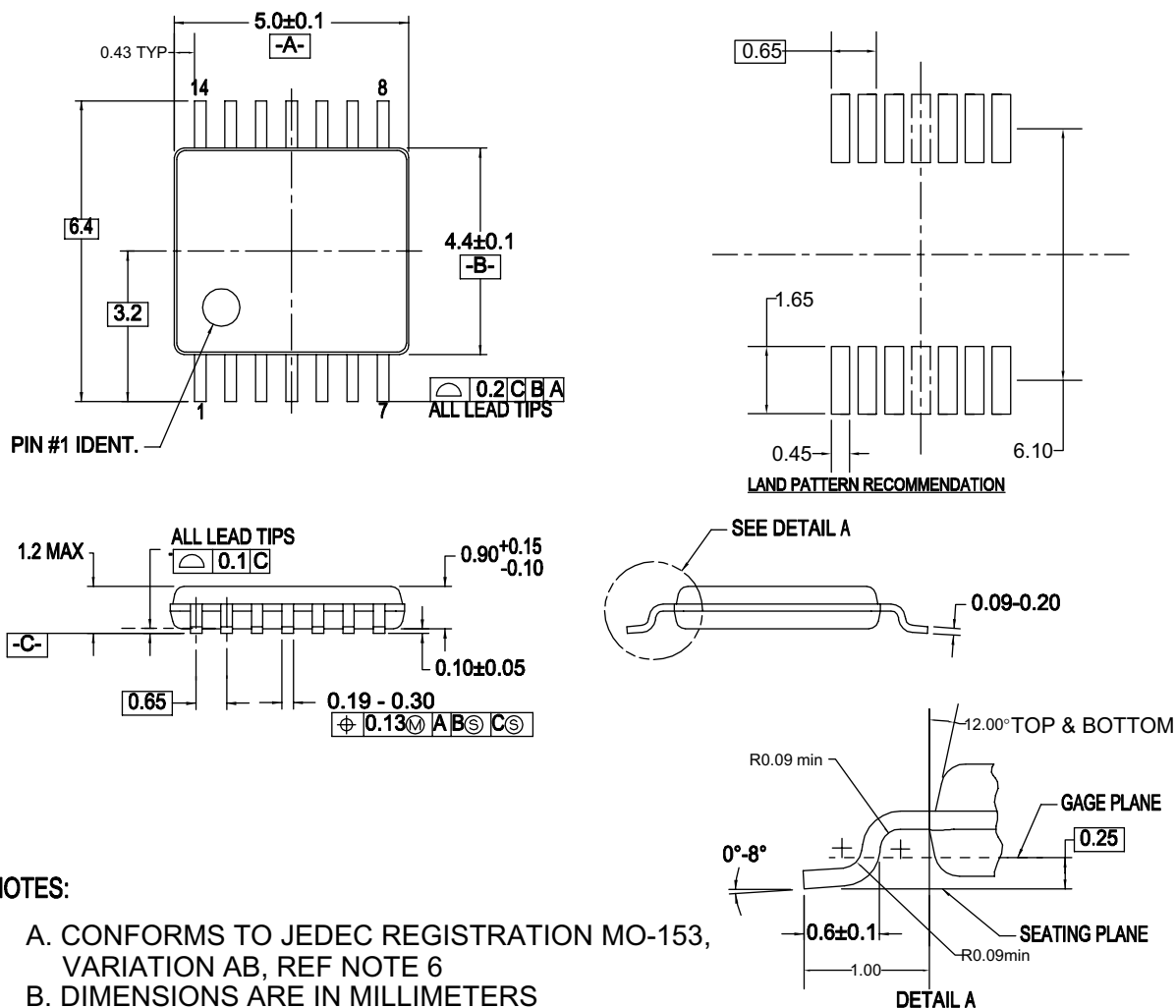
**Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**

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## Physical Dimensions (Continued)



## NOTES:

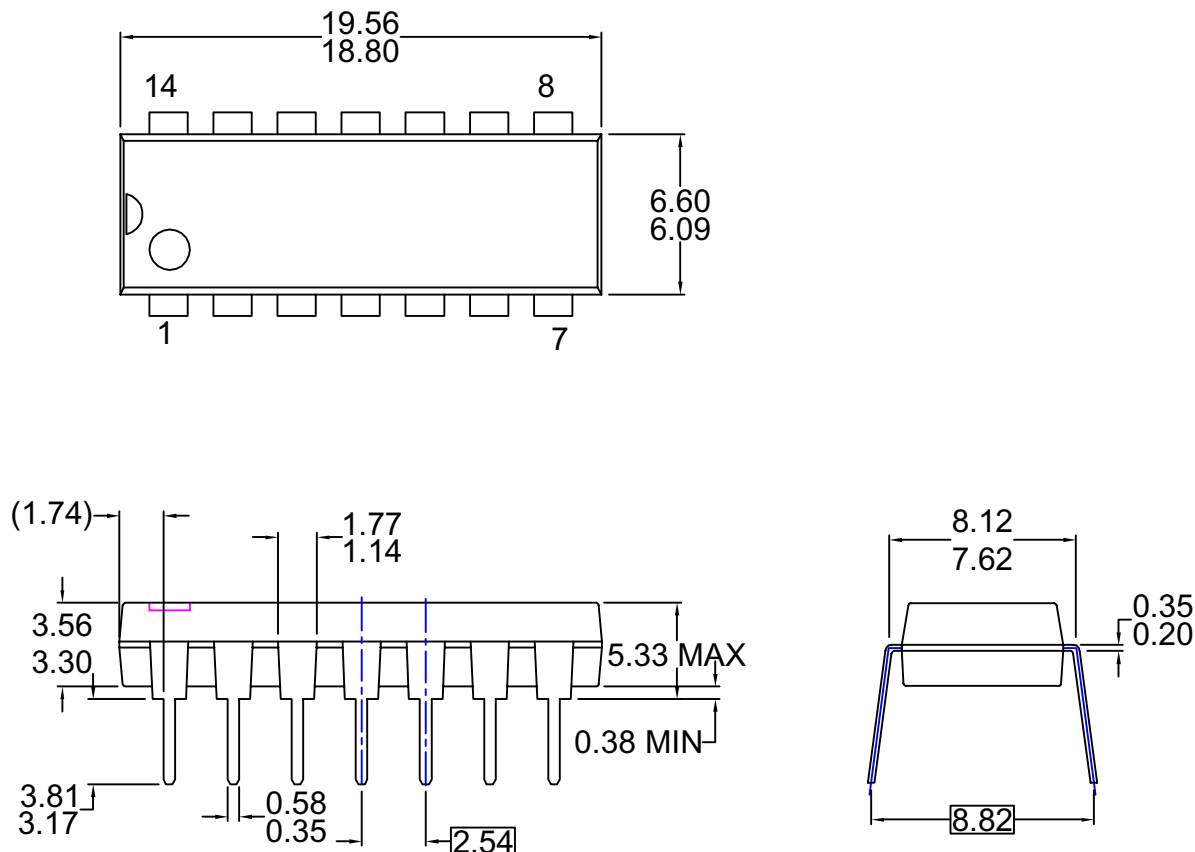
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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**Physical Dimensions** (Continued)**NOTES: UNLESS OTHERWISE SPECIFIED**

THIS PACKAGE CONFORMS TO

A) JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS,  
MOLD FLASH, AND TIE BAR EXTRUSIONS.D) DIMENSIONS AND TOLERANCES PER  
ASME Y14.5-1994

E) DRAWING FILE NAME: MKT-N14AREV7

**Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**

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Rev. I32

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