

312 OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64 GRAY SCALES)

The μPD16633B is a source driver for TFT-LCDs capable of dealing with displays with 64 gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ -corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as 9.8 V_{P-P}, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 45 MHz when driving at 3.0 V, this driver is applicable to XGA-standard TFT-LCD panels.

FEATURES

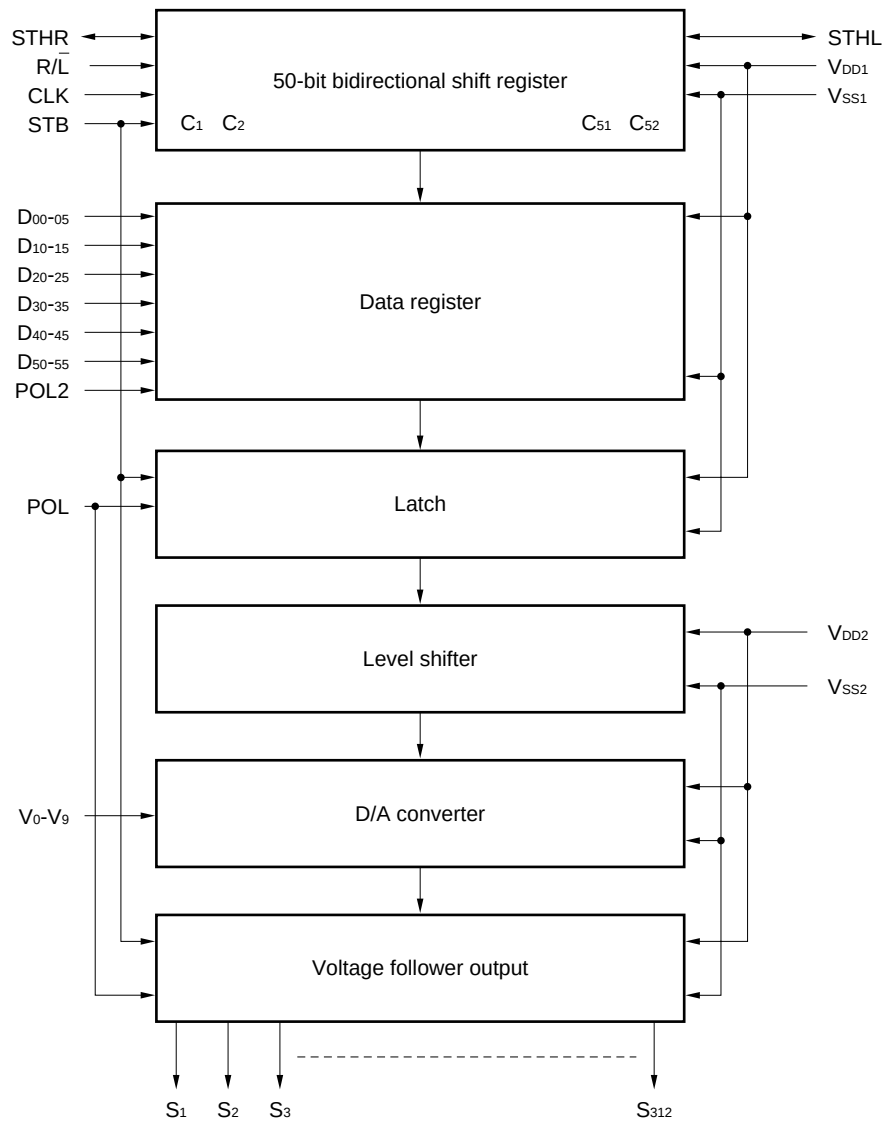
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- Output dynamic range 9.8 V_{P-P} min. (@V_{DD2} = 10.0 V)
- CMOS level input
- Input of 6 bits (gradation data) by 6 dots
- High-speed data transfer: f_{max.} = 45 MHz (internal data transfer speed when operating at 3.0 V)
- 312 outputs
- Apply for only dot inversion
- Display data inversion function (POL2 terminal.)
- Single bank arrangement is possible (loaded with slim TCP)

ORDERING INFORMATION

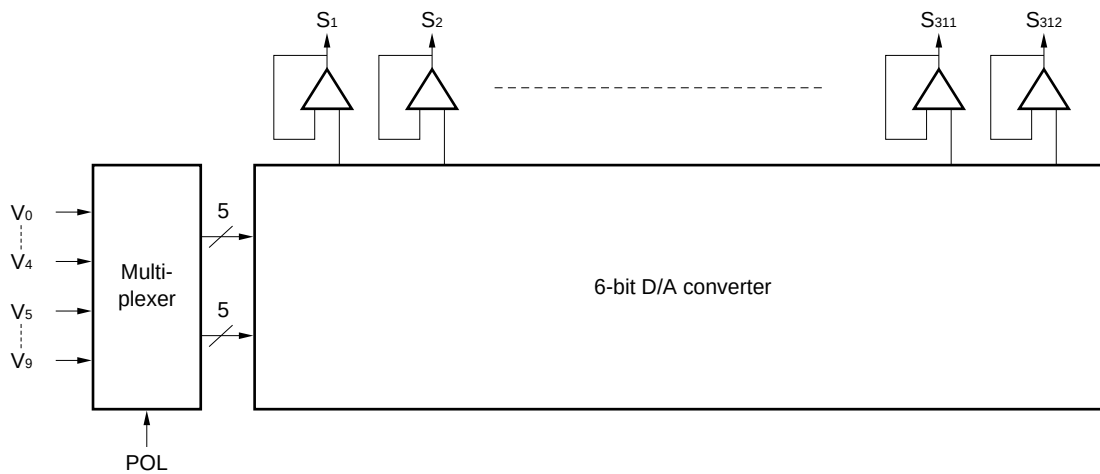
Part Number	Package
μPD16633BN-xxx	TCP (TAB package)

The TCP's external shape is customized. To order your TCP's external shape, please contact a NEC salesperson.

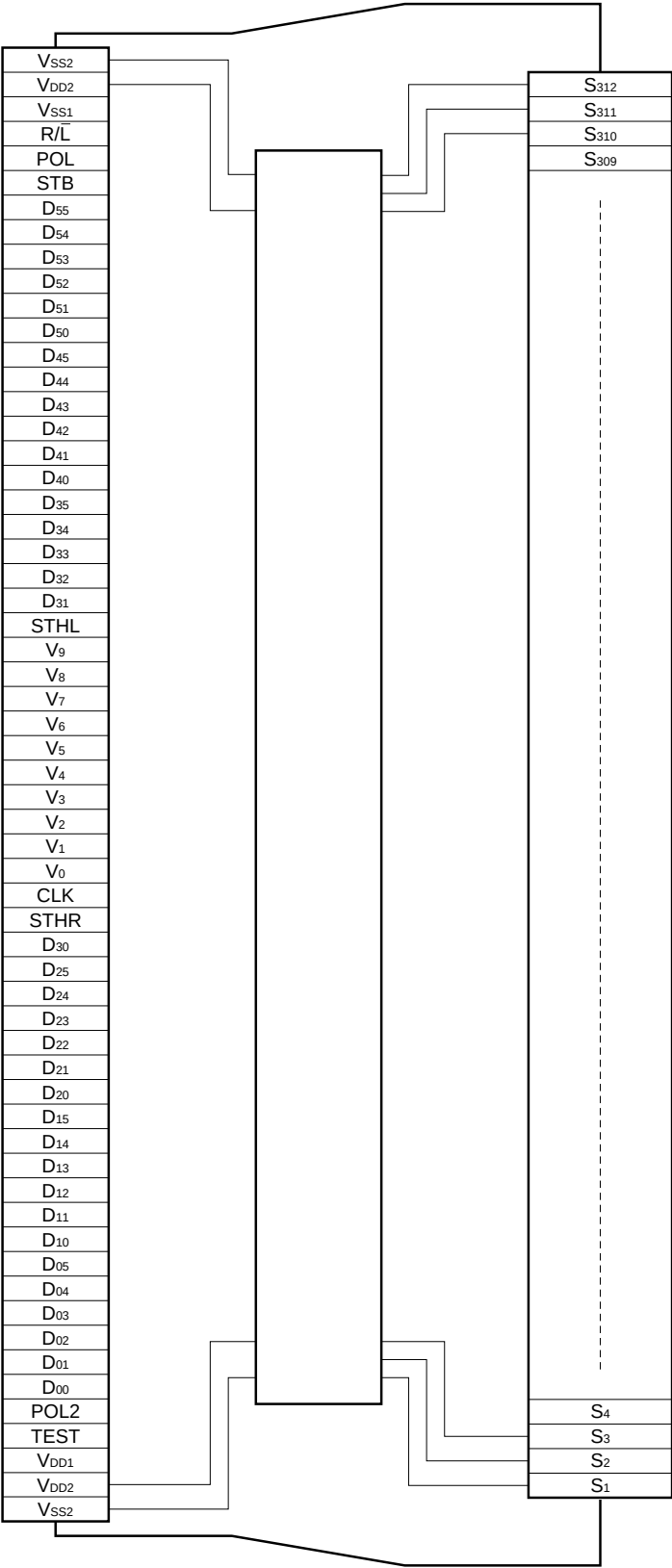
1. BLOCK DIAGRAM



2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16633BN-xxx) (Copper Plated surface)



Caution This figure does not specify the TCP package.

4. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S ₁ to S ₃₁₂	Driver output	The D/A converted 64-gray-scale analog voltage is output.
D ₀₀ to D ₀₅	Display data input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D _{x0} : LSB, D _{x5} : MSB
D ₁₀ to D ₁₅		
D ₂₀ to D ₂₅		
D ₃₀ to D ₃₅		
D ₄₀ to D ₄₅		
D ₅₀ to D ₅₅		
R/L	Shift direction control input	These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R/L = H: STHR input, S ₁ → S ₃₁₂ , STHL output R/L = L: STHL input, S ₃₁₂ → S ₁ , STHR output
STHR	Right shift start pulse input/output	R/L = H: Becomes the start pulse input pin. R/L = L: Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	R/L = H: Becomes the start pulse output pin. R/L = L: Becomes the start pulse input pin.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 52nd clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. The initial-level driver's 52nd clock becomes valid as the next-level driver's start pulse is input. If 54th clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	POL = L: The S _{2n-1} output uses V ₀ to V ₄ as the reference supply; The S _{2n} output uses V ₅ to V ₉ as the reference supply. POL = H: The S _{2n-1} output uses V ₅ to V ₉ as the reference supply; The S _{2n} output uses V ₀ to V ₄ as the reference supply.
POL2	Data inversion	POL2 = H: Display data is inverted. POL2 = L: Display data is not inverted.
V ₀ to V ₉	γ -corrected power supplies	Input the γ -corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. V _{DD2} > V ₀ > V ₁ > V ₂ > V ₃ > V ₄ > V ₅ > V ₆ > V ₇ > V ₈ > V ₉ > V _{SS2}
TEST	Test pin	TEST = H or Open: Standard mode TEST = L: Test mode Please input "H" level.
V _{DD1}	Logic power supply	3.3 V $\pm$ 0.3 V
V _{DD2}	Driver power supply	10.0 V to 13.5 V
V _{SS1}	Logic ground	Grounding
V _{SS2}	Driver ground	Grounding

- Cautions**
1. The power start sequence must be V_{DD1} , logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut down. (Simultaneous power application to V_{DD2} and V_0 to V_9 is possible.)
 2. To stabilize the supply voltage, please be sure to insert a $0.47\ \mu\text{F}$ bypass capacitor between V_{DD1} - V_{SS1} and V_{DD2} - V_{SS2} . Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about $0.01\ \mu\text{F}$ is also advised between the γ -corrected power supply terminals ($V_0, V_1, V_2, \dots, V_9$) and V_{SS2} .

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches. The ladder resistors r_0 to r_{62} are so designed that the ratios between the LCD panel's γ -corrected voltages and V_0 to V_{63} and V_0 to V_{63} are roughly equal; and their respective resistance values are as shown on page 9. Among the 5-by-2 γ -corrected voltages, input gray scale voltages of the same polarity with respect to the common voltage, for the respective five γ -corrected voltages of V_0 to V_4 and V_5 to V_9 .

Figure 1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2} , common electrode potential V_{COM} , and γ -corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships of $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$.

Figures 2-1 and 2-2 show the relationship between the input data and the output data. Table 1 shows the resistance values of the resistor strings.

This driver IC is designed for single-sided mounting. Therefore, please do not use it for γ -corrected power supply level inversion in double-sided mounting. Because the current flowing through ladder resistors r_0 to r_{62} is small, its use for double-sided mounting impairs the IC's stable operation when the level of the γ -corrected power supply terminal is inverted thus causing display failures.

Figure 1. Relationship Between Input Data and Output Voltage

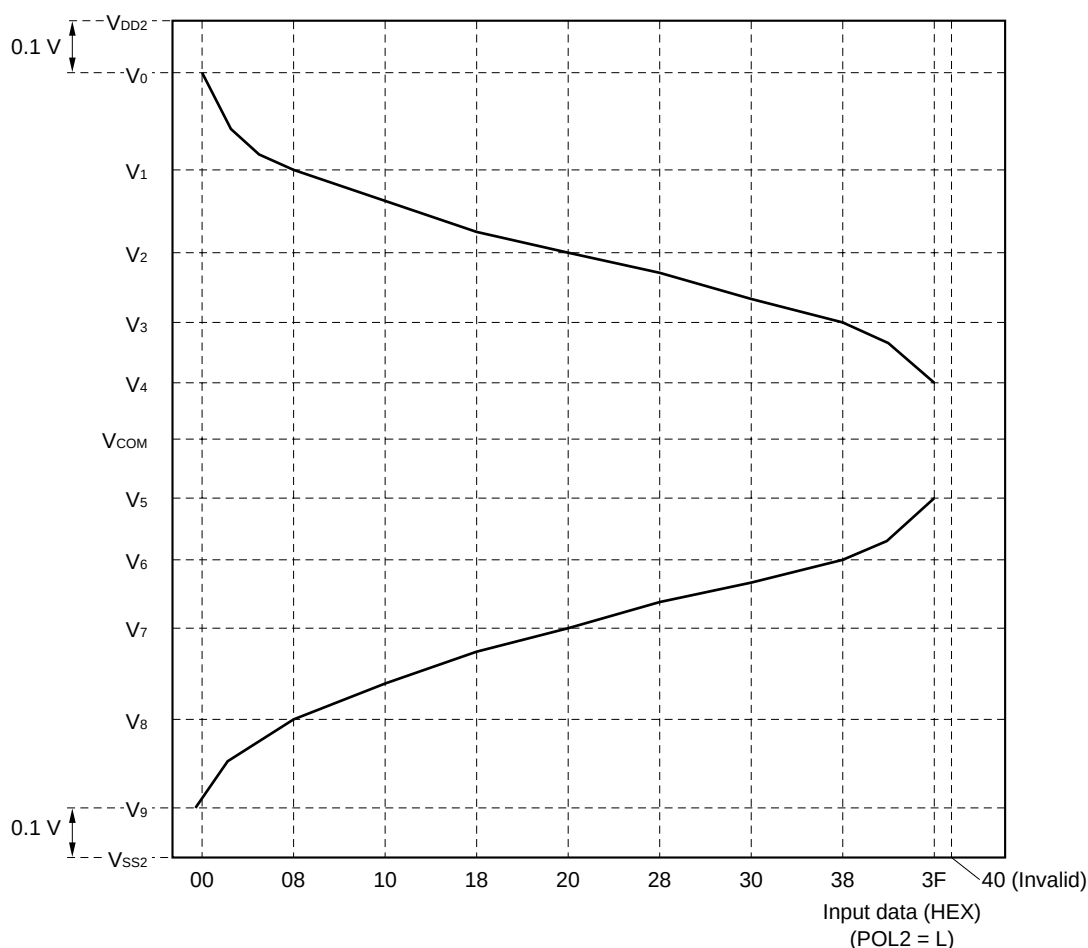


Figure 2-1. Relationship Between Input Data and Output Voltage: $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5$

	Data	D _{X5}	D _{X4}	D _{X3}	D _{X2}	D _{X1}	D _{X0}	Output Voltage	
V ₀	00 _H	0	0	0	0	0	0	V _{0'}	V ₀
	01 _H	0	0	0	0	0	1	V _{1'}	$V_1 + (V_0 - V_1) \times 4500/5300$
	02 _H	0	0	0	0	1	0	V _{2'}	$V_1 + (V_0 - V_1) \times 3700/5300$
	03 _H	0	0	0	0	1	1	V _{3'}	$V_1 + (V_0 - V_1) \times 2900/5300$
	04 _H	0	0	0	1	0	0	V _{4'}	$V_1 + (V_0 - V_1) \times 2200/5300$
	05 _H	0	0	0	1	0	1	V _{5'}	$V_1 + (V_0 - V_1) \times 1500/5300$
	06 _H	0	0	0	1	1	0	V _{6'}	$V_1 + (V_0 - V_1) \times 900/5300$
	07 _H	0	0	0	1	1	1	V _{7'}	$V_1 + (V_0 - V_1) \times 400/5300$
V ₁	08 _H	0	0	1	0	0	0	V _{8'}	V ₁
	09 _H	0	0	1	0	0	1	V _{9'}	$V_2 + (V_1 - V_2) \times 3600/4000$
	0A _H	0	0	1	0	1	0	V _{10'}	$V_2 + (V_1 - V_2) \times 3300/4000$
	0B _H	0	0	1	0	1	1	V _{11'}	$V_2 + (V_1 - V_2) \times 3000/4000$
	0C _H	0	0	1	1	0	0	V _{12'}	$V_2 + (V_1 - V_2) \times 2700/4000$
	0D _H	0	0	1	1	0	1	V _{13'}	$V_2 + (V_1 - V_2) \times 2400/4000$
	0E _H	0	0	1	1	1	0	V _{14'}	$V_2 + (V_1 - V_2) \times 2200/4000$
	0F _H	0	0	1	1	1	1	V _{15'}	$V_2 + (V_1 - V_2) \times 2000/4000$
V ₂	10 _H	0	1	0	0	0	0	V _{16'}	$V_2 + (V_1 - V_2) \times 1800/4000$
	11 _H	0	1	0	0	0	1	V _{17'}	$V_2 + (V_1 - V_2) \times 1600/4000$
	12 _H	0	1	0	0	1	0	V _{18'}	$V_2 + (V_1 - V_2) \times 1400/4000$
	13 _H	0	1	0	0	1	1	V _{19'}	$V_2 + (V_1 - V_2) \times 1300/4000$
	14 _H	0	1	0	1	0	0	V _{20'}	$V_2 + (V_1 - V_2) \times 1200/4000$
	15 _H	0	1	0	1	0	1	V _{21'}	$V_2 + (V_1 - V_2) \times 1100/4000$
	16 _H	0	1	0	1	1	0	V _{22'}	$V_2 + (V_1 - V_2) \times 1000/4000$
	17 _H	0	1	0	1	1	1	V _{23'}	$V_2 + (V_1 - V_2) \times 900/4000$
V ₃	18 _H	0	1	1	0	0	0	V _{24'}	$V_2 + (V_1 - V_2) \times 800/4000$
	19 _H	0	1	1	0	0	1	V _{25'}	$V_2 + (V_1 - V_2) \times 700/4000$
	1A _H	0	1	1	0	1	0	V _{26'}	$V_2 + (V_1 - V_2) \times 600/4000$
	1B _H	0	1	1	0	1	1	V _{27'}	$V_2 + (V_1 - V_2) \times 500/4000$
	1C _H	0	1	1	1	0	0	V _{28'}	$V_2 + (V_1 - V_2) \times 400/4000$
	1D _H	0	1	1	1	0	1	V _{29'}	$V_2 + (V_1 - V_2) \times 300/4000$
	1E _H	0	1	1	1	1	0	V _{30'}	$V_2 + (V_1 - V_2) \times 200/4000$
	1F _H	0	1	1	1	1	1	V _{31'}	$V_2 + (V_1 - V_2) \times 100/4000$
V ₄	20 _H	1	0	0	0	0	0	V _{32'}	V ₂
	21 _H	1	0	0	0	0	1	V _{33'}	$V_3 + (V_2 - V_3) \times 2600/2700$
	22 _H	1	0	0	0	1	0	V _{34'}	$V_3 + (V_2 - V_3) \times 2500/2700$
	23 _H	1	0	0	0	1	1	V _{35'}	$V_3 + (V_2 - V_3) \times 2400/2700$
	24 _H	1	0	0	1	0	0	V _{36'}	$V_3 + (V_2 - V_3) \times 2300/2700$
	25 _H	1	0	0	1	0	1	V _{37'}	$V_3 + (V_2 - V_3) \times 2200/2700$
	26 _H	1	0	0	1	1	0	V _{38'}	$V_3 + (V_2 - V_3) \times 2100/2700$
	27 _H	1	0	0	1	1	1	V _{39'}	$V_3 + (V_2 - V_3) \times 2000/2700$
V ₅	28 _H	1	0	1	0	0	0	V _{40'}	$V_3 + (V_2 - V_3) \times 1900/2700$
	29 _H	1	0	1	0	0	1	V _{41'}	$V_3 + (V_2 - V_3) \times 1800/2700$
	2A _H	1	0	1	0	1	0	V _{42'}	$V_3 + (V_2 - V_3) \times 1700/2700$
	2B _H	1	0	1	0	1	1	V _{43'}	$V_3 + (V_2 - V_3) \times 1600/2700$
	2C _H	1	0	1	1	0	0	V _{44'}	$V_3 + (V_2 - V_3) \times 1500/2700$
	2D _H	1	0	1	1	0	1	V _{45'}	$V_3 + (V_2 - V_3) \times 1400/2700$
	2E _H	1	0	1	1	1	0	V _{46'}	$V_3 + (V_2 - V_3) \times 1300/2700$
	2F _H	1	0	1	1	1	1	V _{47'}	$V_3 + (V_2 - V_3) \times 1200/2700$
V ₆	30 _H	1	1	0	0	0	0	V _{48'}	$V_3 + (V_2 - V_3) \times 1100/2700$
	31 _H	1	1	0	0	0	1	V _{49'}	$V_3 + (V_2 - V_3) \times 1000/2700$
	32 _H	1	1	0	0	1	0	V _{50'}	$V_3 + (V_2 - V_3) \times 900/2700$
	33 _H	1	1	0	0	1	1	V _{51'}	$V_3 + (V_2 - V_3) \times 800/2700$
	34 _H	1	1	0	1	0	0	V _{52'}	$V_3 + (V_2 - V_3) \times 700/2700$
	35 _H	1	1	0	1	0	1	V _{53'}	$V_3 + (V_2 - V_3) \times 600/2700$
	36 _H	1	1	0	1	1	0	V _{54'}	$V_3 + (V_2 - V_3) \times 400/2700$
	37 _H	1	1	0	1	1	1	V _{55'}	$V_3 + (V_2 - V_3) \times 200/2700$
V ₇	38 _H	1	1	1	0	0	0	V _{56'}	V ₃
	39 _H	1	1	1	0	0	1	V _{57'}	$V_4 + (V_3 - V_4) \times 2300/2500$
	3A _H	1	1	1	0	1	0	V _{58'}	$V_4 + (V_3 - V_4) \times 2100/2500$
	3B _H	1	1	1	0	1	1	V _{59'}	$V_4 + (V_3 - V_4) \times 1800/2500$
	3C _H	1	1	1	1	0	0	V _{60'}	$V_4 + (V_3 - V_4) \times 1500/2500$
	3D _H	1	1	1	1	0	1	V _{61'}	$V_4 + (V_3 - V_4) \times 1200/2500$
	3E _H	1	1	1	1	1	0	V _{62'}	$V_4 + (V_3 - V_4) \times 800/2500$
	3F _H	1	1	1	1	1	1	V _{63'}	V ₄

Caution Between V₄ and V₅ terminal is connected by using the resistor (9 kΩ) in the chip.

Figure 2-2. Relationship Between Input Data and Output Voltage: $V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$

	Data	D _{X5}	D _{X4}	D _{X3}	D _{X2}	D _{X1}	D _{X0}	Output Voltage	
								V ₀ "	V ₉
V ₄ → V ₆₃ '	00 _H	0	0	0	0	0	0	V ₀ "	V ₉
	01 _H	0	0	0	0	0	1	V ₁ "	$V_9 + (V_8 - V_9) \times 800/5300$
	02 _H	0	0	0	0	1	0	V ₂ "	$V_9 + (V_8 - V_9) \times 1600/5300$
	03 _H	0	0	0	0	1	1	V ₃ "	$V_9 + (V_8 - V_9) \times 2400/5300$
	04 _H	0	0	0	1	0	0	V ₄ "	$V_9 + (V_8 - V_9) \times 3100/5300$
	05 _H	0	0	0	1	0	1	V ₅ "	$V_9 + (V_8 - V_9) \times 3800/5300$
	06 _H	0	0	0	1	1	0	V ₆ "	$V_9 + (V_8 - V_9) \times 4400/5300$
V ₅ → V ₆₃ "	07 _H	0	0	0	1	1	1	V ₇ "	$V_9 + (V_8 - V_9) \times 4900/5300$
	08 _H	0	0	1	0	0	0	V ₈ "	V ₈
	09 _H	0	0	1	0	0	1	V ₉ "	$V_8 + (V_7 - V_8) \times 400/4000$
	0A _H	0	0	1	0	1	0	V ₁₀ "	$V_8 + (V_7 - V_8) \times 700/4000$
	0B _H	0	0	1	0	1	1	V ₁₁ "	$V_8 + (V_7 - V_8) \times 1000/4000$
	0C _H	0	0	1	1	0	0	V ₁₂ "	$V_8 + (V_7 - V_8) \times 1300/4000$
	0D _H	0	0	1	1	0	1	V ₁₃ "	$V_8 + (V_7 - V_8) \times 1600/4000$
V ₆ → V ₆₂ "	0E _H	0	0	1	1	1	0	V ₁₄ "	$V_8 + (V_7 - V_8) \times 1800/4000$
	0F _H	0	0	1	1	1	1	V ₁₅ "	$V_8 + (V_7 - V_8) \times 2000/4000$
	10 _H	0	1	0	0	0	0	V ₁₆ "	$V_8 + (V_7 - V_8) \times 2200/4000$
	11 _H	0	1	0	0	0	1	V ₁₇ "	$V_8 + (V_7 - V_8) \times 2400/4000$
	12 _H	0	1	0	0	1	0	V ₁₈ "	$V_8 + (V_7 - V_8) \times 2600/4000$
	13 _H	0	1	0	0	1	1	V ₁₉ "	$V_8 + (V_7 - V_8) \times 2700/4000$
	14 _H	0	1	0	1	0	0	V ₂₀ "	$V_8 + (V_7 - V_8) \times 2800/4000$
V ₇ → V ₆₁ "	15 _H	0	1	0	1	0	1	V ₂₁ "	$V_8 + (V_7 - V_8) \times 2900/4000$
	16 _H	0	1	0	1	1	0	V ₂₂ "	$V_8 + (V_7 - V_8) \times 3000/4000$
	17 _H	0	1	0	1	1	1	V ₂₃ "	$V_8 + (V_7 - V_8) \times 3100/4000$
	18 _H	0	1	1	0	0	0	V ₂₄ "	$V_8 + (V_7 - V_8) \times 3200/4000$
	19 _H	0	1	1	0	0	1	V ₂₅ "	$V_8 + (V_7 - V_8) \times 3300/4000$
	1A _H	0	1	1	0	1	0	V ₂₆ "	$V_8 + (V_7 - V_8) \times 3400/4000$
	1B _H	0	1	1	0	1	1	V ₂₇ "	$V_8 + (V_7 - V_8) \times 3500/4000$
V ₈ → V ₆₀ "	1C _H	0	1	1	1	0	0	V ₂₈ "	$V_8 + (V_7 - V_8) \times 3600/4000$
	1D _H	0	1	1	1	0	1	V ₂₉ "	$V_8 + (V_7 - V_8) \times 3700/4000$
	1E _H	0	1	1	1	1	0	V ₃₀ "	$V_8 + (V_7 - V_8) \times 3800/4000$
	1F _H	0	1	1	1	1	1	V ₃₁ "	$V_8 + (V_7 - V_8) \times 3900/4000$
	20 _H	1	0	0	0	0	0	V ₃₂ "	V ₇
	21 _H	1	0	0	0	0	1	V ₃₃ "	$V_7 + (V_6 - V_7) \times 100/2700$
	22 _H	1	0	0	0	1	0	V ₃₄ "	$V_7 + (V_6 - V_7) \times 200/2700$
V ₉ → V ₅₉ "	23 _H	1	0	0	0	1	1	V ₃₅ "	$V_7 + (V_6 - V_7) \times 300/2700$
	24 _H	1	0	0	1	0	0	V ₃₆ "	$V_7 + (V_6 - V_7) \times 400/2700$
	25 _H	1	0	0	1	0	1	V ₃₇ "	$V_7 + (V_6 - V_7) \times 500/2700$
	26 _H	1	0	0	1	1	0	V ₃₈ "	$V_7 + (V_6 - V_7) \times 600/2700$
	27 _H	1	0	0	1	1	1	V ₃₉ "	$V_7 + (V_6 - V_7) \times 700/2700$
	28 _H	1	0	1	0	0	0	V ₄₀ "	$V_7 + (V_6 - V_7) \times 800/2700$
	29 _H	1	0	1	0	0	1	V ₄₁ "	$V_7 + (V_6 - V_7) \times 900/2700$
V ₆ → V ₅₈ "	2A _H	1	0	1	0	1	0	V ₄₂ "	$V_7 + (V_6 - V_7) \times 1000/2700$
	2B _H	1	0	1	0	1	1	V ₄₃ "	$V_7 + (V_6 - V_7) \times 1100/2700$
	2C _H	1	0	1	1	0	0	V ₄₄ "	$V_7 + (V_6 - V_7) \times 1200/2700$
	2D _H	1	0	1	1	0	1	V ₄₅ "	$V_7 + (V_6 - V_7) \times 1300/2700$
	2E _H	1	0	1	1	1	0	V ₄₆ "	$V_7 + (V_6 - V_7) \times 1400/2700$
	2F _H	1	0	1	1	1	1	V ₄₇ "	$V_7 + (V_6 - V_7) \times 1500/2700$
	30 _H	1	1	0	0	0	0	V ₄₈ "	$V_7 + (V_6 - V_7) \times 1600/2700$
V ₇ → V ₅₇ "	31 _H	1	1	0	0	0	1	V ₄₉ "	$V_7 + (V_6 - V_7) \times 1700/2700$
	32 _H	1	1	0	0	1	0	V ₅₀ "	$V_7 + (V_6 - V_7) \times 1800/2700$
	33 _H	1	1	0	0	1	1	V ₅₁ "	$V_7 + (V_6 - V_7) \times 1900/2700$
	34 _H	1	1	0	1	0	0	V ₅₂ "	$V_7 + (V_6 - V_7) \times 2000/2700$
	35 _H	1	1	0	1	0	1	V ₅₃ "	$V_7 + (V_6 - V_7) \times 2100/2700$
	36 _H	1	1	0	1	1	0	V ₅₄ "	$V_7 + (V_6 - V_7) \times 2300/2700$
	37 _H	1	1	0	1	1	1	V ₅₅ "	$V_7 + (V_6 - V_7) \times 2500/2700$
V ₈ → V ₅₆ "	38 _H	1	1	1	0	0	0	V ₅₆ "	V ₆
	39 _H	1	1	1	0	0	1	V ₅₇ "	$V_6 + (V_5 - V_6) \times 200/2500$
	3A _H	1	1	1	0	1	0	V ₅₈ "	$V_6 + (V_5 - V_6) \times 400/2500$
	3B _H	1	1	1	0	1	1	V ₅₉ "	$V_6 + (V_5 - V_6) \times 700/2500$
	3C _H	1	1	1	1	0	0	V ₆₀ "	$V_6 + (V_5 - V_6) \times 1000/2500$
	3D _H	1	1	1	1	0	1	V ₆₁ "	$V_6 + (V_5 - V_6) \times 1300/2500$
	3E _H	1	1	1	1	1	0	V ₆₂ "	$V_6 + (V_5 - V_6) \times 1700/2500$
V ₉ → V ₅₅ "	3F _H	1	1	1	1	1	1	V ₆₃ "	V ₅

Caution Between V₄ and V₅ terminal is connected by using the resistor (9 kΩ) in the chip.

Ladder Resistance Value (r₀ to r₆₂): Reference Value

Table 1. Resistance values of the resistor strings

	Resistor Name	Resistance Value (Ω)	Resistor Name	Resistance Value (Ω)	
V ₀ , V ₉ →	r ₀	800	r ₃₂	100	← V ₂ , V ₇
	r ₁	800	r ₃₃	100	
	r ₂	800	r ₃₄	100	
	r ₃	700	r ₃₅	100	
	r ₄	700	r ₃₆	100	
	r ₅	600	r ₃₇	100	
	r ₆	500	r ₃₈	100	
V ₁ , V ₈ →	r ₇	400	r ₃₉	100	
	r ₈	400	r ₄₀	100	
	r ₉	300	r ₄₁	100	
	r ₁₀	300	r ₄₂	100	
	r ₁₁	300	r ₄₃	100	
	r ₁₂	300	r ₄₄	100	
	r ₁₃	200	r ₄₅	100	
	r ₁₄	200	r ₄₆	100	
	r ₁₅	200	r ₄₇	100	
	r ₁₆	200	r ₄₈	100	
	r ₁₇	200	r ₄₉	100	
	r ₁₈	100	r ₅₀	100	
	r ₁₉	100	r ₅₁	100	
	r ₂₀	100	r ₅₂	100	
	r ₂₁	100	r ₅₃	200	
	r ₂₂	100	r ₅₄	200	
	r ₂₃	100	r ₅₅	200	← V ₃ , V ₆
	r ₂₄	100	r ₅₆	200	
	r ₂₅	100	r ₅₇	200	
	r ₂₆	100	r ₅₈	300	
	r ₂₇	100	r ₅₉	300	
	r ₂₈	100	r ₆₀	300	
	r ₂₉	100	r ₆₁	400	
	r ₃₀	100	r ₆₂	800	← V ₄ , V ₅
V ₂ , V ₇ →	r ₃₁	100	Total	14500	

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 6 bits × 2 RGBs (6 dots)

Input width : 36 bits (2-pixel data)

$R/\bar{L} = H$ (Right shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₁₁	S ₃₁₂
Data	D ₀₀ -D ₀₅	D ₁₀ -D ₁₅	D ₂₀ -D ₂₅	D ₃₀ -D ₃₅	...	D ₄₀ -D ₄₅	D ₅₀ -D ₅₅

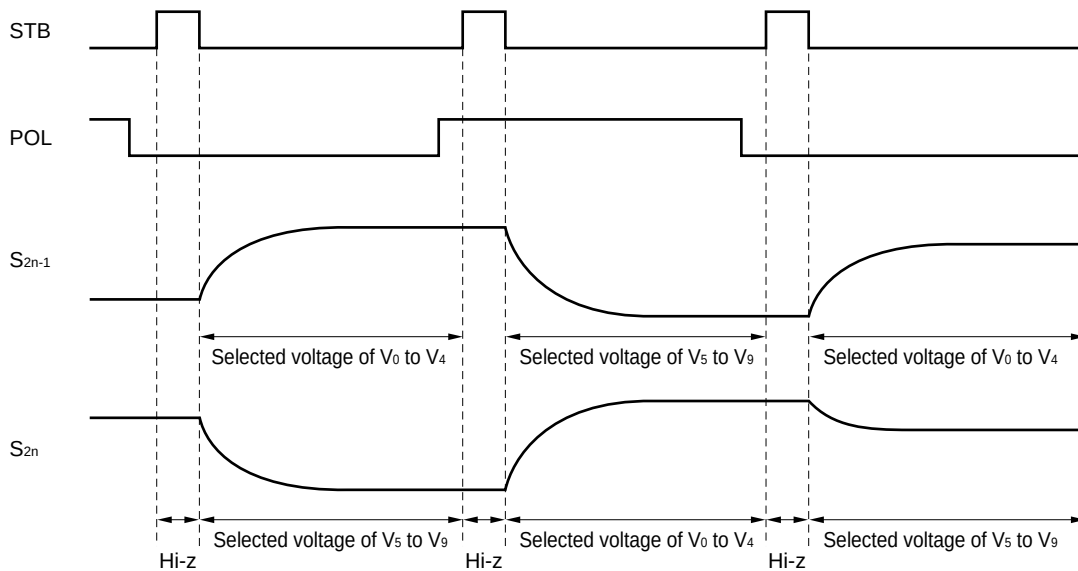
$R/\bar{L} = L$ (Left shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₁₁	S ₃₁₂
Data	D ₀₀ -D ₀₅	D ₁₀ -D ₁₅	D ₂₀ -D ₂₅	D ₃₀ -D ₃₅	...	D ₄₀ -D ₄₅	D ₅₀ -D ₅₅

S_{2n-1} (Odd output), S_{2n} (Even output) n = 1, 2, ..., 156

POL	S _{2n-1}	S _{2n}
L	V ₀ to V ₄	V ₅ to V ₉
H	V ₅ to V ₉	V ₀ to V ₄

7. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

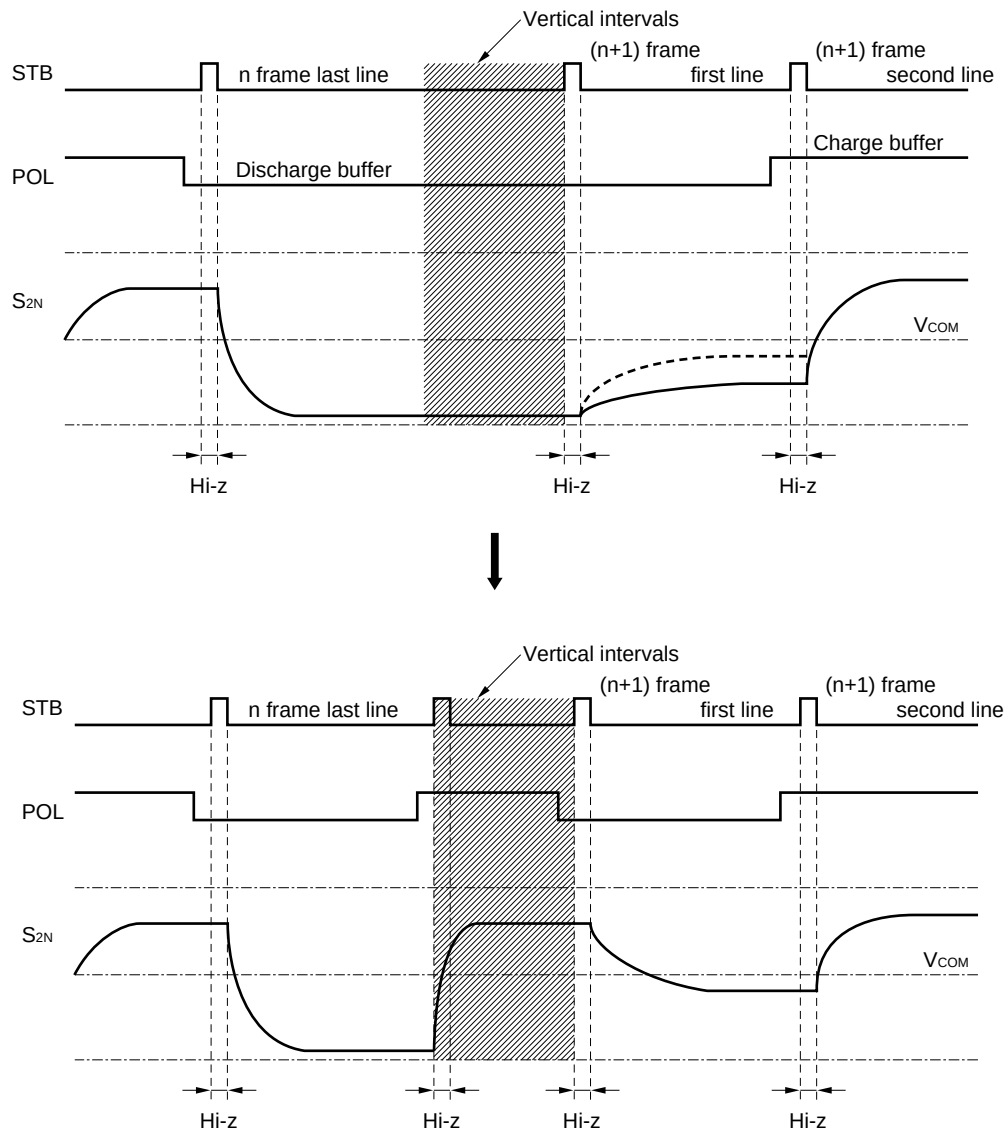


8. CAUTIONS ABOUT FRAME INVERSION

In the case of dot inversion, n frame last line and (n+1) frame first line is the same polarity.
When write the same polarity twice, there are two cases as follows.

- (1) last line output in n frame > first line output in (n+1) frame → Possible to write
- (2) last line output in n frame < first line output in (n+1) frame → Not possible to write

μPD16633B has charge buffer and discharge buffer, so need to inversion polarity and write in the case of both ways.



9. ELECTRIC SPECIFICATION

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	-0.5 to +6.5	V
Driver Part Supply Voltage	V_{DD2}	-0.5 to +15.0	V
Logic Part Input Voltage	V_{I1}	-0.5 to $V_{DD1} + 0.5$	V
Driver Part Input Voltage	V_{I2}	-0.5 to $V_{DD2} + 0.5$	V
Logic Part Output Voltage	V_{O1}	-0.5 to $V_{DD1} + 0.5$	V
Driver Part Output Voltage	V_{O2}	-0.5 to $V_{DD2} + 0.5$	V
Operating Temperature Range	T_A	-10 to +75	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +125	$^\circ\text{C}$

Recommended Operating Condition ($T_A = -10\text{ to }+75^\circ\text{C}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Driver Part Supply Voltage	V_{DD2}	10.0	10.5	13.5	V
High-Level Input Voltage	V_{IH}	$0.7V_{DD1}$		V_{DD1}	V
Low-Level Input Voltage	V_{IL}	V_{SS1}		$0.3V_{DD1}$	V
γ -Corrected Voltage	V_0 to V_9	$V_{SS2} + 0.05$		$V_{DD2} - 0.05$	V
Driver Part Output Voltage	V_O	$V_{SS2} + 0.1$		$V_{DD2} - 0.1$	V
Maximum Clock Frequency	$f_{\text{max.}}$	45			MHz

Electrical Specifications ($T_A = -10\text{ to }+75^\circ\text{C}$, $V_{DD1} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DD2} = 10.5\text{ V} \pm 0.5\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Leak Current	I_{IL}				± 1.0	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), $I_{OH} = 0\text{ mA}$	$V_{DD1} - 0.1$			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), $I_{OL} = 0\text{ mA}$			0.1	V
γ -Corrected Supply Current	I_γ	$V_0-V_9 = 10\text{ V}$ V_0, V_9		0.3	0.5	mA
Driver Output Current	V_{VOH}	$V_X = 9\text{ V}$, $V_{OUT} = 3\text{ V}$ ^{Note}		-0.6	-0.3	mA
	V_{VOL}	$V_X = 3\text{ V}$, $V_{OUT} = 9\text{ V}$ ^{Note}	0.3	0.6		mA

Note V_X refers to the output voltage of analog output pins S_1 to S_{312} .

V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{312} .

Electrical Specifications ($T_A = -10$ to $+75^\circ\text{C}$, $V_{DD1} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DD2} = 10.5\text{ V} \pm 0.5\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output Voltage Deviation ^{Note 1}	ΔV_O	Input data		± 5	± 20	mV
Average Output Voltage Variation ^{Note 2}	ΔV_{AV}	Input data		± 10		mV
Output Voltage Range	V_O	Input data	0.1		$V_{DD2} - 0.1$	V
Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1} , No loads		1.6	10.0	mA
Driver Part Dynamic Current Consumption 1 ^{Notes 3, 4}	I_{DD21}	$V_{DD2} = 10.5\text{ V} \pm 0.5\text{ V}$, No loads		4.4	8.0	mA
Driver Part Dynamic Current Consumption 1 ^{Notes 3, 4}	I_{DD22}	$V_{DD2} = 13.5\text{ V} \pm 0.5\text{ V}$, No loads		6.4	10.0	mA

- Notes 1.** The output voltage deviation refers to the voltage difference between adjoining output pins when the display data is the same (within the chip).
- 2.** The average output voltage variation refers to the average output voltage difference between chips. The average output voltage refers to the average voltage between chips when the display data is the same.
- 3.** The STB cycle is defined to be $20\text{ }\mu\text{s}$ at $f_{CLK} = 40\text{ MHz}$. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.
- 4.** Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (10 units).

Switching Characteristics ($T_A = -10$ to $+75^\circ\text{C}$, $V_{DD1} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DD2} = 10.5\text{ V} \pm 0.5\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

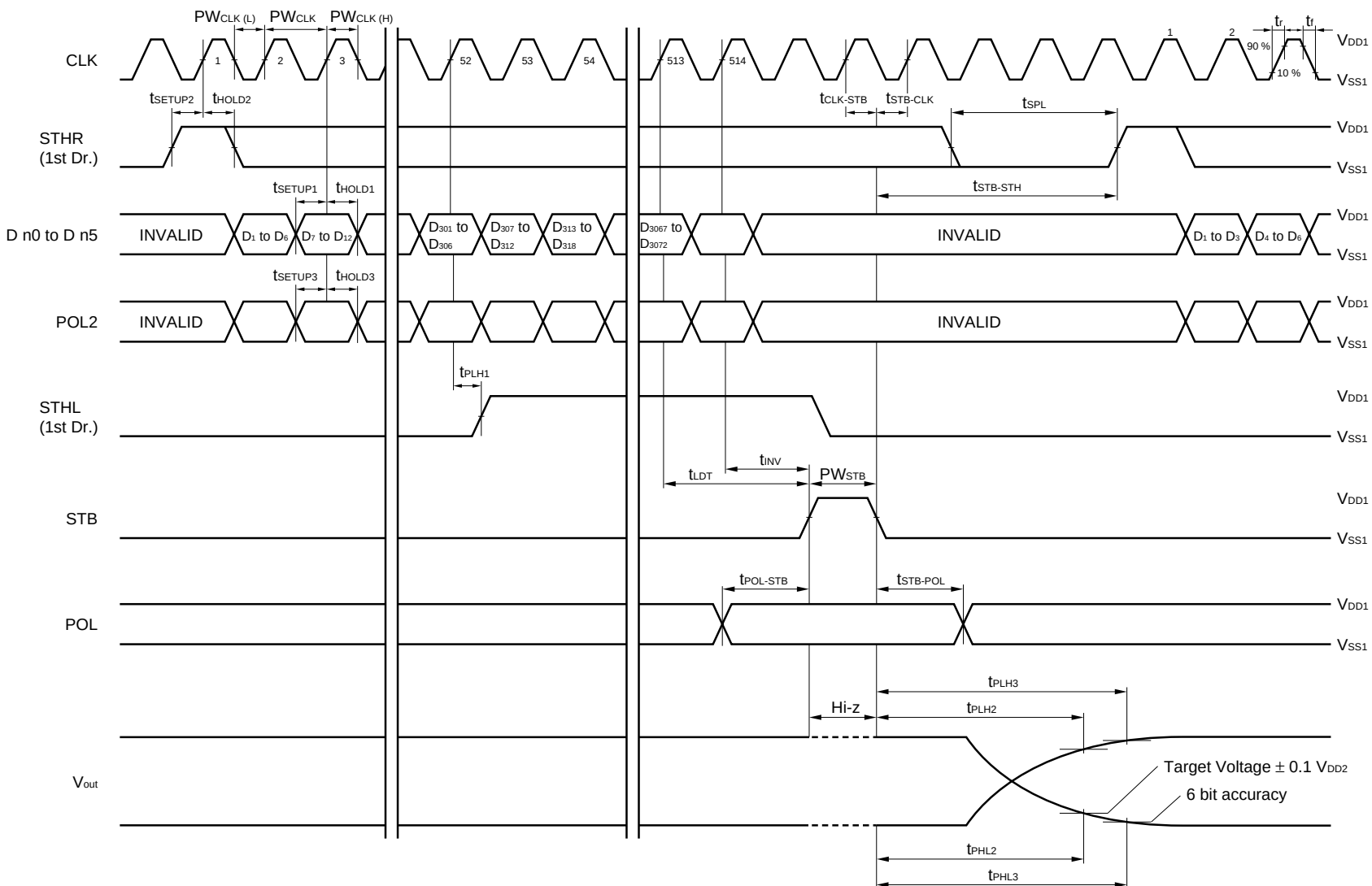
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	$C_L = 25\text{ pF}$		10	15	ns
Driver Output Delay Time 1	t_{PLH2}	$C_L = 50\text{ pF}$, $R_L = 50\text{ k}\Omega$		6.6	11	μs
Driver Output Delay Time 2	t_{PLH3}	$C_L = 50\text{ pF}$, $R_L = 50\text{ k}\Omega$		10	17	μs
Driver Output Delay Time 3	t_{PHL2}	$C_L = 50\text{ pF}$, $R_L = 50\text{ k}\Omega$		6.4	11	μs
Driver Output Delay Time 4	t_{PHL3}	$C_L = 50\text{ pF}$, $R_L = 50\text{ k}\Omega$		9.1	17	μs
Input Capacitance 1	C_{i1}	STHR (STHL) excluded, $T_A = 25^\circ\text{C}$		6.4	15	pF
Input Capacitance 2	C_{i2}	STHR (STHL), $T_A = 25^\circ\text{C}$		6.3	15	pF

Timing Requirement ($T_A = -10$ to $+75^\circ\text{C}$, $V_{DD1} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$, $t_r = t_f = 8.0\text{ ns}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		22			ns
Clock Pulse Low Period	$PW_{CLK(H)}$		6			ns
Clock Pulse High Period	$PW_{CLK(L)}$		6			ns
Data Setup Time	t_{SETUP1}		6			ns
Data Hold Time	t_{HOLD1}		6			ns
Start Pulse Setup Time	t_{SETUP2}		6			ns
Start Pulse Hold Time	t_{HOLD2}		6			ns
POL2 Setup Time	t_{SETUP3}		6			ns
POL2 Hold Time	t_{HOLD3}		6			ns
Start Pulse Low Period	t_{SPL}		5			ns
STB Pulse Width	PW_{STB}		0.5			μs
Data Invalid Period	t_{INV}		1			CLK
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK $\uparrow \rightarrow$ STB $\downarrow$	5			ns
STB-CLK Time	$t_{STB-CLK}$	STB $\downarrow \rightarrow$ CLK $\downarrow$	5			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB $\downarrow \rightarrow$ STHR (L) $\uparrow$	50			ns
POL-STB Time	$t_{POL-STB}$	POL $\uparrow$ or $\downarrow \rightarrow$ STB $\uparrow$	-5			ns
STB-POL Time	$t_{STB-POL}$	STB $\downarrow \rightarrow$ POL $\downarrow$ or $\uparrow$	5			ns

10. SWITCHING CHARACTERISTICS WAVEFORM (R/L = H)

Unless otherwise specified, the input level is defined to be $V_{IH} = 0.5V_{DD1}$



11. RECOMMENDED MOUNTING CONDITIONS

When mounting this product, please make sure that the following recommended conditions are satisfied.

For packaging methods and conditions other than those recommended below, please contact NEC sales personnel.

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 sec; pressure 100 g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C; pressure 3 to 8 kg/cm ² ; time 3 to 5 sec. Real bonding 165 to 180°C; pressure 25 to 45 kg/cm ² , time 30 to 40 secs. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

Reference

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)

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