

74ALVC164245

16-bit dual supply translating transceiver; 3-state

Rev. 04 — 11 November 2008

Product data sheet

1. General description

The 74ALVC164245 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC164245 is a 16-bit (dual octal) dual supply translating transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V and 5 V bus in a mixed 3 V and 5 V supply environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The direction control inputs (1DIR and 2DIR) determine the direction of the data flow. nDIR (active HIGH) enables data from nA ports to nB ports. nDIR (active LOW) enables data from nB ports to nA ports. The output enable inputs ($1\overline{OE}$ and $2\overline{OE}$), when HIGH, disable both nA and nB ports by placing them in a high-impedance OFF-state. Pins nA, $\overline{nOE}$ and nDIR are referenced to $V_{CC(A)}$ and pins nB are referenced to $V_{CC(B)}$.

In suspend mode, when one of the supply voltages is zero, there will be no current flow from the non-zero supply towards the zero supply. The A-outputs must be set 3-state and the voltage on the A-bus must be smaller than V_{diode} (typical 0.7 V). $V_{CC(B)} \geq V_{CC(A)}$ (except in suspend mode).

2. Features

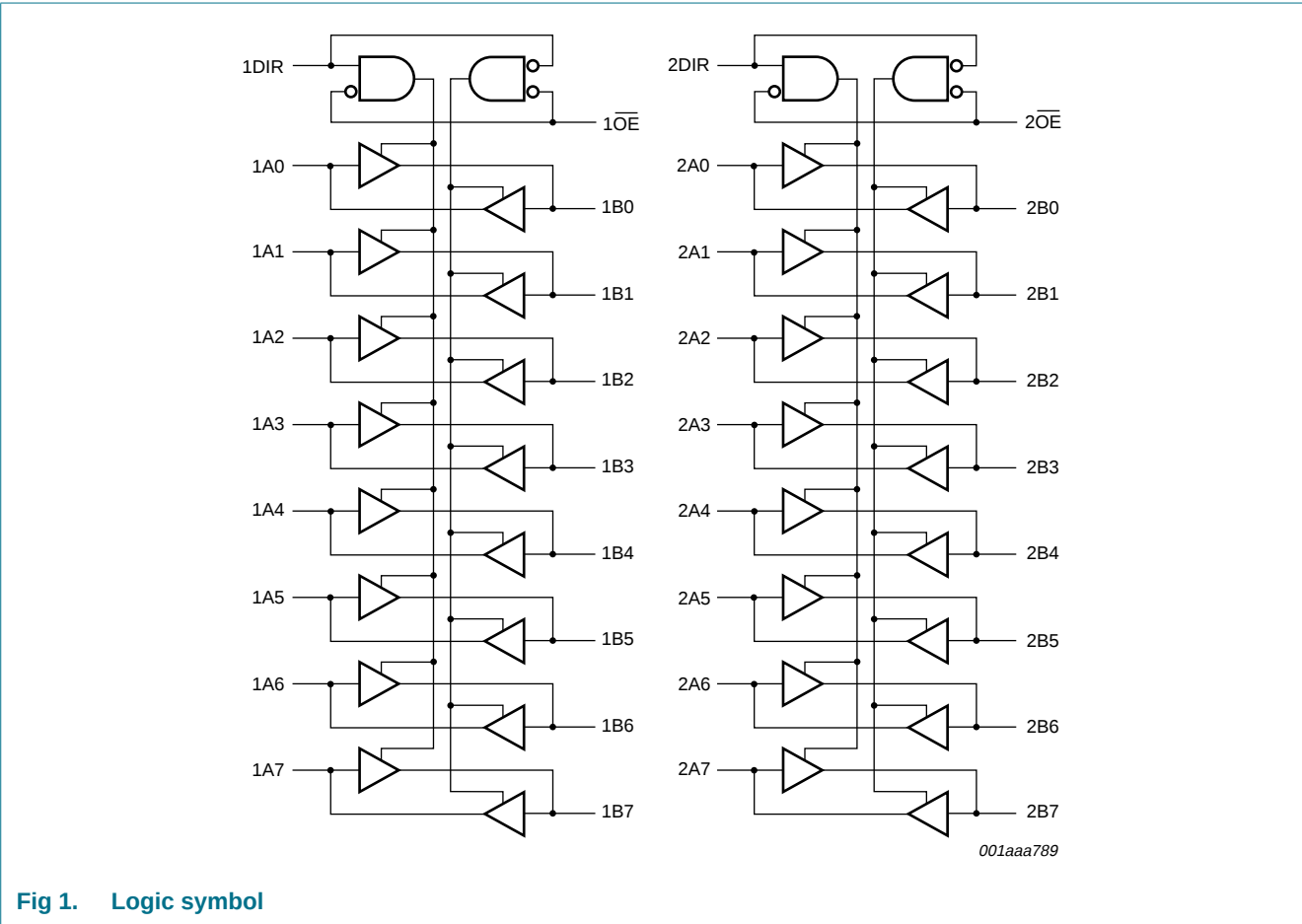
- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range:
 - ◆ 3 V port ($V_{CC(A)}$): 1.5 V to 3.6 V
 - ◆ 5 V port ($V_{CC(B)}$): 1.5 V to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Control inputs voltage range from 2.7 V to 5.5 V
- Inputs accept voltages up to 5.5 V
- High-impedance outputs when $V_{CC(A)}$ or $V_{CC(B)} = 0$ V
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from -40°C to $+85^{\circ}\text{C}$ and -40°C to $+125^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74ALVC164245DL	−40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74ALVC164245DGG	−40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74ALVC164245BQ	−40 °C to +125 °C	HUQFN60U	plastic thermal enhanced ultra thin quad flat package; no leads; 60 terminals; UTLP based; body 4 x 6 x 0.55 mm	SOT1025-1

4. Functional diagram



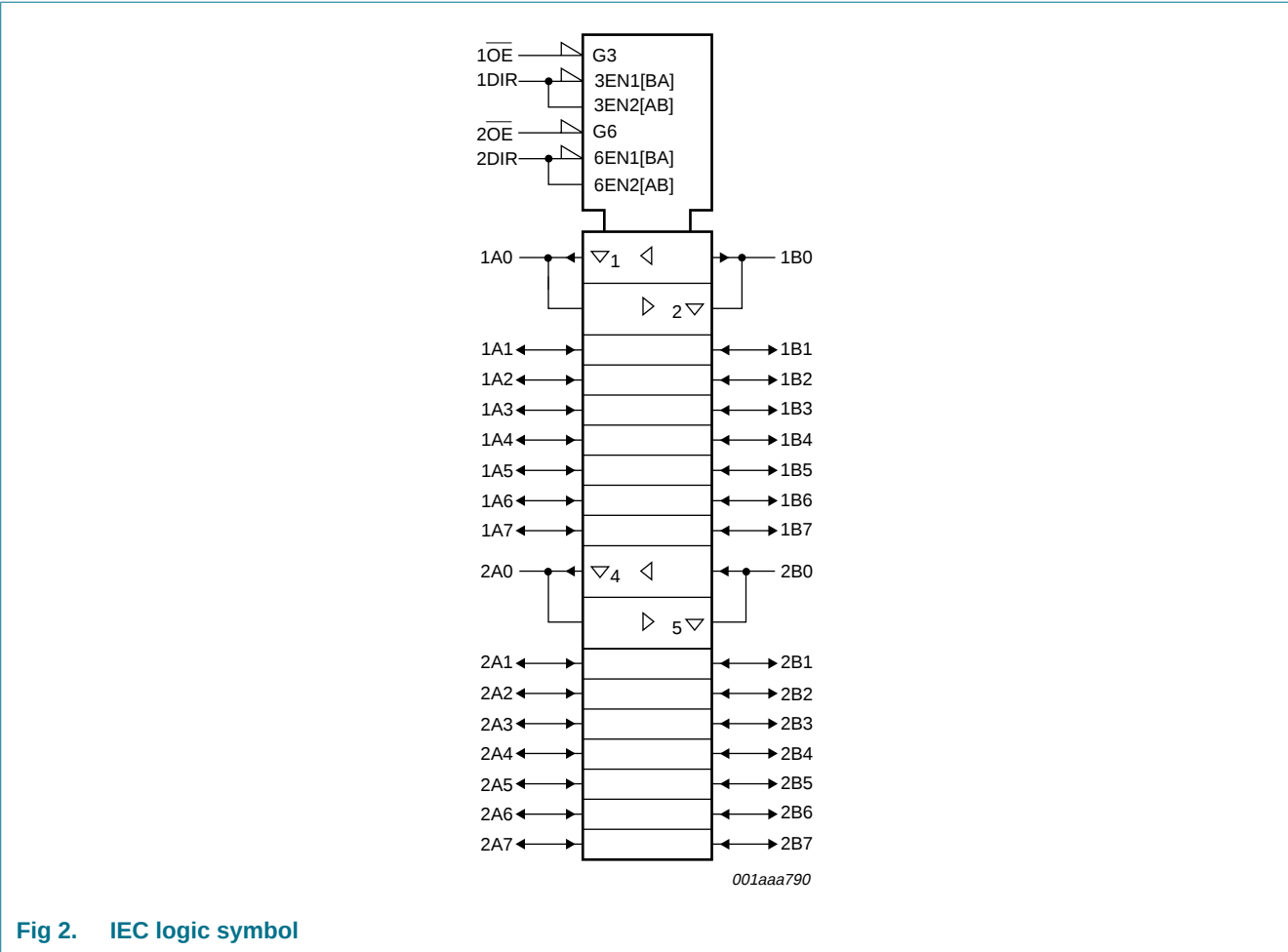
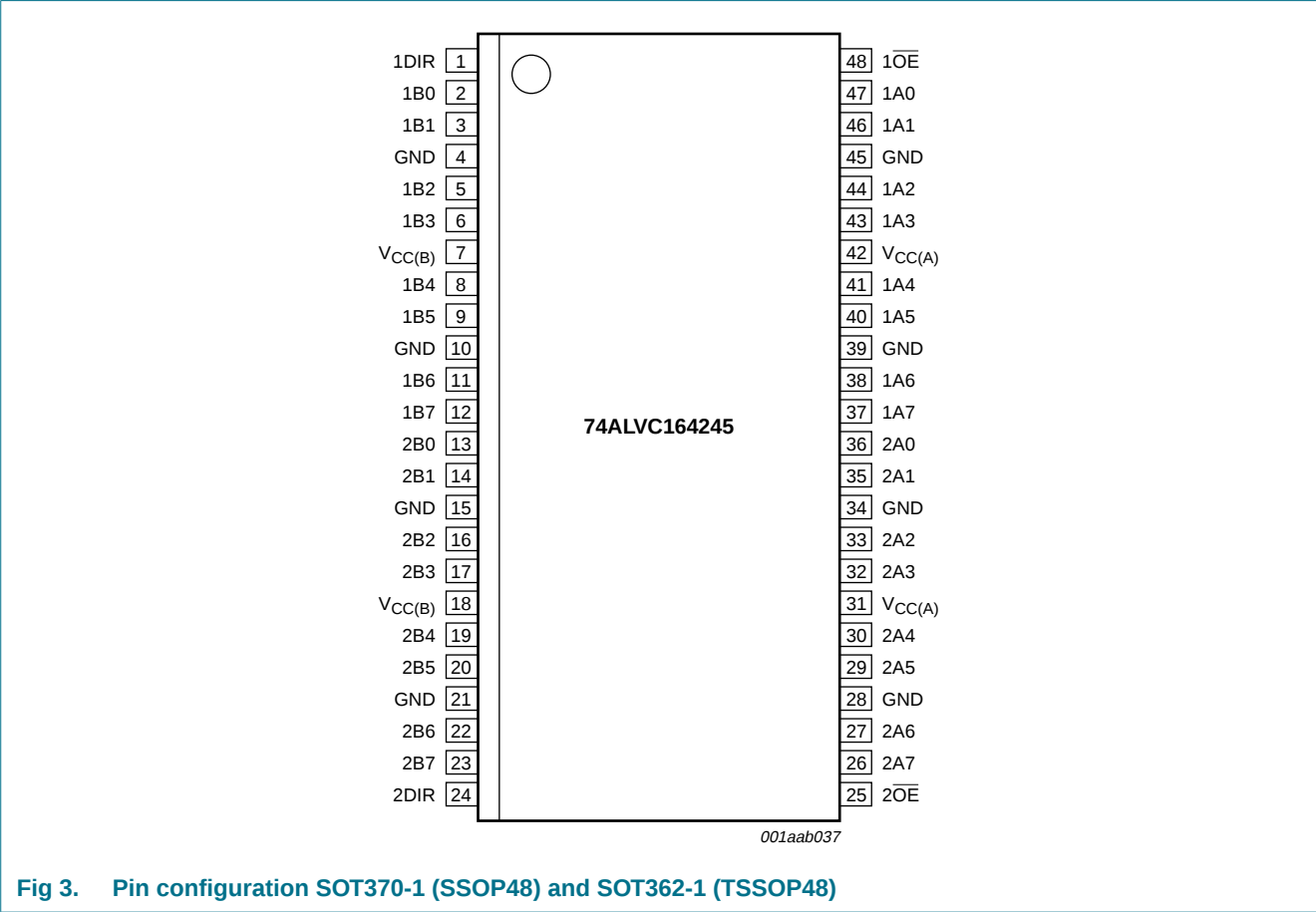
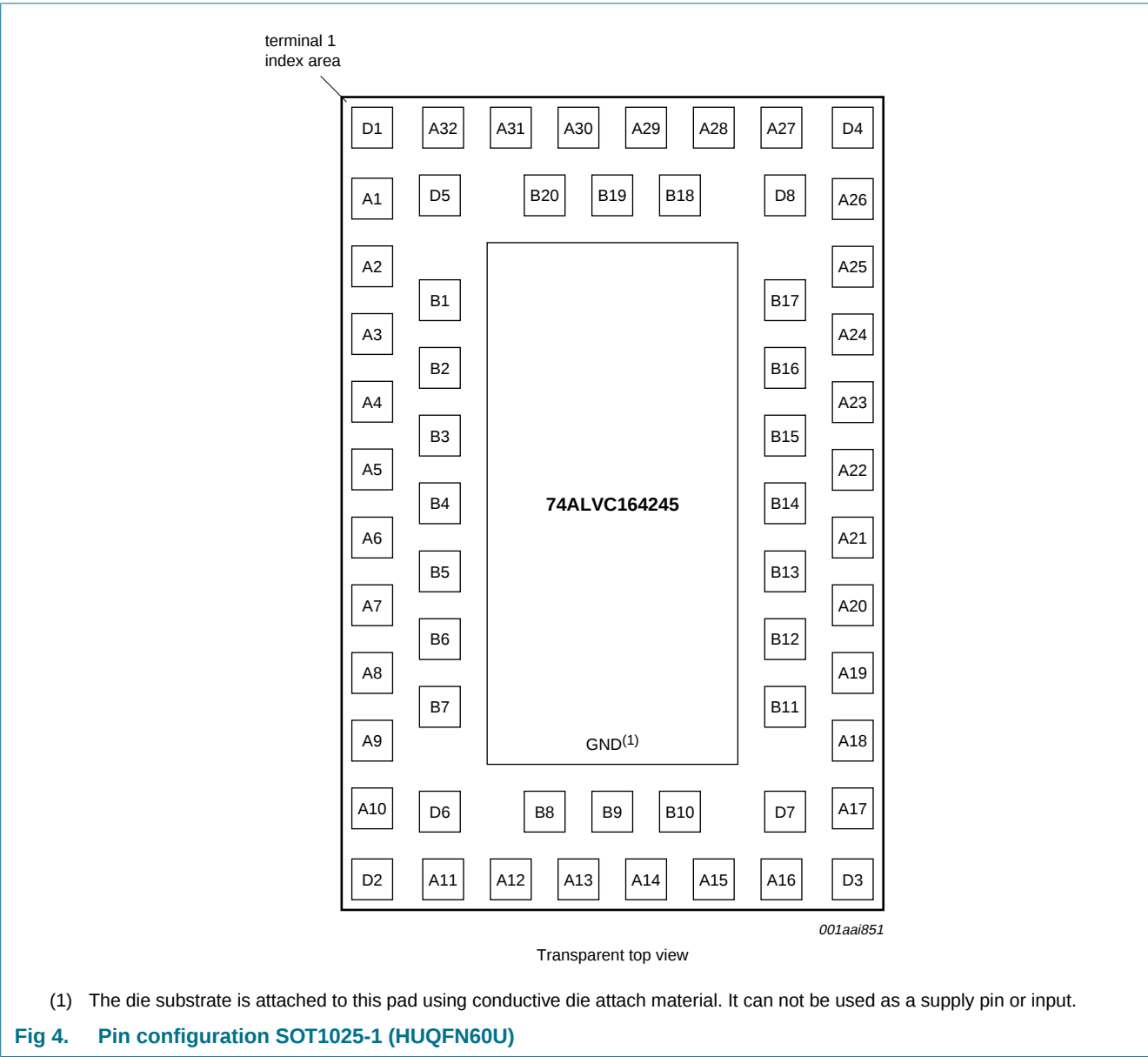


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning





5.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	SOT370-1 and SOT362-1	SOT1025-1	
1DIR, 2DIR	1, 24	A30, A13	direction control input
1B0 to 1B7	2, 3, 5, 6, 8, 9, 11, 12	B20, A31, D5, D1, A2, B2, B3, A5	data input/output
2B0 to 2B7	13, 14, 16, 17, 19, 20, 22, 23	A6, B5, B6, A9, D2, D6, A12, B8	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	A32, A3, A8, A11, A16, A19, A24, A27	ground (0 V)
V _{CC(B)}	7, 18	A1, A10,	supply voltage B (5 V bus)
1 $\overline{\text{OE}}$, 2 $\overline{\text{OE}}$	48, 25	A29, A14	output enable input (active LOW)
1A0 to 1A7	47, 46, 44, 43, 41, 40, 38, 37	B18, A28, D8, D4, A25, B16, B15, A22	data input/output
2A0 to 2A7	36, 35, 33, 32, 30, 29, 27, 26	A21, B13, B12, A18, D3, D7, A15, B10	data input/output
V _{CC(A)}	31, 42	A17, A26	supply voltage A (3 V bus)
n.c.	-	A4, A7, A20, A23, B1, B4, B7, B9, B11, B14, B17, B19	not connected

6. Functional description

Table 3. Function table^[1]

Inputs		Outputs	
n $\overline{\text{OE}}$	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V). See Table note 1.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC(B)}	supply voltage B	V _{CC(B)} ≥ V _{CC(A)}	-0.5	+6.0	V
V _{CC(A)}	supply voltage A	V _{CC(B)} ≥ V _{CC(A)}	-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		^[2] -0.5	+6.0	V
V _{I/O}	input/output voltage		-0.5	V _{CC} + 0.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	output HIGH or LOW	^[2] -0.5	V _{CC} + 0.5	V
		output 3-state	^[2] -0.5	+6.0	V
I _{O(sink/source)}	output sink or source current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V). See Table note 1.

Symbol	Parameter	Conditions	Min	Max	Unit
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{\text{amb}} = -40\text{ °C to }+125\text{ °C}$			
		(T)SSOP48 package	[3] -	500	mW
		HUQFN60U package	[4] -	1000	mW

- [1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- [2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [3] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
- [4] Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{\text{CC(B)}}$	supply voltage B	$V_{\text{CC(B)}} \geq V_{\text{CC(A)}}$				
		maximum speed performance	2.7	-	5.5	V
		low-voltage applications	1.5	-	5.5	V
$V_{\text{CC(A)}}$	supply voltage A	$V_{\text{CC(B)}} \geq V_{\text{CC(A)}}$				
		maximum speed performance	2.7	-	3.6	V
		low-voltage applications	1.5	-	3.6	V
V_{I}	input voltage	control inputs: $\overline{\text{nOE}}$ and nDIR	0	-	5.5	V
$V_{\text{I/O}}$	input/output voltage	A port	0	-	$V_{\text{CC(A)}}$	V
		B port	0	-	$V_{\text{CC(B)}}$	V
V_{O}	output voltage	A port	0	-	$V_{\text{CC(A)}}$	V
		B port	0	-	$V_{\text{CC(B)}}$	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{\text{CC(A)}} = 2.7\text{ V to }3.0\text{ V}$	0	-	20	ns/V
		$V_{\text{CC(A)}} = 3.0\text{ V to }3.6\text{ V}$	0	-	10	ns/V
		$V_{\text{CC(B)}} = 3.0\text{ V to }4.5\text{ V}$	0	-	20	ns/V
		$V_{\text{CC(B)}} = 4.5\text{ V to }5.5\text{ V}$	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{IH}	HIGH-level input voltage	B port							
		V _{CC(B)} = 3.0 V to 5.5 V [2]	2.0	-	-	2.0	-	-	V
		A port, n $\overline{\text{OE}}$ and nDIR							
		V _{CC(A)} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC(A)} = 2.3 V to 2.7 V [2]	1.7	-	-	1.7	-	-	V
		B port							
		V _{CC(B)} = 4.5 V to 5.5 V [2]	-	-	0.8	-	-	0.8	V
		V _{CC(B)} = 3.0 V to 3.6 V [2]	-	-	0.7	-	-	0.7	V
		A port, n $\overline{\text{OE}}$ and nDIR							
		V _{CC(A)} = 3.0 V to 3.6 V	-	-	0.8	-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _{CC(A)} = 2.3 V to 2.7 V [2]	-	-	0.7	-	-	0.7	V
		B port; V _I = V _{IH} or V _{IL}							
		I _O = -24 mA; V _{CC(B)} = 4.5 V	V _{CC(B)} - 0.8	-	-	V _{CC(B)} - 1.2	-	-	V
		I _O = -12 mA; V _{CC(B)} = 4.5 V	V _{CC(B)} - 0.5	-	-	V _{CC(B)} - 0.8	-	-	V
		I _O = -18 mA; V _{CC(B)} = 3.0 V	V _{CC(B)} - 0.8	-	-	V _{CC(B)} - 1.0	-	-	V
		I _O = -100 μ A; V _{CC(B)} = 3.0 V	V _{CC(B)} - 0.2	V _{CC(B)}	-	V _{CC(B)} - 0.3	V _{CC(B)}	-	V
		A port; V _I = V _{IH} or V _{IL}							
		I _O = -24 mA; V _{CC(A)} = 3.0 V	V _{CC(A)} - 0.7	-	-	V _{CC(A)} - 1.0	-	-	V
		I _O = -100 μ A; V _{CC(A)} = 3.0 V	V _{CC(A)} - 0.2	-	-	V _{CC(A)} - 0.3	-	-	V
		I _O = -12 mA; V _{CC(A)} = 2.7 V	V _{CC(A)} - 0.5	-	-	V _{CC(A)} - 0.8	-	-	V
		I _O = -8 mA; V _{CC(A)} = 2.3 V	V _{CC(A)} - 0.6	-	-	V _{CC(A)} - 0.6	-	-	V
		I _O = -100 μ A; V _{CC(A)} = 2.3 V	V _{CC(A)} - 0.2	V _{CC(A)}	-	V _{CC(A)} - 0.3	V _{CC(A)}	-	V
V _{OL}	LOW-level output voltage	B port; V _I = V _{IH} or V _{IL}							
		I _O = 24 mA; V _{CC(B)} = 4.5 V	-	-	0.55	-	-	0.60	V
		I _O = 12 mA; V _{CC(B)} = 4.5 V	-	-	0.40	-	-	0.80	V
		I _O = 100 μ A; V _{CC(B)} = 4.5 V	-	-	0.20	-	-	0.30	V
		I _O = 18 mA; V _{CC(B)} = 3.0 V	-	-	0.55	-	-	0.80	V
		I _O = 100 μ A; V _{CC(B)} = 3.0 V	-	-	0.20	-	-	0.30	V
		A port; V _I = V _{IH} or V _{IL}							
		I _O = 24 mA; V _{CC(A)} = 3.0 V	-	-	0.55	-	-	0.80	V
		I _O = 100 μ A; V _{CC(A)} = 3.0 V	-	-	0.20	-	-	0.30	V
		I _O = 12 mA; V _{CC(A)} = 2.7 V	-	-	0.40	-	-	0.60	V
		I _O = 12 mA; V _{CC(A)} = 2.3 V	-	-	0.60	-	-	0.60	V
		I _O = 100 μ A; V _{CC(A)} = 2.3 V	-	-	0.20	-	-	0.20	V

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Typ	Max	
I _I	input leakage current	V _I = 5.5 V or GND	-	±0.1	±5	-	±0.1	±10	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	-	±0.1	±10	-	±0.1	±20	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A	-	0.1	40	-	0.1	80	μA
ΔI _{CC}	additional supply current	per control pin; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5	5000	μA
C _I	input capacitance		-	4.0	-	-	-	-	pF
C _{I/O}	input/output capacitance	A and B port	-	5.0	-	-	-	-	pF

[1] All typical values are measured at V_{CC(B)} = 5.0 V, V_{CC(A)} = 3.3 V and T_{amb} = 25 °C.[2] If V_{CC(A)} < 2.7 V, the switching levels at all inputs are not TTL compatible.[3] For transceivers, the parameter I_{OZ} includes the input leakage current.[4] V_{CC(A)} = 2.7 V to 3.6 V: other inputs at V_{CC(A)} or GND; V_{CC(B)} = 4.5 V to 5.5 V: other inputs at V_{CC(B)} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristicsGND = 0 V; t_r = t_f ≤ 2.5 ns; C_L = 50 pF; for test circuit see Figure 7.

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nAn to nBn; see Figure 5						
		V _{CC(A)} = 2.3 V to 2.7 V; V _{CC(B)} = 3.0 V tot 3.6 V	1.5	3.3	7.6	1.5	9.5	ns
		V _{CC(A)} = 2.7 V; V _{CC(B)} = 4.5 V to 5.5 V	1.0	3.0	5.9	1.0	7.5	ns
		V _{CC(A)} = 3.0 V to 3.6 V; V _{CC(B)} = 4.5 V to 5.5 V	1.0	2.9	5.8	1.0	7.5	ns
		nBn to nAn; see Figure 5						
		V _{CC(A)} = 2.3 V to 2.7 V; V _{CC(B)} = 3.0 V tot 3.6 V	1.0	3.0	7.6	1.0	9.5	ns
		V _{CC(A)} = 2.7 V; V _{CC(B)} = 4.5 V to 5.5 V	1.0	4.3	6.7	1.0	8.5	ns
		V _{CC(A)} = 3.0 V to 3.6 V; V _{CC(B)} = 4.5 V to 5.5 V	1.2	2.5	5.8	1.2	7.5	ns

Table 7. Dynamic characteristics ...continuedGND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{en}	enable time	nOE to nBn; see Figure 6 ^[2]						
		V _{CC(A)} = 2.3 V to 2.7 V; V _{CC(B)} = 3.0 V tot 3.6 V	1.5	4.1	11.5	1.5	14.5	ns
		V _{CC(A)} = 2.7 V; V _{CC(B)} = 4.5 V to 5.5 V	1.5	3.6	9.2	1.5	11.5	ns
		V _{CC(A)} = 3.0 V to 3.6 V; V _{CC(B)} = 4.5 V to 5.5 V	1.0	3.2	8.9	1.0	12.0	ns
		nOE to nAn; see Figure 6 ^[2]						
		V _{CC(A)} = 2.3 V to 2.7 V; V _{CC(B)} = 3.0 V tot 3.6 V	1.5	4.6	12.3	1.5	15.5	ns
		V _{CC(A)} = 2.7 V; V _{CC(B)} = 4.5 V to 5.5 V	1.5	4.3	9.3	1.5	12.0	ns
		V _{CC(A)} = 3.0 V to 3.6 V; V _{CC(B)} = 4.5 V to 5.5 V	1.0	3.2	8.9	1.0	11.5	ns
t _{dis}	disable time	nOE to nBn; see Figure 6 ^[2]						
		V _{CC(A)} = 2.3 V to 2.7 V; V _{CC(B)} = 3.0 V tot 3.6 V	2.0	2.7	10.5	2.0	13.5	ns
		V _{CC(A)} = 2.7 V; V _{CC(B)} = 4.5 V to 5.5 V	2.5	4.6	9.0	2.5	11.5	ns
		V _{CC(A)} = 3.0 V to 3.6 V; V _{CC(B)} = 4.5 V to 5.5 V	2.1	4.9	8.6	2.1	11.0	ns
		nOE to nAn; see Figure 6 ^[2]						
		V _{CC(A)} = 2.3 V to 2.7 V; V _{CC(B)} = 3.0 V tot 3.6 V	1.0	2.7	9.3	1.0	12.0	ns
		V _{CC(A)} = 2.7 V; V _{CC(B)} = 4.5 V to 5.5 V	1.5	3.5	9.0	1.5	11.5	ns
		V _{CC(A)} = 3.0 V to 3.6 V; V _{CC(B)} = 4.5 V to 5.5 V	2.0	3.2	8.6	2.0	11.0	ns

Table 7. Dynamic characteristics ...continued

$GND = 0\text{ V}$; $t_r = t_f \leq 2.5\text{ ns}$; $C_L = 50\text{ pF}$; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	$T_{\text{amb}} = -40\text{ °C to }+85\text{ °C}$			$T_{\text{amb}} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ ^[1]	Max	Min	Max	
C_{PD}	power dissipation capacitance	5 V port: nAn to nBn; [3][4] $V_{CC(B)} = 5\text{ V}$; $V_{CC(A)} = 3.3\text{ V}$						
		outputs enabled	-	30	-	-	-	pF
		outputs disabled	-	15	-	-	-	pF
		3 V port: nBn to nAn; [3][4] $V_{CC(B)} = 5\text{ V}$; $V_{CC(A)} = 3.3\text{ V}$						
		outputs enabled	-	40	-	-	-	pF
		outputs disabled	-	5	-	-	-	pF

[1] All typical values are measured at nominal voltage for $V_{CC(B)}$ and $V_{CC(A)}$ and at $T_{\text{amb}} = 25\text{ °C}$.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

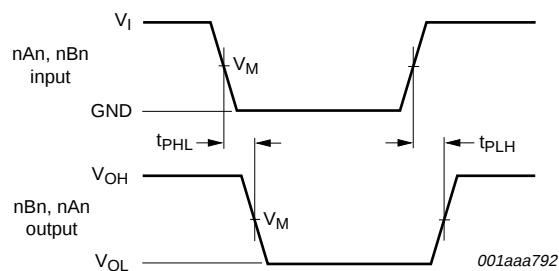
V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[4] The condition is $V_I = GND$ to V_{CC} .

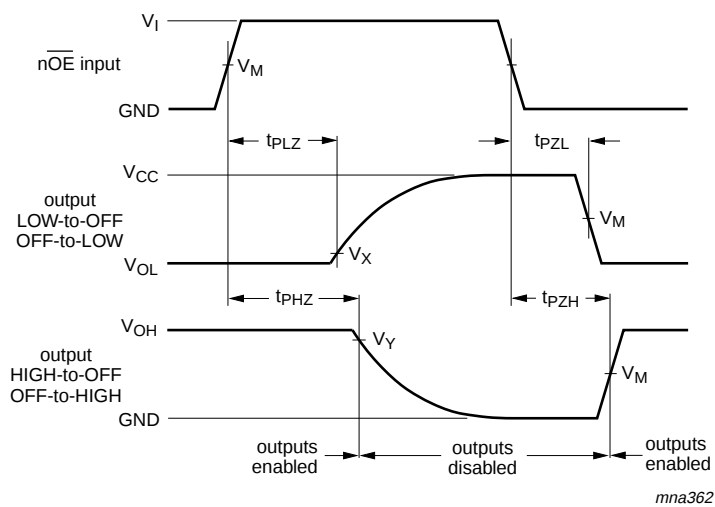
11. AC waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. Input (nAn, nBn) to output (nBn, nAn) propagation delays



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with output load.

Fig 6. 3-state enable and disable times

Table 8. Measurement points

Direction	Supply voltage		Input		Output		
	$V_{CC(A)}$	$V_{CC(B)}$	V_I	V_M	V_M	V_X	V_Y
A port to B port	2.3 V to 2.7 V	2.7 V to 3.6 V	$V_{CC(A)}$	$0.5 \times V_{CC(A)}$	1.5 V	$V_{OL(B)} + 0.3 \text{ V}$	$V_{OH(B)} - 0.3 \text{ V}$
B port to A port	2.3 V to 2.7 V	2.7 V to 3.6 V	2.7 V	1.5 V	$0.5 \times V_{CC(A)}$	$V_{OL(A)} + 0.15 \text{ V}$	$V_{OH(A)} - 0.15 \text{ V}$
A port to B port	2.7 V to 3.6 V	4.5 V to 5.5 V	2.7 V	1.5 V	$0.5 \times V_{CC(B)}$	$0.2 \times V_{CC(B)}$	$0.8 \times V_{CC(B)}$
B port to A port	2.7 V to 3.6 V	4.5 V to 5.5 V	3.0 V	1.5 V	1.5 V	$V_{OL(A)} + 0.3 \text{ V}$	$V_{OH(A)} - 0.3 \text{ V}$

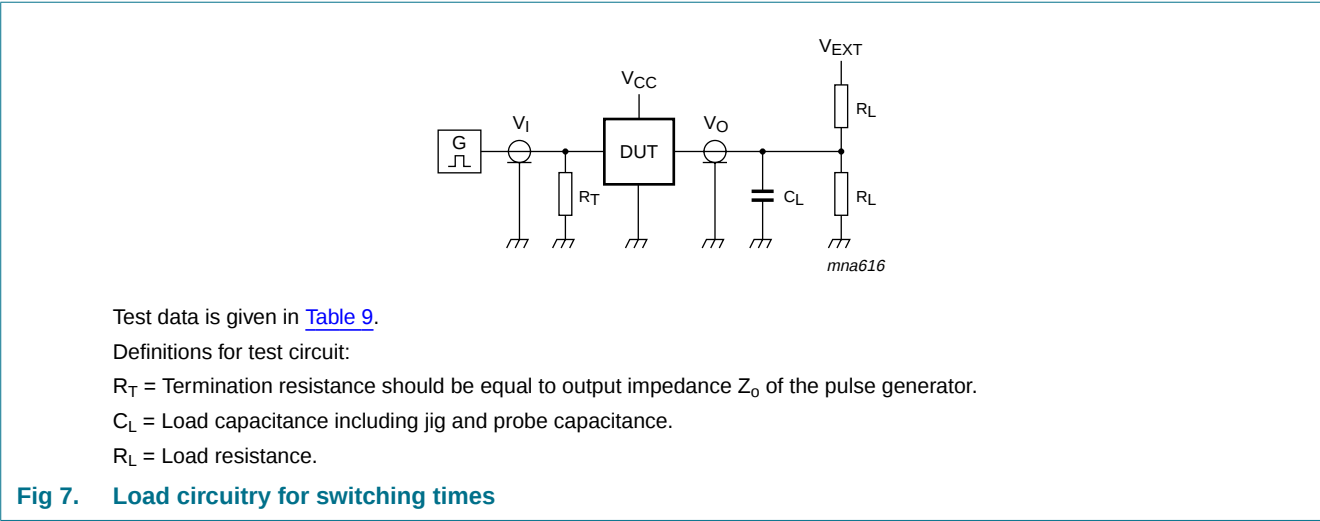


Table 9. Test data

Direction	Supply voltage		Load		V _{EXT}		
	V _{CC(A)}	V _{CC(B)}	C _L	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
A port to B port	2.3 V to 2.7 V	2.7 V to 3.6 V	50 pF	500 Ω	open	GND	2 × V _{CC}
B port to A port	2.3 V to 2.7 V	2.7 V to 3.6 V	50 pF	500 Ω	open	GND	6.0 V
A port to B port	2.7 V to 3.6 V	4.5 V to 5.5 V	50 pF	500 Ω	open	GND	2 × V _{CC}
B port to A port	2.7 V to 3.6 V	4.5 V to 5.5 V	50 pF	500 Ω	open	GND	6.0 V

12. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm SOT370-1

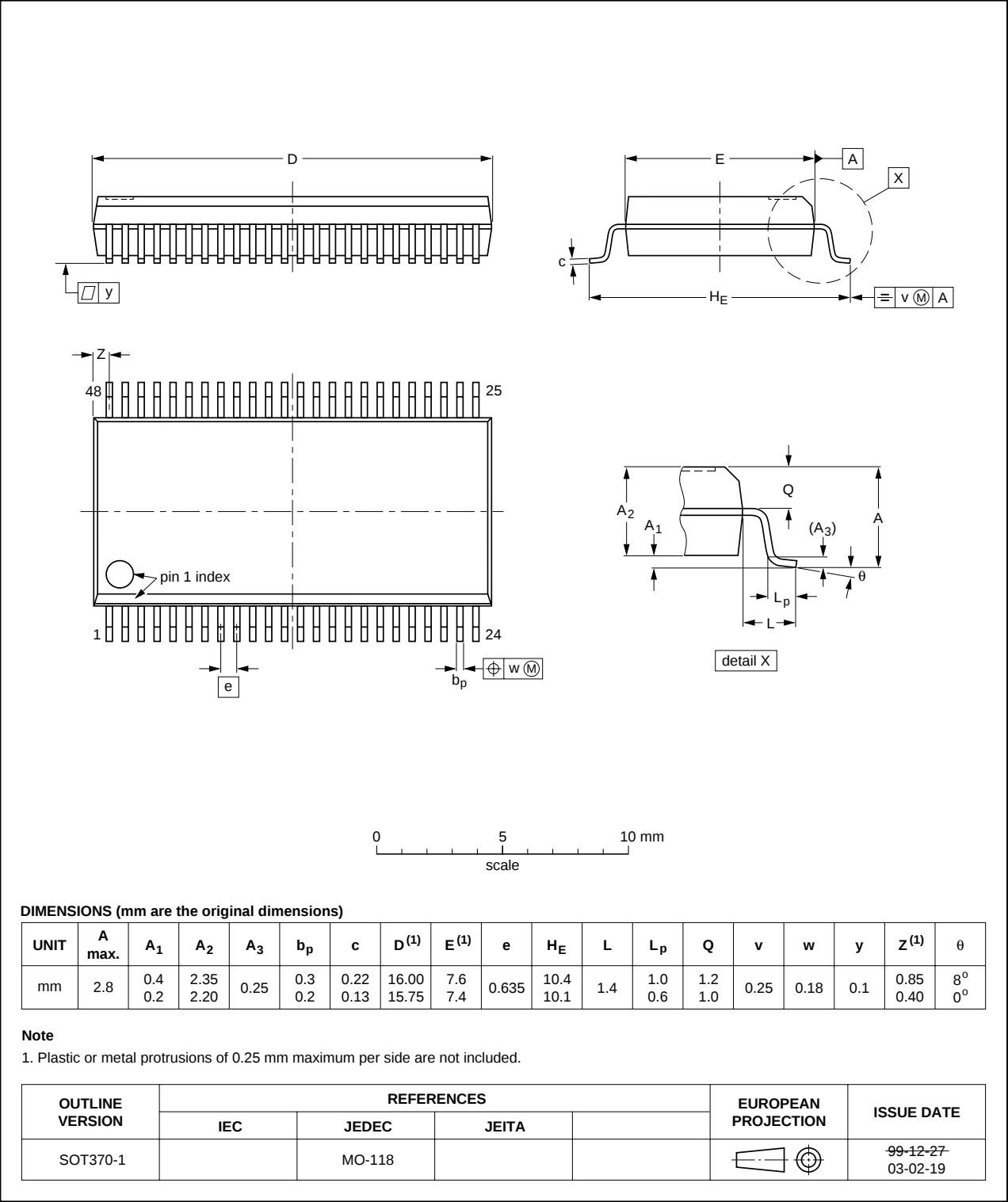


Fig 8. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

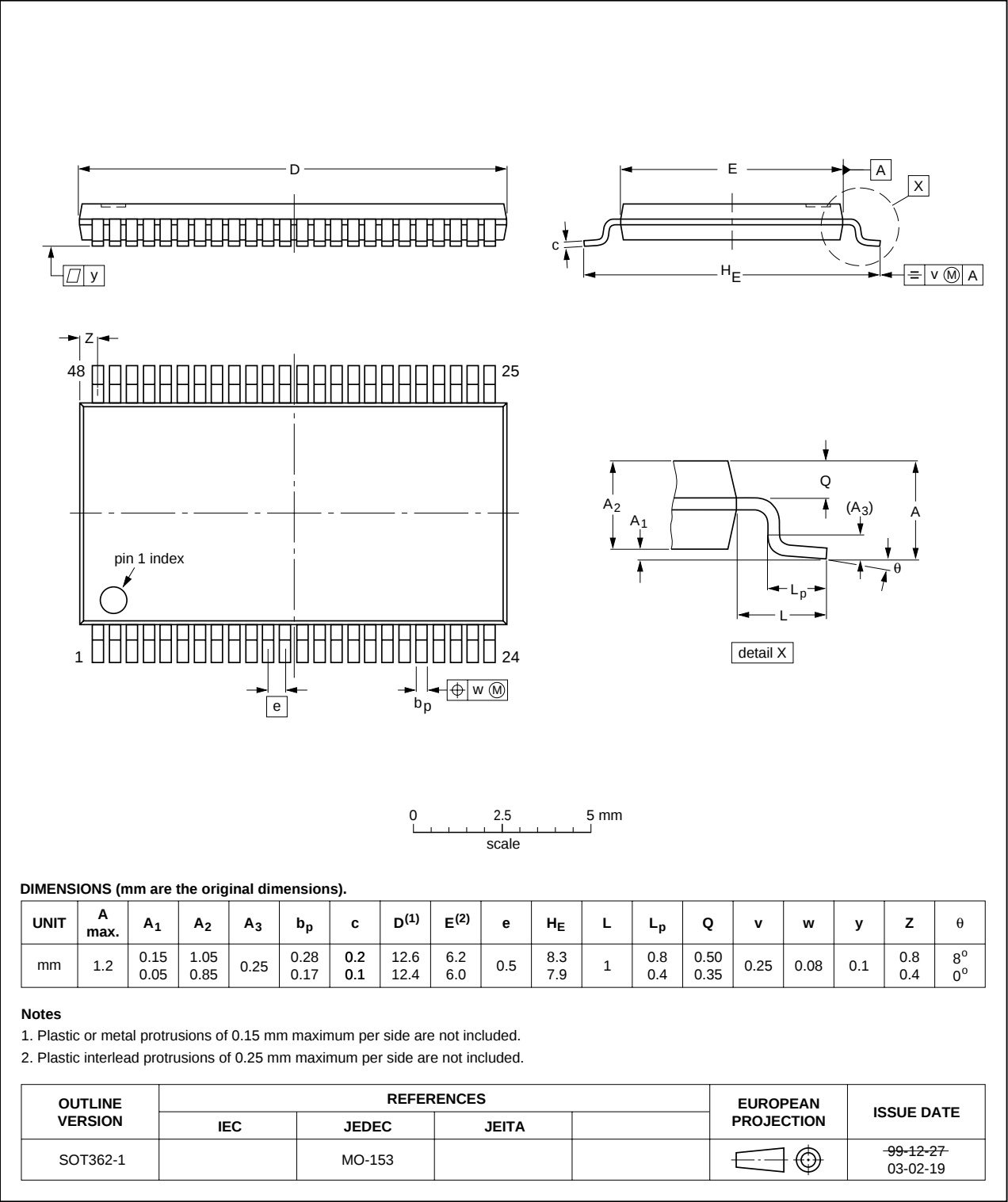


Fig 9. Package outline SOT362-1 (TSSOP48)

HUQFN60U: plastic thermal enhanced ultra thin quad flat package; no leads
 60 terminals; UTLP based; body 4 x 6 x 0.55 mm

SOT1025-1

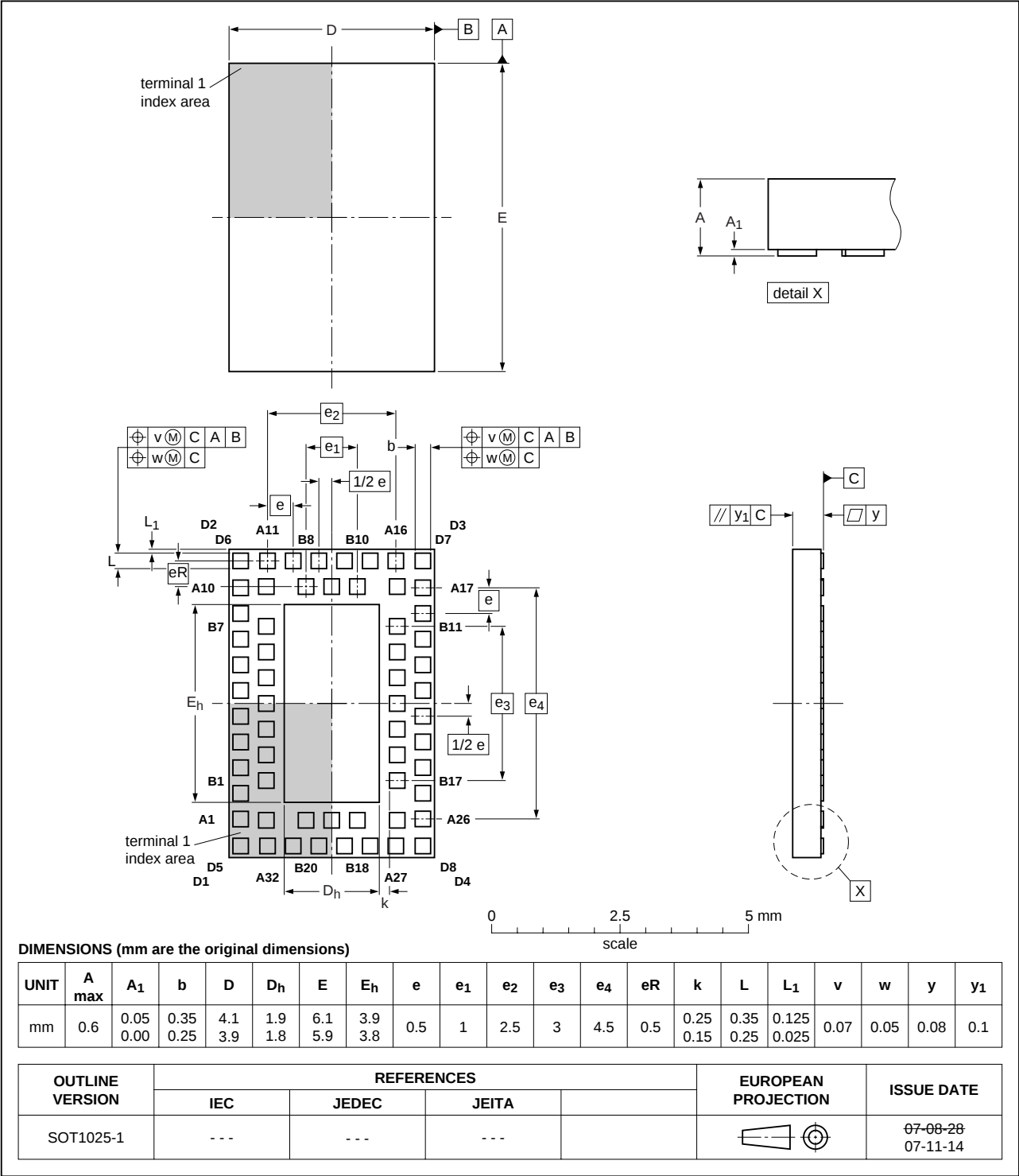


Fig 10. Package outline SOT1025-1 (HUQFN60U)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC164245_4	20081111	Product data sheet	-	74ALVC164245_3
Modifications:	• Added type number 74ALVC164245 (HUQFN60U package)			
74ALVC164245_3	20040914	Product data sheet	-	74ALVC164245_2
74ALVC164245_2	20040601	Product data sheet	-	74ALVC164245_1
74ALVC164245_1	19980826	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1 General description 1

2 Features 1

3 Ordering information 2

4 Functional diagram 2

5 Pinning information 4

5.1 Pinning 4

5.2 Pin description 6

6 Functional description 6

7 Limiting values 6

8 Recommended operating conditions 7

9 Static characteristics 8

10 Dynamic characteristics 9

11 AC waveforms 11

12 Package outline 14

13 Abbreviations 17

14 Revision history 17

15 Legal information 18

15.1 Data sheet status 18

15.2 Definitions 18

15.3 Disclaimers 18

15.4 Trademarks 18

16 Contact information 18

17 Contents 19



Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.