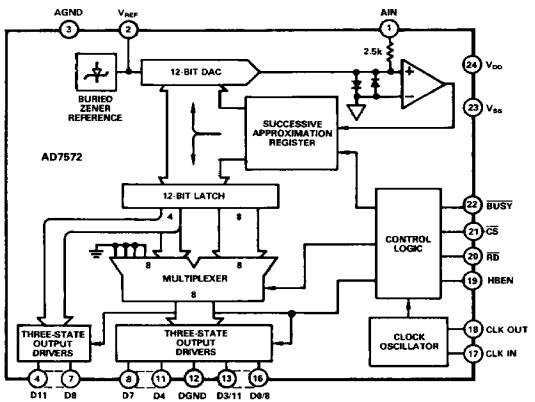
# LC²MOS
# Complete, High Speed 12-Bit ADC
# AD7572



**FEATURES**

**12-Bit Resolution and Accuracy**
**Fast Conversion Time**
**AD7572XX05: 5μs**
**AD7572XX12: 12.5μs**
**Complete with On-Chip Reference**
**Fast Bus Access Time: 90ns**
**Low Power: 135mW**
**Small, 0.3", 24-Pin Package and 28-Terminal Surface Mount Packages**

**FUNCTIONAL BLOCK DIAGRAM**




**GENERAL DESCRIPTION**

The AD7572 is a complete, 12-bit ADC that offers high speed performance combined with low, CMOS power levels. The AD7572 uses an accurate, high speed DAC and comparator in a successive-approximation loop to achieve a fast conversion time. An on-chip, buried Zener diode provides a stable reference voltage to give low drift performance over the full temperature range and the specified accuracy is achieved without any user trims. An on-chip clock circuit is provided, which may be used with a crystal for stand-alone operation, or the clock input may be driven from an external clock source such as a divided-down microprocessor clock. The only other external components required for basic operation of the AD7572 are decoupling capacitors for the supply voltages and reference output.

The AD7572 has a high speed digital interface with three-state data outputs and can operate under the control of standard microprocessor Read ($\overline{RD}$) and decoded address ($\overline{CS}$) signals. Interface timing is sufficiently fast to allow the AD7572 to operate with most popular microprocessors, with three-state enable times of only 90ns and bus relinquish times of 75ns.

The AD7572 is fabricated in Analog Devices Linear Compatible CMOS process (LC²MOS), an advanced, all ion-implanted process that combines fast CMOS logic and linear, bipolar circuits on a single chip, thus achieving excellent linear performance while still retaining low CMOS power levels.

The AD7572 is available in both 0.3" wide , 24-pin DIPs and in a 28-terminal plastic leaded chip carrier (PLCC) and leadless ceramic chip carrier (LCCC).

**PRODUCT HIGHLIGHTS**

1. Fast, 5μs and 12.5μs conversion times make the AD7572 ideal for a wide range of applications in telecommunications, sonar and radar signal processing or any wideband data acquisition system.
2. On-chip buried-Zener reference has temperature coefficient as low as 25ppm/°C, giving low full-scale drift over the operating temperature range.
3. Stable DAC and comparator give excellent linearity and low zero error over the full temperature range.
4. Fast, easy-to-use digital interface has three-state bus access times of 90ns and bus relinquish times of 75ns, allowing the AD7572 to interface to most popular microprocessors.
5. LC²MOS circuitry gives low power drain (135mW) from +5, −15 volt supplies.
6. 24-pin 0.3" package offers space saving over parts in 28-pin 0.6" DIP.

# AD7572—SPECIFICATIONS

($V_{DD}$ = 5V ± 5%, $V_{SS}$ = −15V ± 5%, $f_{CLK}$: 2.5MHz for AD7572XX05, 1MHz for AD7572XX12. All Specifications $T_{min}$ to $T_{max}$ unless otherwise noted. Specifications apply to Slow Memory Mode.)

| Parameter | J, A, S Versions[1] | K, B, T Versions | L Version | C, U Versions | Units | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| ACCURACY | | | | | | |
| Resolution | 12 | 12 | 12 | 12 | Bits | |
| Integral Nonlinearity @ +25°C | ±1 | ±1 | ±1/2 | ±1/2 | LSB max | |
| $T_{min}$ to $T_{max}$ | ±1 | ±1 | ±1/2 | ±3/4 | LSB max | |
| Differential Nonlinearity | ±1 | ±1 | ±1 | ±1 | LSB max | |
| Minimum Resolution for which no Missing Codes are Guaranteed | 12 | 12 | 12 | 12 | Bits | |
| Offset Error @ +25°C | ±4 | ±3 | ±3 | ±3 | LSB max | |
| $T_{min}$ to $T_{max}$ | ±6 | ±5 | ±4 | ±4 | LSB max | Typical Change over Temp Is ± 1LSB |
| Full Scale (FS) Error[2] @ +25°C | ±15 | ±10 | ±10 | ±10 | LSB max | $V_{DD}$ = 5V; $V_{SS}$ = −15V; FS = 5V |
| Full Scale TC[3,4] | 45 | 25 | 25 | 25 | ppm/°C max | Ideal Last Code Transition = FS − 3/2LSBs |
| ANALOG INPUT | | | | | | |
| Input Voltage Range | 0 to +5 | 0 to +5 | 0 to +5 | 0 to +5 | Volts | For Bipolar Operation See |
| Input Current | 3.5 | 3.5 | 3.5 | 3.5 | mA max | Figures 10 & 12 |
| INTERNAL REFERENCE VOLTAGE | | | | | | |
| $V_{REF}$ Output @ +25°C | −5.2/−5.3 | −5.2/−5.3 | −5.2/−5.3 | −5.2/−5.3 | V min/V max | −5.25V ± 1% |
| $V_{REF}$ Output TC | 40 | 20 | 20 | 20 | ppm/°C typ | |
| Output Current Sink Capability | 550 | 550 | 550 | 550 | μA max | External Load Should Not Change During Conversion |
| POWER SUPPLY REJECTION | | | | | | |
| $V_{DD}$ Only | ±1/2 | ±1/2 | ±1/2 | ±1/2 | LSB typ | FS Change, $V_{SS}$ = −15V $V_{DD}$ = +4.75V to +5.25V |
| $V_{SS}$ Only | ±1/2 | ±1/2 | ±1/2 | ±1/2 | LSB typ | FS Change, $V_{DD}$ = 5V $V_{SS}$ = −14.25V to −15.75V |
| LOGIC INPUTS | | | | | | |
| $\overline{CS}$, $\overline{RD}$, HBEN, CLK IN | | | | | | $V_{DD}$ = 5V ± 5% |
| $V_{INL}$, Input Low Voltage | +0.8 | +0.8 | +0.8 | +0.8 | V max | |
| $V_{INH}$, Input High Voltage | +2.4 | +2.4 | +2.4 | +2.4 | V min | |
| $C_{IN}$,[5] Input Capacitance | 10 | 10 | 10 | 10 | pF max | |
| $\overline{CS}$, $\overline{RD}$, HBEN | | | | | | |
| $I_{IN}$, Input Current | ±10 | ±10 | ±10 | ±10 | μA max | $V_{IN}$ = 0 to $V_{DD}$ |
| CLK IN | | | | | | |
| $I_{IN}$, Input Current | ±20 | ±20 | ±20 | ±20 | μA max | $V_{IN}$ = 0 to $V_{DD}$ |
| LOGIC OUTPUTS | | | | | | |
| D11–D0/8, $\overline{BUSY}$, CLK OUT | | | | | | |
| $V_{OL}$, Output Low Voltage | +0.4 | +0.4 | +0.4 | +0.4 | V max | $I_{SINK}$ = 1.6mA |
| $V_{OH}$, Output High Voltage | +4.0 | +4.0 | +4.0 | +4.0 | V min | $I_{SOURCE}$ = 200μA |
| D11–D0/8 | | | | | | |
| Floating State Leakage Current | ±10 | ±10 | ±10 | ±10 | μA max | |
| Floating State Output Capacitance[5] | 15 | 15 | 15 | 15 | pF max | |
| CONVERSION TIME | | | | | | |
| AD7572XX05 | | | | | | |
| Synchronous Clock | 5 | 5 | 5 | 5 | μs max | $f_{CLK}$ = 2.5MHz. See Under |
| Asynchronous Clock | 4.8/5.2 | 4.8/5.2 | 4.8/5.2 | 4.8/5.2 | μs min/max | Control Inputs Synchronization |
| AD7572XX12 | | | | | | |
| Synchronous Clock | 12.5 | 12.5 | 12.5 | 12.5 | μs max | $f_{CLK}$ = 1MHz |
| Asynchronous Clock | 12/13 | 12/13 | 12/13 | 12/13 | μs min/μs max | |
| POWER REQUIREMENTS | | | | | | |
| $V_{DD}$ | +5 | +5 | +5 | +5 | V NOM | ±5% for Specified Performance |
| $V_{SS}$ | −15 | −15 | −15 | −15 | V NOM | ±5% for Specified Performance |
| $I_{DD}$[6] | 7 | 7 | 7 | 7 | mA max | $\overline{CS}$ = $\overline{RD}$ = $V_{DD}$, AIN = 5V |
| $I_{SS}$[6] | 12 | 12 | 12 | 12 | mA max | $\overline{CS}$ = $\overline{RD}$ = $V_{DD}$, AIN = 5V |
| Power Dissipation | 135 | 135 | 135 | 135 | mW typ | |
| | 215 | 215 | 215 | 215 | mW max | |

NOTES

[1]Temperature range as follows: J, K, L Versions; 0 to +70°C.
A, B, C Versions; −25°C to +85°C.
S, T, U Versions; −55°C to +125°C.

[2]Includes internal voltage reference error.

[3]Full-Scale TC = ΔFS/ΔT, where ΔFS is Full-Scale change from $T_A$ = +25°C to $T_{min}$ or $T_{max}$.

[4]Includes internal voltage reference drift.

[5]Sample tested to ensure compliance.

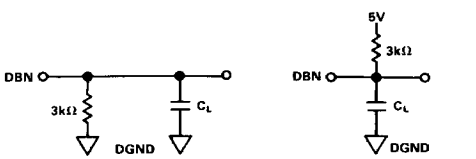
[6]Power supply current is measured when AD7572 is inactive, i.e., $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH.

Specifications subject to change without notice.

## TIMING CHARACTERISTICS[1] ($V_{DD}$ = 5V, $V_{SS}$ −15V)

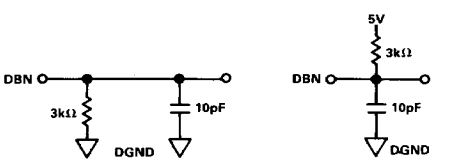
| Parameter | Limit at +25°C (All Grades) | Limit at $T_{min}$, $T_{max}$ (J, K, L, A, B, C Grades) | Limit at $T_{min}$, $T_{max}$ (S, T, U Grades) | Units | Conditions/Comments |
|---|---|---|---|---|---|
| $t_1$ | 0 | 0 | 0 | ns min | $\overline{CS}$ to $\overline{RD}$ Setup Time |
| $t_2$ | 190 | 230 | 270 | ns max | $\overline{RD}$ to $\overline{BUSY}$ Propagation Delay |
| $t_3$[2] | 90 | 110 | 120 | ns max | Data Access Time after $\overline{RD}$, $C_L$ = 20pF |
| | 125 | 150 | 170 | ns max | Data Access Time after $\overline{RD}$, $C_L$ = 100pF |
| $t_4$ | $t_3$ | $t_3$ | $t_3$ | ns min | $\overline{RD}$ Pulse Width |
| $t_5$ | 0 | 0 | 0 | ns min | $\overline{CS}$ to $\overline{RD}$ Hold Time |
| $t_6$[2] | 70 | 90 | 100 | ns max | Data Setup Time after $\overline{BUSY}$ |
| $t_7$[3] | 20 | 20 | 20 | ns min | Bus Relinquish Time |
| | 75 | 85 | 90 | ns max | |
| $t_8$ | 0 | 0 | 0 | ns min | HBEN to $\overline{RD}$ Setup Time |
| $t_9$ | 0 | 0 | 0 | ns min | HBEN to $\overline{RD}$ Hold Time |
| $t_{10}$ | 200 | 200 | 200 | ns min | Delay Between Successive Read Operations |

NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]$t_3$ and $t_6$ are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[3]$t_7$ is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.




*a. High-Z to $V_{OH}$ ($t_3$) and $V_{OL}$ to $V_{OH}$ ($t_6$)* *b. High-Z to $V_{OL}$ ($t_3$) and $V_{OH}$ to $V_{OL}$ ($t_6$)*

*Figure 1. Load Circuits for Access Time*




*a. $V_{OH}$ to High-Z* *b. $V_{OL}$ to High-Z*

*Figure 2. Load Circuits for Output Float Delay*

### ABSOLUTE MAXIMUM RATINGS*
($T_A$ = +25°C unless otherwise noted)

| | |
|---|---|
| $V_{DD}$ to DGND | −0.3V to +7V |
| $V_{SS}$ to DGND | +0.3V to −17V |
| AGND to DGND | −0.3V, $V_{DD}$ + 0.3V |
| AIN to AGND | −15V to +15V |
| Digital Input Voltage to DGND (CLK IN, HBEN, $\overline{RD}$, $\overline{CS}$) | −0.3V, $V_{DD}$ +0.3V |
| Digital Output Voltage to DGND (D11–D0/8, CLK OUT, $\overline{BUSY}$) | −0.3V, $V_{DD}$ +0.3V |
| Operating Temperature Range | |
| Commercial (J, K, L Versions) | 0 to +70°C |
| Industrial (A, B, C Versions) | −25°C to +85°C |
| Extended (S, T, U Versions) | −55°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10secs) | +300°C |
| Power Dissipation (Any Package) to +75°C | 1,000mW |
| Derates above +75°C by | 10mW/°C |

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**CAUTION**
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

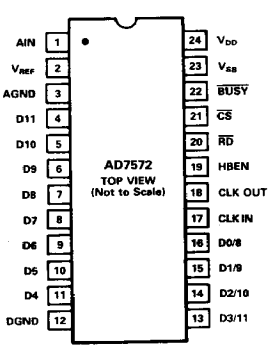
## ORDERING GUIDE[1]

| Model[2] | Conversion Time | Temperature Range | Full-Scale TC | Accuracy Grade | Package Option[3] |
|---|---|---|---|---|---|
| AD7572JN05 | 5µs | 0 to +70°C | 45ppm/°C | ±1LSB | N-24 |
| AD7572KN05 | 5µs | 0 to +70°C | 25ppm/°C | ±1LSB | N-24 |
| AD7572LN05 | 5µs | 0 to +70°C | 25ppm/°C | ±1/2LSB | N-24 |
| AD7572JP05 | 5µs | 0 to +70°C | 45ppm/°C | ±1LSB | P-28A |
| AD7572KP05 | 5µs | 0 to +70°C | 25ppm/°C | ±1LSB | P-28A |
| AD7572LP05 | 5µs | 0 to +70°C | 25ppm/°C | ±1/2LSB | P-28A |
| AD7572AQ05 | 5µs | −25°C to +85°C | 45ppm/°C | ±1LSB | Q-24 |
| AD7572BQ05 | 5µs | −25°C to +85°C | 25ppm/°C | ±1LSB | Q-24 |
| AD7572CQ05 | 5µs | −25°C to +85°C | 25ppm/°C | ±1/2LSB | Q-24 |
| AD7572SQ05 | 5µs | −55°C to +125°C | 45ppm/°C | ±1LSB | Q-24 |
| AD7572TQ05 | 5µs | −55°C to +125°C | 25ppm/°C | ±1LSB | Q-24 |
| AD7572UQ05 | 5µs | −55°C to +125°C | 25ppm/°C | ±1/2LSB | Q-24 |
| AD7572SE05 | 5µs | −55°C to +125°C | 45ppm/°C | ±1LSB | E-28A |
| AD7572TE05 | 5µs | −55°C to +125°C | 25ppm/°C | ±1LSB | E-28A |
| AD7572UE05 | 5µs | −55°C to +125°C | 25ppm/°C | ±1/2LSB | E-28A |
| AD7572JN12 | 12.5µs | 0 to +70°C | 45ppm/°C | ±1LSB | N-24 |
| AD7572KN12 | 12.5µs | 0 to +70°C | 25ppm/°C | ±1LSB | N-24 |
| AD7572LN12 | 12.5µs | 0 to +70°C | 25ppm/°C | ±1/2LSB | N-24 |
| AD7572JP12 | 12.5µs | 0 to +70°C | 45ppm/°C | ±1LSB | P-28A |
| AD7572KP12 | 12.5µs | 0 to +70°C | 25ppm/°C | ±1LSB | P-28A |
| AD7572LP12 | 12.5µs | 0 to +70°C | 25ppm/°C | ±1/2LSB | P-28A |
| AD7572AQ12 | 12.5µs | −25°C to +85°C | 45ppm/°C | ±1LSB | Q-24 |
| AD7572BQ12 | 12.5µs | −25°C to +85°C | 25ppm/°C | ±1LSB | Q-24 |
| AD7572CQ12 | 12.5µs | −25°C to +85°C | 25ppm/°C | ±1/2LSB | Q-24 |
| AD7572SQ12 | 12.5µs | −55°C to +125°C | 45ppm/°C | ±1LSB | Q-24 |
| AD7572TQ12 | 12.5µs | −55°C to +125°C | 25ppm/°C | ±1LSB | Q-24 |
| AD7572UQ12 | 12.5µs | −55°C to +125°C | 25ppm/°C | ±1/2LSB | Q-24 |
| AD7572SE12 | 12.5µs | −55°C to +125°C | 45ppm/°C | ±1LSB | E-28A |
| AD7572TE12 | 12.5µs | −55°C to +125°C | 25ppm/°C | ±1LSB | E-28A |
| AD7572UE12 | 12.5µs | −55°C to +125°C | 25ppm/°C | ±1/2LSB | E-28A |

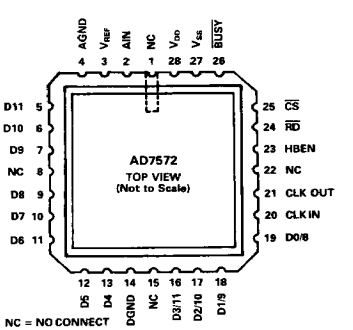
NOTES
[1]Analog Devices Reserves the right to ship ceramic (D-24A) in lieu cerdip (Q-24) hermetic package.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC Drawing #5962-87591.
[3]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information ssection.

## PIN CONFIGURATIONS

**DIP**




**LCCC**




**PLCC**