

# FDS9953A

# Dual 30V P-Channel PowerTrench<sup>O</sup> MOSFET

### **General Description**

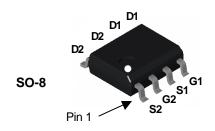
This PChannel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gave drive voltage ratings (4.5V-25V).

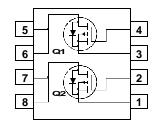
### **Applications**

- Power management
- Load switch
- Battery protection

#### **Features**

- -2.9 A, -30 V  $R_{DS(ON)} = 130 \text{ m}\Omega$  @  $V_{GS} = -10 \text{ V}$   $R_{DS(ON)} = 200 \text{ m}\Omega$  @  $V_{GS} = -4.5 \text{ V}$
- Low gate charge (2.5nC typical)
- Fast switching speed
- High performance trench technology for extremely low R<sub>DS(ON)</sub>
- High power and current handling capability





## Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units	
V <sub>DSS</sub>	Drain-Source Voltage		-30	V
V <sub>GSS</sub>	Gate-Source Voltage		±25	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	±2.9	А
	- Pulsed		±10	
P <sub>D</sub>	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperat	-55 to +150	°C	

### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
R <sub>0</sub> JC	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

## **Package Marking and Ordering Information**

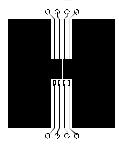
Device Marking	evice Marking Device		Tape width	Quantity
FDS9953A	FDS9953A FDS9953A		12mm	2500 units

Symbol	Parameter	Test Conditions	Тур	Max	Units	
Off Char	acteristics		- II		I.	I.
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-30			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 μA, Referenced to 25°C		-23		mV/°C
l <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{ V},  V_{GS} = 0 \text{ V}$			-2	μΑ
Igssf	Gate-Body Leakage, Forward	$V_{GS} = -25 \text{ V},  V_{DS} = 0 \text{ V}$			-100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	$V_{GS} = 25 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
On Chara	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-1	-1.8	-3.0	V
ΔV <sub>GS(th)</sub> ΔT <sub>J</sub>	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , Referenced to 25°C		4		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$\begin{split} V_{GS} &= -10 \text{ V},  I_D = -1 \text{ A} \\ V_{GS} &= -10 \text{ V},  I_D = -1 \text{ A},  T_J = 125^{\circ}\text{C} \\ V_{GS} &= -4.5 \text{ V},  I_D = -0.5 \text{ A} \\ V_{GS} &= -4.5 \text{ V},  I_D = -0.5 \text{ A},  T_J = 125^{\circ}\text{C} \end{split}$		95 137 142 202	130 200 200 310	mΩ
L	On–State Drain Current	$V_{GS} = -10 \text{ V}, \qquad V_{DS} = -5 \text{ V}$	<b>-</b> 5			Α
I <sub>D(on)</sub>	On-State Drain Guirent	$\begin{split} &V_{GS} = -4.5 \text{ V}, \text{ I}_D = -0.5 \text{ A}, \text{ T}_J = 125 ^{\circ}\text{C} \\ &V_{GS} = -10 \text{ V}, \qquad V_{DS} = -5 \text{ V} \\ &V_{GS} = -4.5 \text{ V}, \qquad V_{DS} = -5 \text{ V} \end{split}$	-1.5			
<b>g</b> FS	Forward Transconductance	$V_{DS} = -15 \text{ V}, \qquad I_{D} = -1 \text{ A}$		4		S
Dynamic	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -15 \text{ V},  V_{GS} = 0 \text{ V},$		185		pF
Coss	Output Capacitance	f = 1.0 MHz		56		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 = 1.0 ((1))		26		pF
Switchin	g Characteristics (Note 2)					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = -15 \text{ V}, \qquad I_D = -1 \text{ A},$		4.5	9	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = -10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		13	23	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			11	20	ns
t <sub>f</sub>	Turn-Off Fall Time			2	4	ns
Qg	Total Gate Charge	$V_{DS} = -5 V$ , $I_{D} = -1 A$ ,		2.5	3.5	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = -10 V		0.8		nC
Q <sub>gd</sub>	Gate-Drain Charge			0.9		nC
Drain-Sc	ource Diode Characteristics	and Maximum Ratings				
l <sub>s</sub>	Maximum Continuous Drain-Source				-1.2	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_{S} = -1.3 \text{ A}  \text{(Note 2)}$		-0.8	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_F = -1.25\text{A},$		17	100	nS

# **Typical Characteristics**

#### Notes:

 R<sub>BLR</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>BLC</sub> is guaranteed by design while R<sub>BCA</sub> is determined by the user's board design.



78°C/W when mounted on a 0.5in² pad of 2 oz copper



125°C/W when mounted on a 0.02 in<sup>2</sup> pad of 2 oz copper



135°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

# **Typical Characteristics**

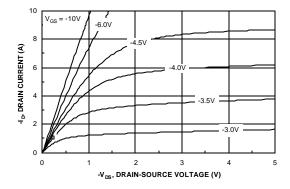


Figure 1. On-Region Characteristics.

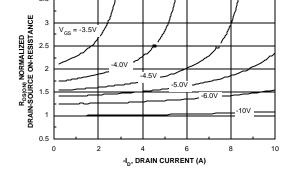


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

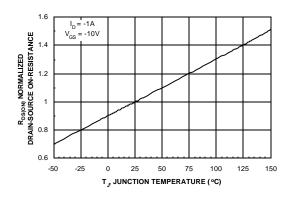


Figure 3. On-Resistance Variation with Temperature.

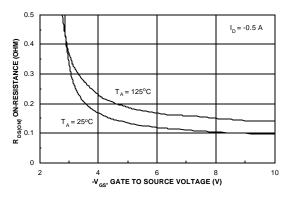


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

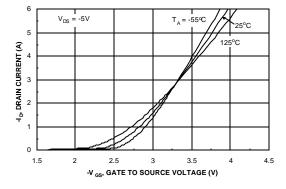


Figure 5. Transfer Characteristics.

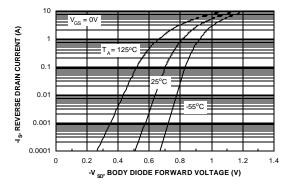
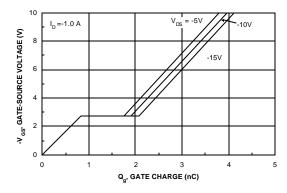


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

# **Typical Characteristics**



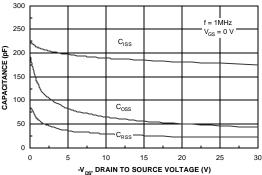


Figure 7. Gate Charge Characteristics.

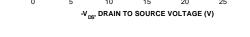
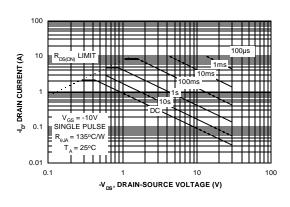


Figure 8. Capacitance Characteristics.



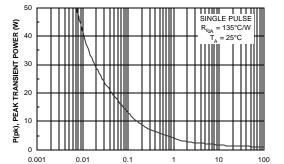


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

t<sub>1</sub>, TIME (sec)

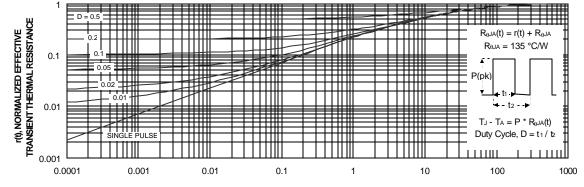


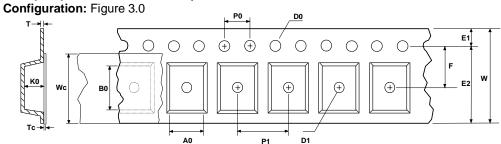
Figure 11. Transient Thermal Response Curve.

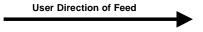
Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

#### **SOIC-8 Tape and Reel Data** FAIRCHILD SEMICONDUCTOR TM SOIC(8lds) Packaging Configuration: Figure 1.0 ATTENTION Packaging Description: Packaging Description: SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13° or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7° or 177cm diameter reel. This and some other options are further described in the Packaging Information table. Embossed ESD Marking Antistatic Cover Tape These full reside are individually barcode labeled and placed inside a standard intermediate box fillustrated in figure 10) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts. Static Dissipative **Embossed Carrier Tape** F63TNR Customized Label SOIC (8lds) Packaging Information L86Z **Packaging Option** F011 D84Z no flow code **SOIC-8 Unit Orientation** Packaging type TNR Qty per Reel/Tube/Bag 2,500 4,000 500 Reel Size 13" Dia 13" Dia 7" Dia Barcode Label Box Dimension (mm) 355x333x40 530x130x83 355x333x40 193x183x80 Max qty per Box 5.000 30.000 8.000 2.000 Weight per unit (gm) 0.0774 0.0774 0.0774 0.0774 Weight per Reel (kg) Barcode Label Barcode Label 355mm x 333mm x 40mm Intermediate container for 13" reel option F63TNR Label sample 193mm x 183mm x 80mm Pizza Box for Standard Option SOIC(8lds) Tape Leader and Trailer D/C1: Z9842AB QTY1: D/C2: QTY2: Configuration: Figure 2.0 (F63TNR)3 0 $\bigcirc$ $\bigcirc$ 0 $\bigcirc$ $\circ$ $\bigcirc$ 0 0 0 0 0 0 Carrier Tape Components Cover Tape Leader Tape 1680mm minimum or 210 empty pockets Trailer Tape 640mm minimum or 80 empty pockets



## SOIC(8lds) Embossed Carrier Tape



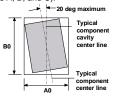


	Dimensions are in millimeter													
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SOIC(8lds) (12mm)	5.30 +/-0.10	6.50 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation



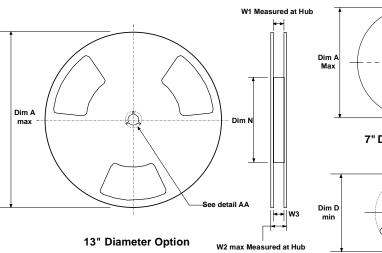
Sketch B (Top View)
Component Rotation

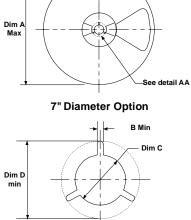


Sketch C (Top View)

Component lateral movement

### SOIC(8lds) Reel Configuration: Figure 4.0



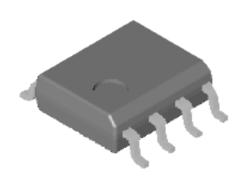


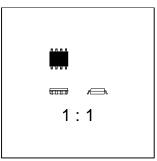
								DETAIL AA	١	
	Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)	
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4	
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4	

# **SOIC-8 Package Dimensions**



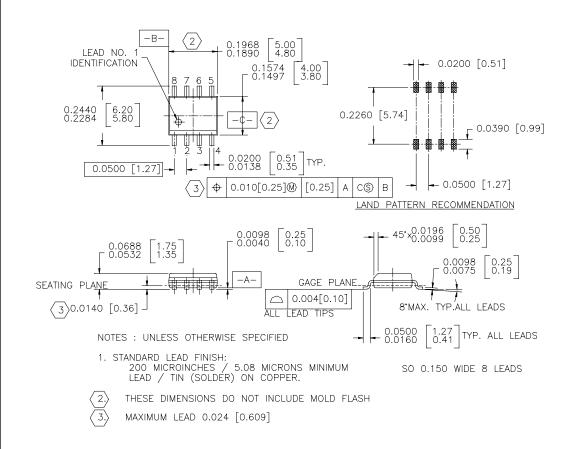
# SOIC-8 (FS PKG Code S1)





Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774



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EnSigna™ MicroFET™ SILENT SWITCHER® FACT™ MICROWIRE™ SMART START™

FACT Quiet Series™ OPTOLOGIC™ Stealth™

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#### PRODUCT STATUS DEFINITIONS

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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