

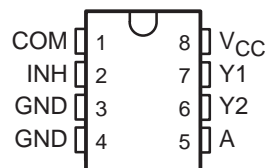
SN74AUC2G53

SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR 2:1 ANALOG MULTIPLEXER/DEMULPLEXER

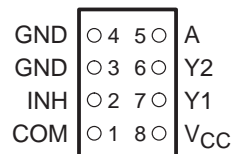
SCES484A – AUGUST 2003 – REVISED NOVEMBER 2003

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Operates at 0.8 V to 2.7 V
- Sub 1-V Operable
- Low Power Consumption, 10 μ A at 2.7 V
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

**DCT OR DCU PACKAGE
(TOP VIEW)**



**YEP OR YZP PACKAGE
(BOTTOM VIEW)**



description/ordering information

This analog switch is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.1-V to 2.7-V V_{CC} operation.

The SN74AUC2G53 can handle both analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Tape and reel	SN74AUC2G53YEPR	___U4_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74AUC2G53YZPR	
	SSOP – DCT	Tape and reel	SN74AUC2G53DCTR	U53___
	VSSOP – DCU	Tape and reel	SN74AUC2G53DCUR	U53_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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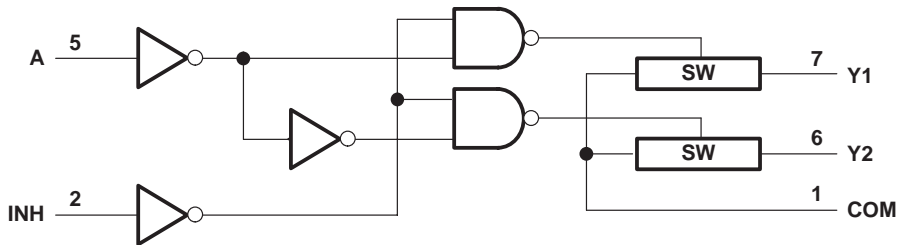
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FUNCTION TABLE

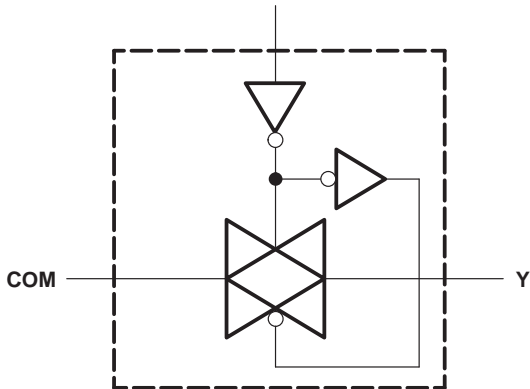
CONTROL INPUTS		ON CHANNEL
INH	A	
L	L	Y1
L	H	Y2
H	X	None

logic diagram (positive logic)



NOTE A: For simplicity, the test conditions shown in Figures 1 through 4 and 6 through 10 are for the demultiplexer configuration. Signals may be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

simplified schematic, each switch (SW)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 3.6 V
Input voltage range, V_I (see Notes 1 and 2)	–0.5 V to 3.6 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Control input clamp current, I_{IK} ($V_I < 0$)	–50 mA
I/O port diode current, I_{IOK} ($V_{I/O} < 0$ or $V_{I/O} > V_{CC}$)	±50 mA
On-state switch current, I_T ($V_{I/O} = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DCT package	220°C/W
DCU package	227°C/W
YEP/YZP package	102°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to ground unless otherwise specified.
 2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	2.7	V
V_{IH}	High-level input voltage	$V_{CC} = 0.8$ V	V_{CC}		V
		$V_{CC} = 1.1$ V to 1.95 V	$0.65 \times V_{CC}$		
		$V_{CC} = 2.3$ V to 2.7 V	1.7		
V_{IL}	Low-level input voltage	$V_{CC} = 0.8$ V		0	V
		$V_{CC} = 1.1$ V to 1.95 V		$0.35 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V		0.7	
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_I	Control input voltage		0	3.6	V
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8$ V to 1.6 V		20	ns/V
		$V_{CC} = 1.65$ V to 1.95 V		10	
		$V_{CC} = 2.3$ V to 2.7 V		3.5	
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP†	MAX	UNIT
r _{on}	On-state switch resistance	V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figures 1 and 2)	I _S = 4 mA	1.1 V			40	Ω
				1.65 V		12.5	20	
			I _S = 8 mA	2.3 V		6	15	
r _{on(p)}	Peak on resistance	V _I = V _{CC} to GND, V _{INH} = V _{IL} (see Figures 1 and 2)	I _S = 4 mA	1.1 V		131	180	Ω
				1.65 V		32	80	
			I _S = 8 mA	2.3 V		15	20	
Δr _{on}	Difference of on-state resistance between switches	V _I = V _{CC} to GND, V _C = V _{IH} (see Figures 1 and 2)	I _S = 4 mA	1.1 V			4	Ω
				1.65 V			1	
			I _S = 8 mA	2.3 V			1	
I _{S(off)}	Off-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH} (see Figure 3)	2.7 V				±1	μA
							±0.1†	
I _{S(on)}	On-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IL} , V _O = Open (see Figure 4)	2.7 V				±1	μA
							±0.1†	
I _I	Control input current	V _C = V _{CC} or GND	2.7 V				±5	μA
I _{CC}	Supply current	V _C = V _{CC} or GND	2.7 V				10	μA
C _{ic}	Control input capacitance		2.5 V			2		pF
C _{io(off)}	Switch input/output capacitance	Y	2.5 V			3		pF
		COM				4.5		
C _{io(on)}	Switch input/output capacitance		2.5 V			9		pF

 † T_A = 25°C

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd} ‡	COM or Y	Y or COM	0.3		0.3		0.3			0.2		0.1	ns
t _{en}	INH	COM or Y	9.2	0.5	3.5	0.5	2.2	0.5	1	1.9	0.5	1.8	ns
t _{dis}			8.1	0.5	4.2	0.5	3.2	0.5	1.9	3.4	0.5	2.6	
t _{en}	A	COM or Y	9.2	0.5	3.6	0.5	2.3	0.5	1.1	1.9	0.5	1.6	ns
t _{dis}			10	0.5	3.6	0.5	2.3	0.5	1.1	2	0.5	1.6	

‡ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

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switching characteristics over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$			$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}^\dagger	COM or Y	Y or COM	0.4			0.2		ns
t_{en}	INH	COM or Y	0.5	1.6	3.1	0.5	2.2	ns
t_{dis}			0.5	2.2	3.4	0.5	2.2	ns
t_{en}	A	COM or Y	0.5	1.6	3	0.5	2.2	ns
t_{dis}			0.5	1.6	3	0.5	2.3	ns

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

analog switch characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response ‡ (switch ON)	COM or Y	Y or COM	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = \text{sine wave}$ (see Figure 6)	0.8 V	90	MHz
				1.1 V	101	
				1.4 V	110	
				1.65 V	122	
				2.3 V	198	
			$C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f_{in} = \text{sine wave}$ (see Figure 6)	0.8 V	>500	
				1.1 V	>500	
				1.4 V	>500	
				1.65 V	>500	
				2.3 V	>500	
Crosstalk § (between switches)	COM or Y	Y or COM	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 7)	0.8 V	-59	dB
				1.1 V	-59	
				1.4 V	-59	
				1.65 V	-59	
				2.3 V	-60	
			$C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 7)	0.8 V	-55	
				1.1 V	-55	
				1.4 V	-55	
				1.65 V	-55	
				2.3 V	-55	
Crosstalk (control input to signal output)	INH	COM or Y	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (square wave) (see Figure 8)	0.8 V	0.56	mV
				1.1 V	0.68	
				1.4 V	0.81	
				1.65 V	0.93	
				2.3 V	1.5	

‡ Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads -3 dB.

§ Adjust f_{in} voltage to obtain 0 dBm at input.

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analog switch characteristics, $T_A = 25^\circ\text{C}$ (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Feed-through attenuation [§] (switch OFF)	COM or Y	Y or COM	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 9)	0.8 V	–60	dB
				1.1 V	–60	
				1.4 V	–60	
				1.65 V	–60	
				2.3 V	–60	
			$C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 9)	0.8 V	–59	
				1.1 V	–59	
				1.4 V	–59	
				1.65 V	–59	
				2.3 V	–59	
Sine-wave distortion	COM or Y	Y or COM	$C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $f_{in} = 1\text{ kHz}$ (sine wave) (see Figure 10)	0.8 V	6.19	%
				1.1 V	0.39	
				1.4 V	0.06	
				1.65 V	0.02	
				2.3 V	0.01	
			$C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $f_{in} = 10\text{ kHz}$ (sine wave) (see Figure 10)	0.8 V	3.55	
				1.1 V	0.38	
				1.4 V	0.04	
				1.65 V	0.02	
				2.3 V	0.02	

[§] Adjust f_{in} voltage to obtain 0 dBm at input.**operating characteristics for INH input, $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$	$V_{CC} = 1.5\text{ V}$	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	UNIT
		TYP	TYP	TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	$f = 10\text{ MHz}$	3	3	3	3	3	pF

operating characteristics for A input, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$	$V_{CC} = 1.5\text{ V}$	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	Outputs enabled	$f = 10\text{ MHz}$	5.5	5.5	5.5	5.5	5.5	pF
	Outputs disabled		0.5	0.5	0.5	0.5	0.5	

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PARAMETER MEASUREMENT INFORMATION

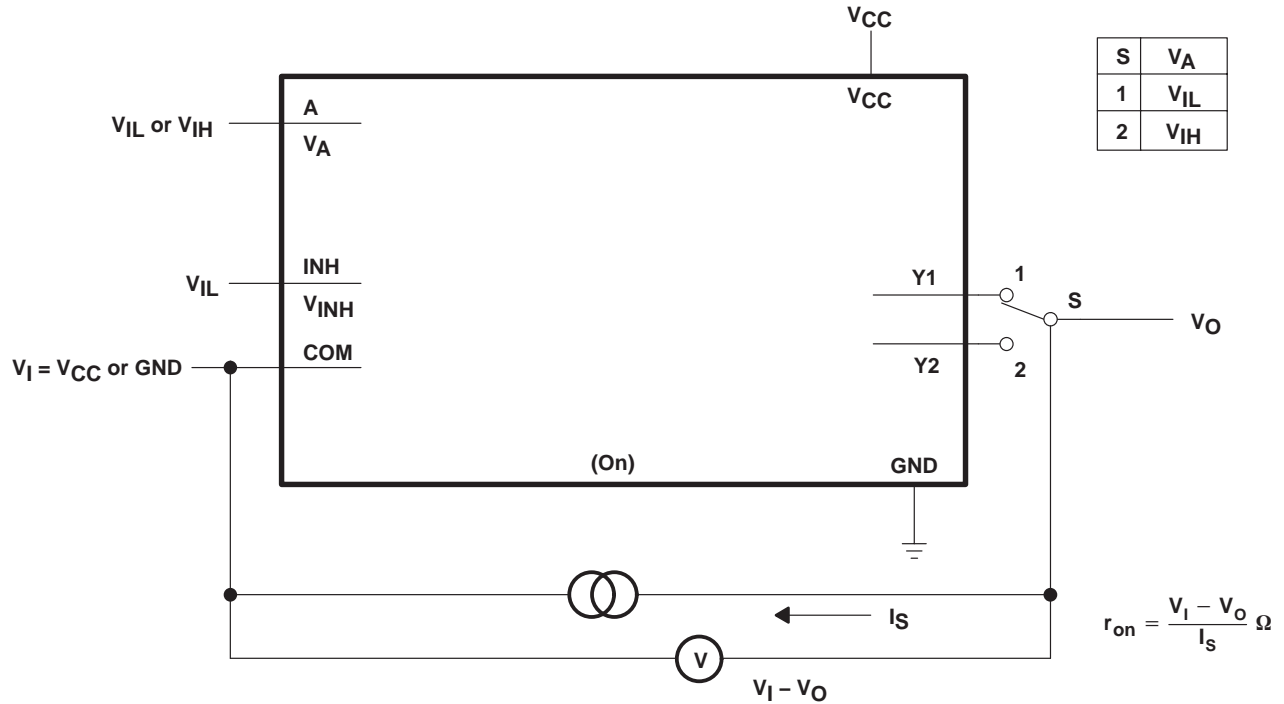


Figure 1. On-State Resistance Test Circuit

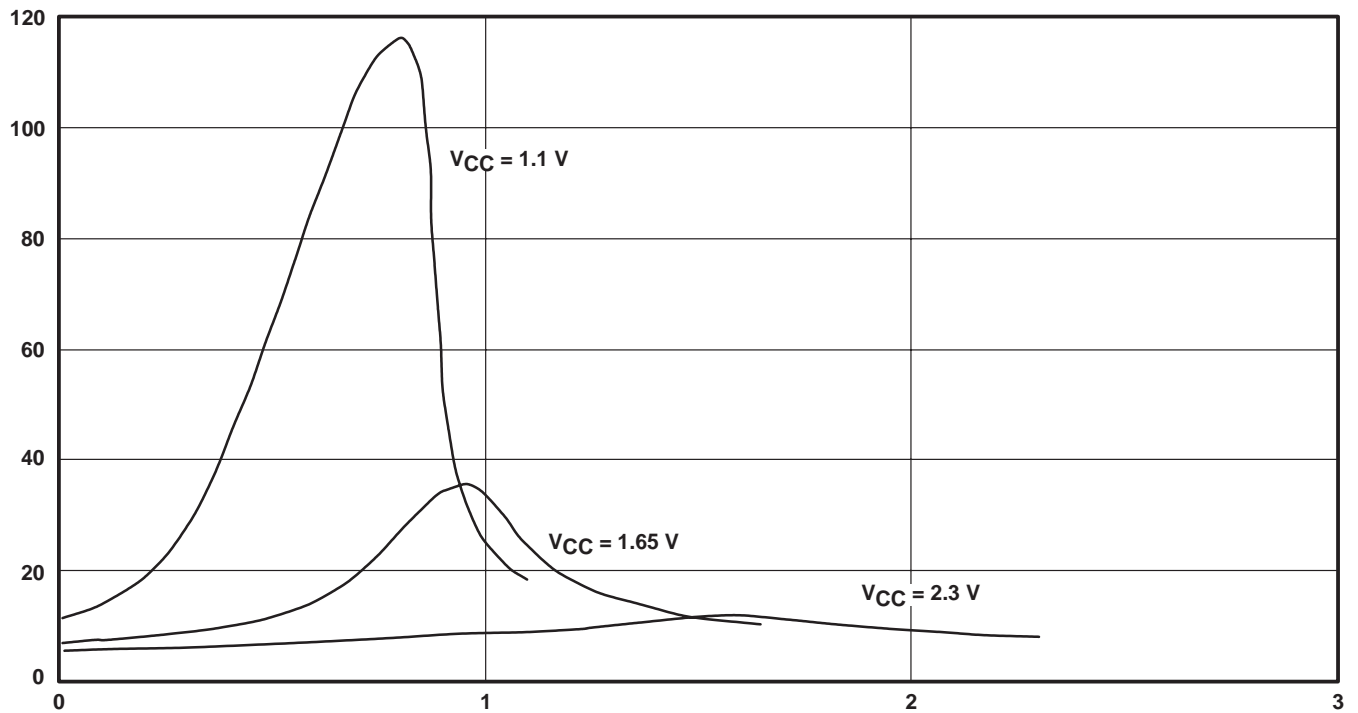


Figure 2. Typical r_{on} as a Function of Voltage (V_I) for $V_I = 0$ to V_{CC}

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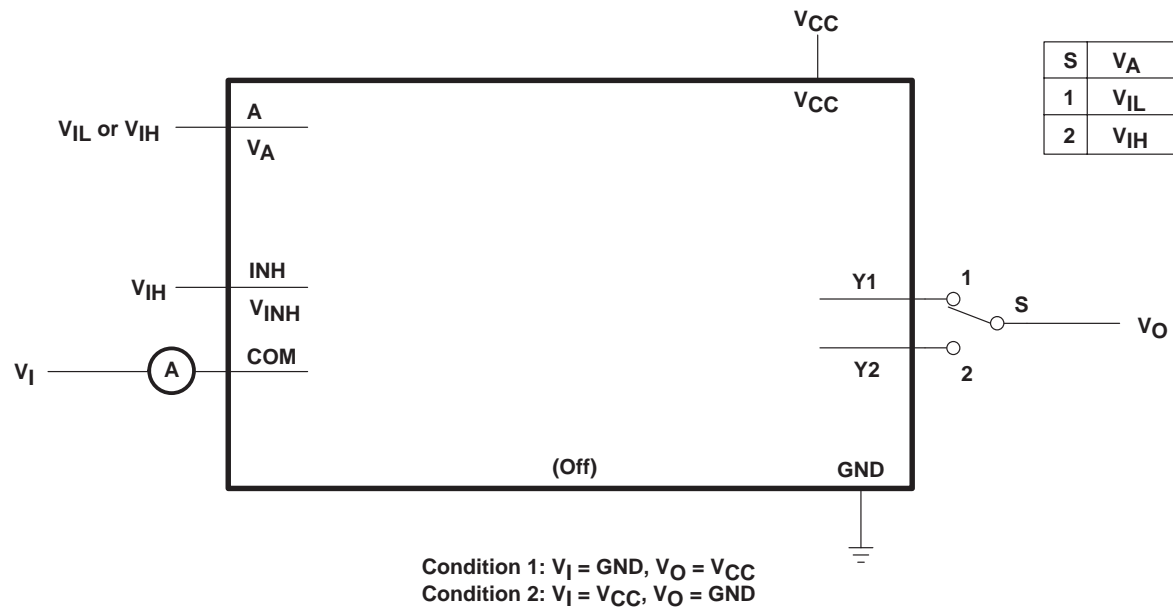


Figure 3. Off-State Switch Leakage-Current Test Circuit

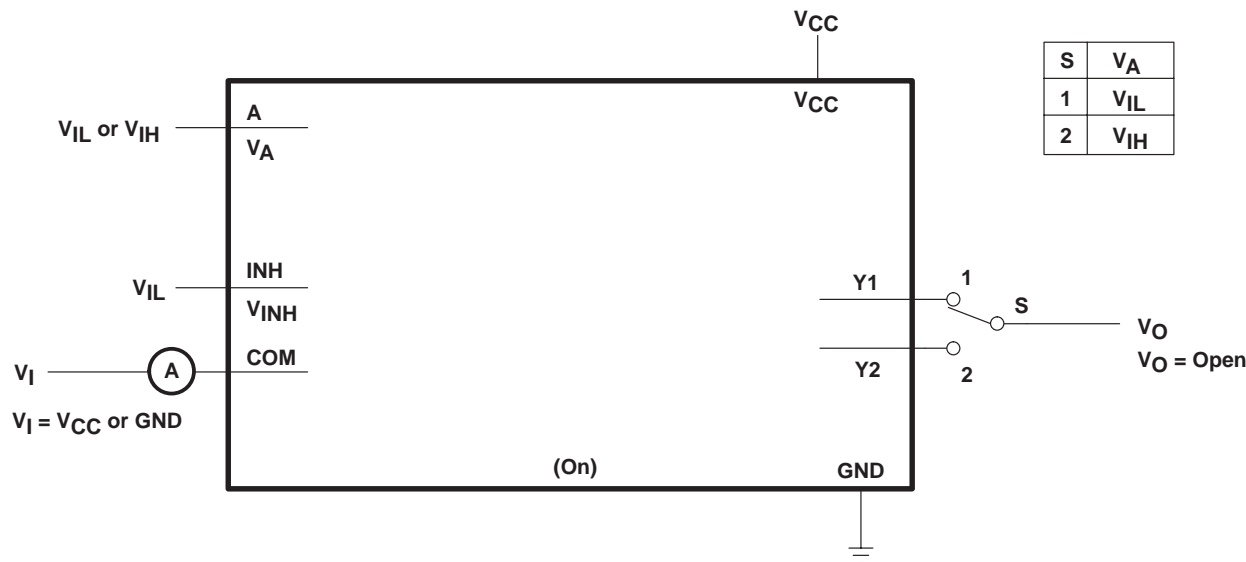


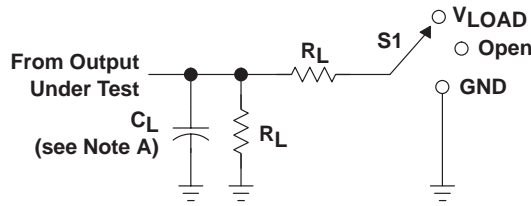
Figure 4. On-State Switch Leakage-Current Test Circuit

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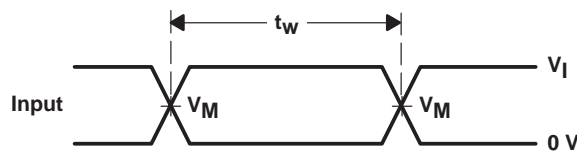
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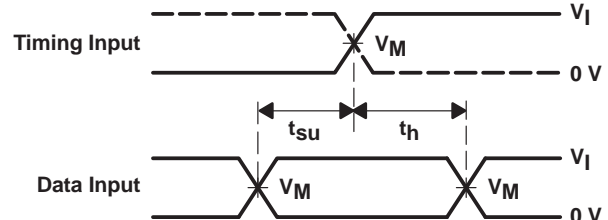
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

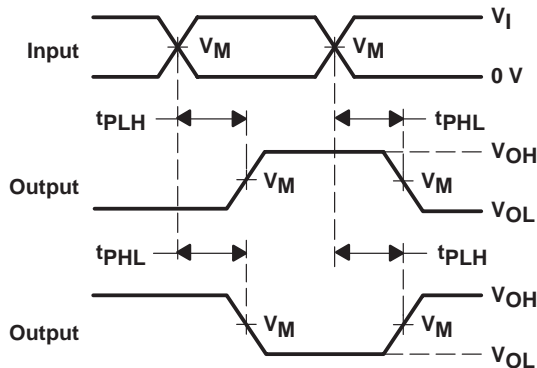
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
0.8 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.1 V
$1.2 \text{ V} \pm 0.1 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.1 V
$1.5 \text{ V} \pm 0.1 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.1 V
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.15 V
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V



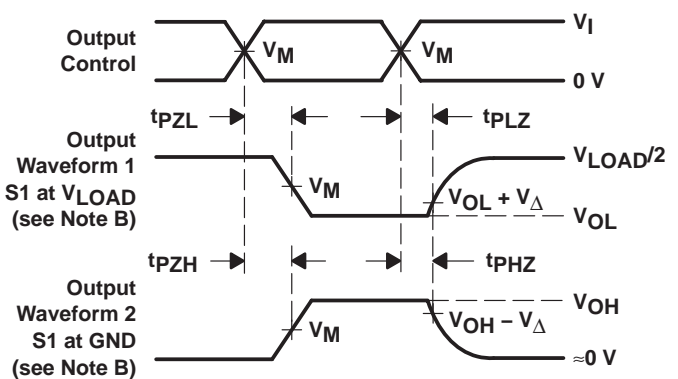
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, slew rate $\geq 1 \text{ V/ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms



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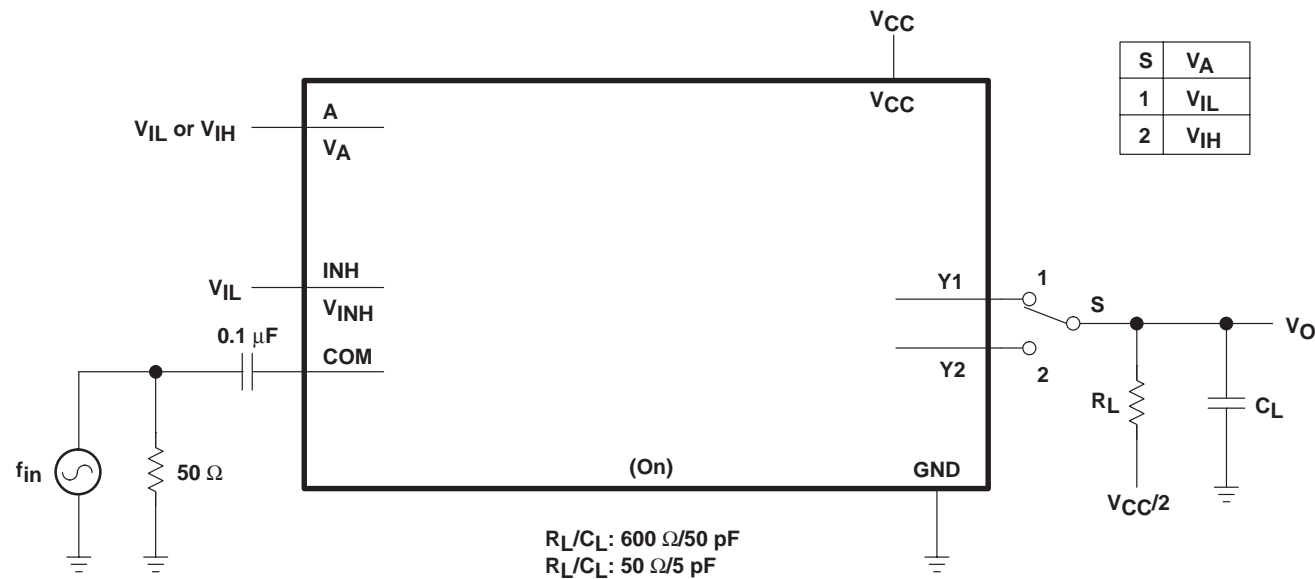


Figure 6. Frequency Response (Switch On)

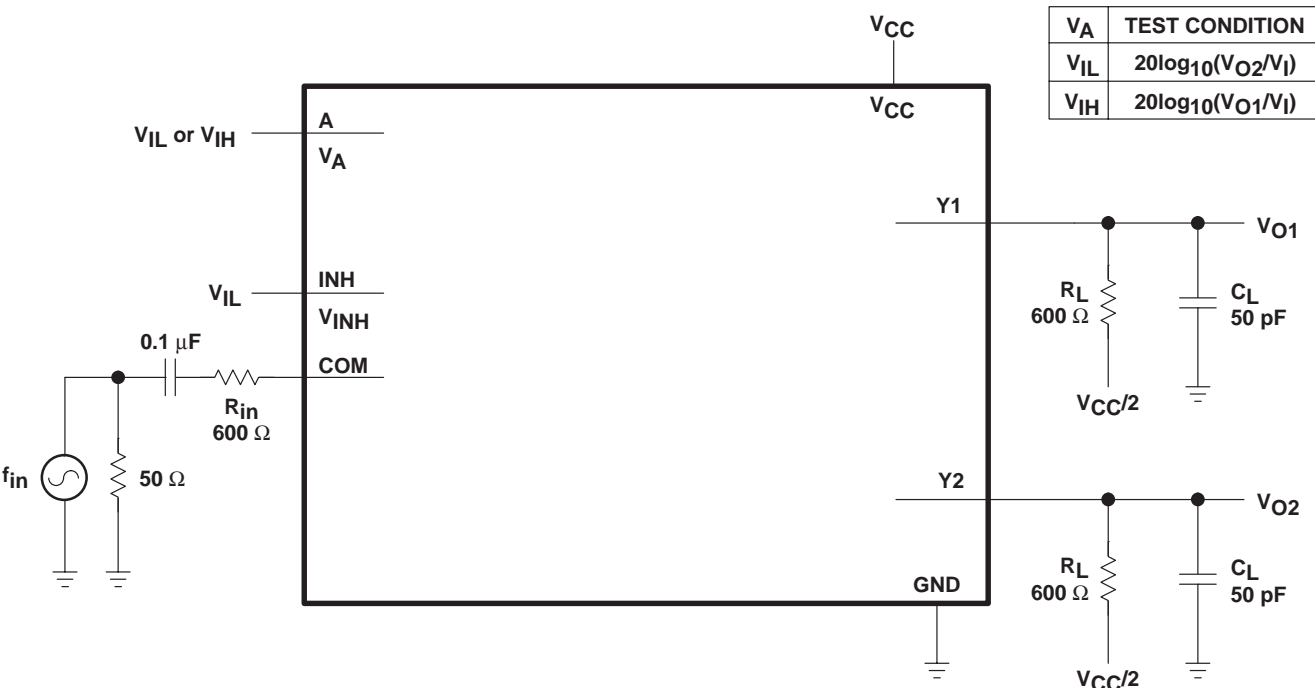


Figure 7. Crosstalk (Between Switches)

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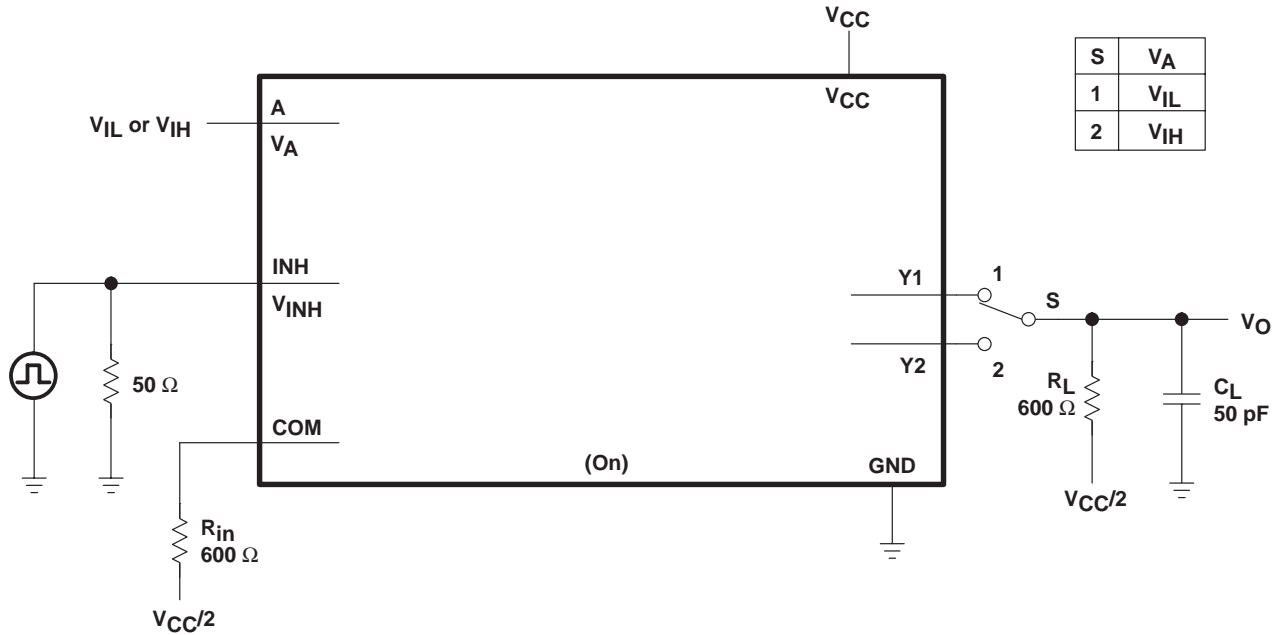


Figure 8. Crosstalk (Control Input, Switch Output)

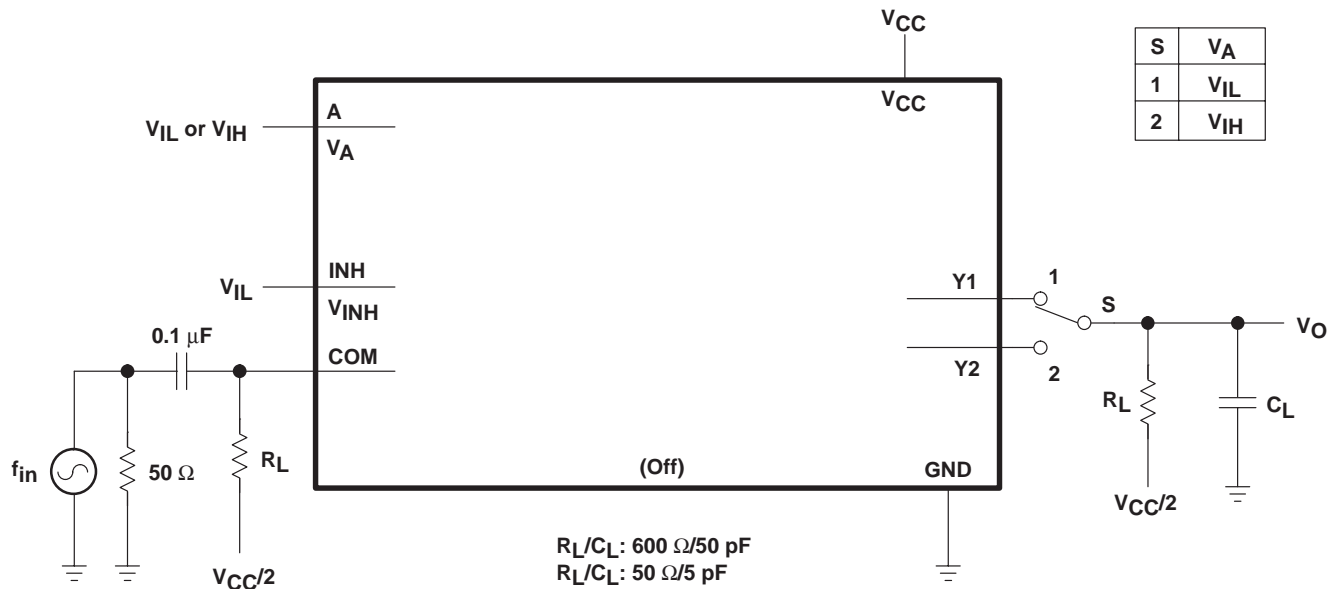


Figure 9. Feedthrough (Switch Off)

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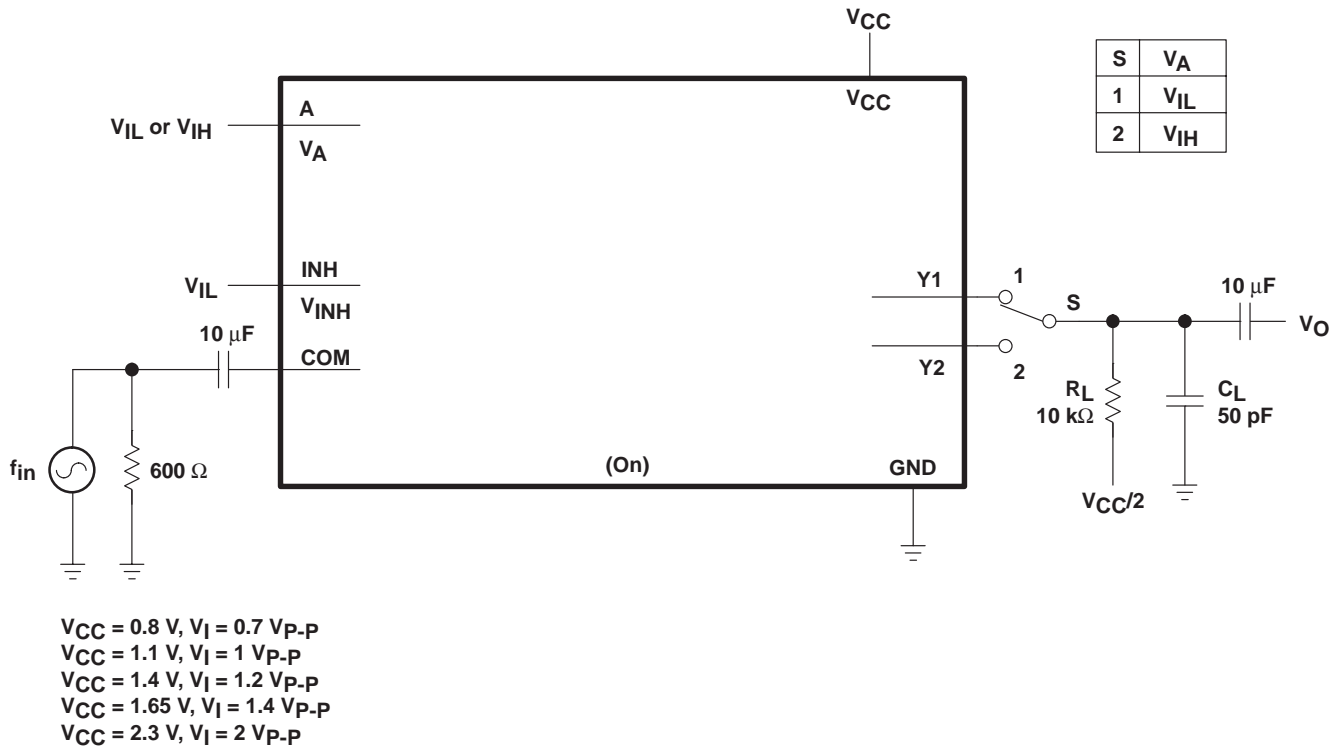


Figure 10. Sine-Wave Distortion

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AUC2G53DCTR	ACTIVE	SM8	DCT	8	3000	None	CU SNPB	Level-1-235C-UNLIM
SN74AUC2G53DCUR	ACTIVE	US8	DCU	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G53YEPR	ACTIVE	WCSP	YEP	8	3000	None	SNPB	Level-1-260C-UNLIM
SN74AUC2G53YZPR	ACTIVE	WCSP	YZP	8	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

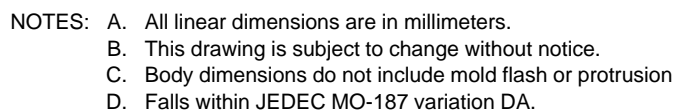
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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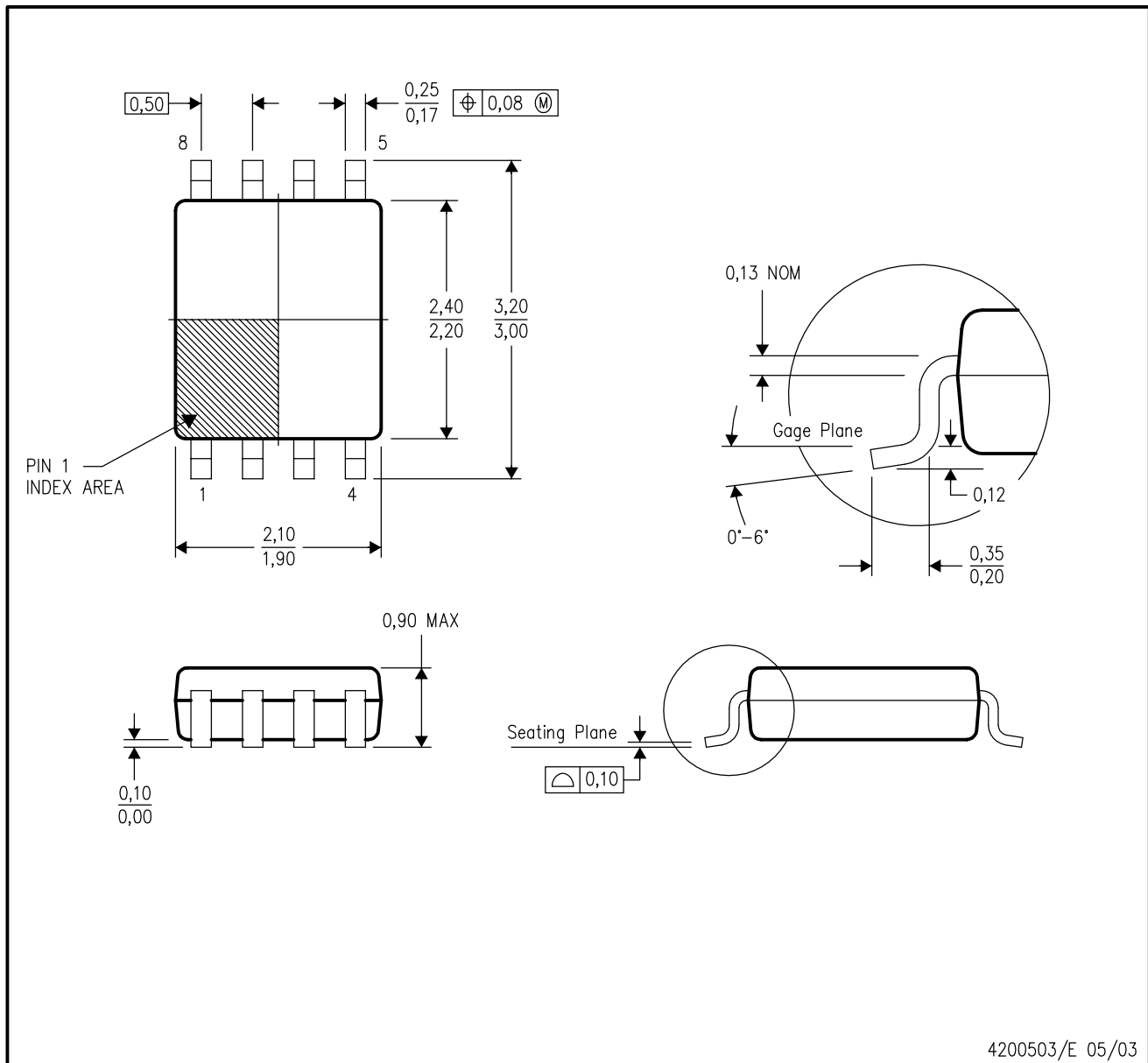
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PLASTIC SMALL-OUTLINE PACKAGE



DCU (R-PDSO-G8)

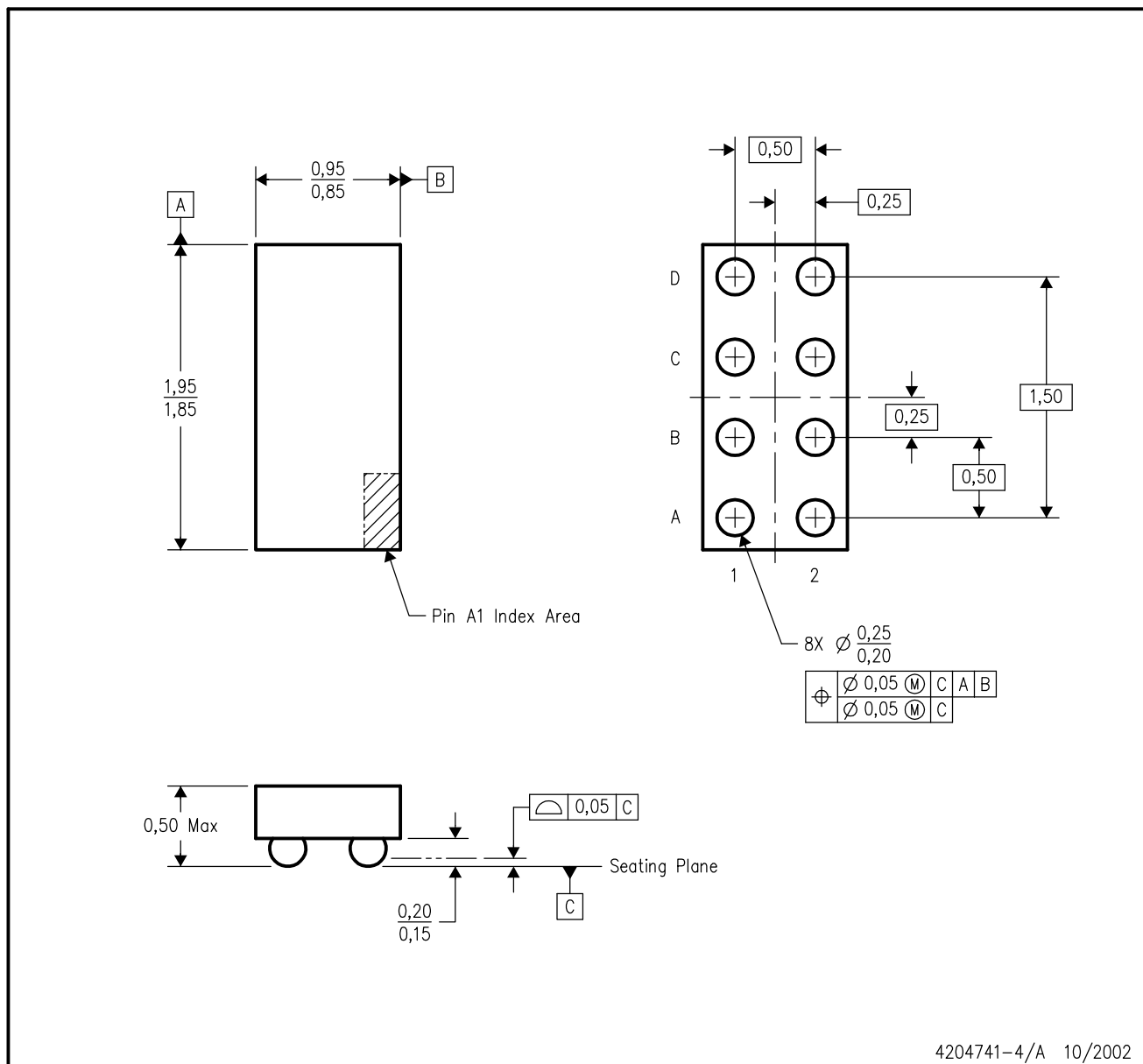
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation CA.

YZP (R-XBGA-N8)

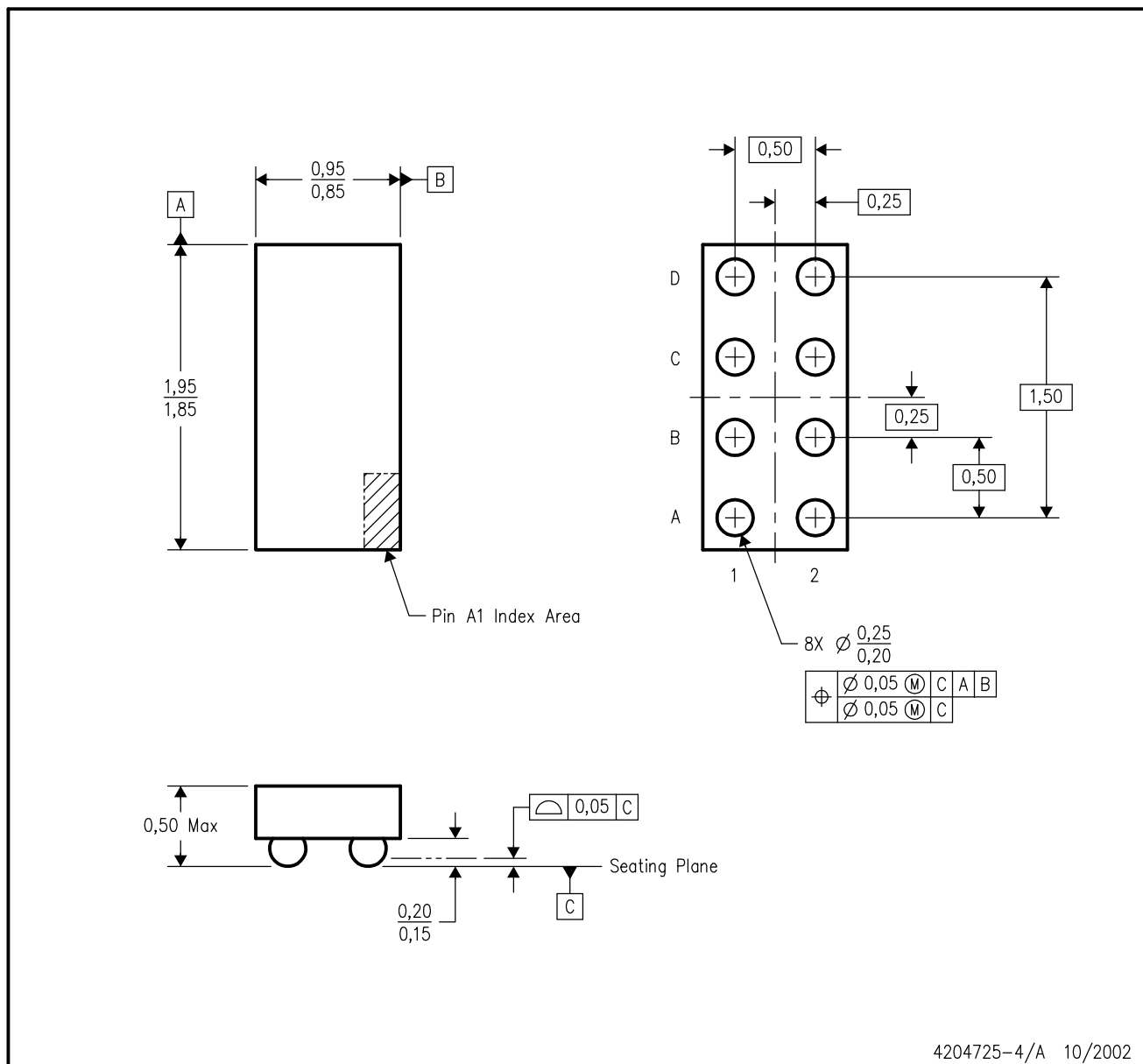
DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

YEP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead-free.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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