



Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (32K x 8-BIT)

IDT71256SA

FEATURES:

- 32K x 8 advanced high-speed CMOS static RAM
- Commercial (0° to 70°C) and Industrial (-40° to 85°C) temperature options
- Equal access and cycle times
 - Commercial: 12/15/20/25ns
 - Industrial: 15/20ns
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Commercial product available in 28-pin 300- and 600-mil Plastic DIP, 300 mil Plastic SOJ and TSOP packages
- Industrial product available in 28-pin 300 mil Plastic SOJ and TSOP packages

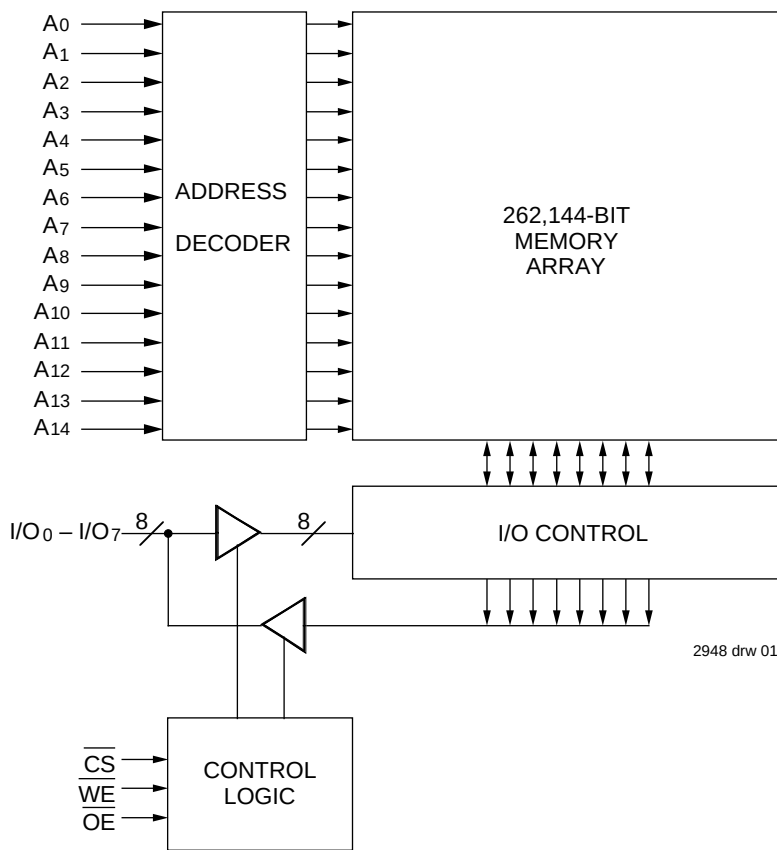
DESCRIPTION:

The IDT71256SA is a 262,144-bit high-speed Static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71256SA has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns. All bidirectional inputs and outputs of the IDT71256SA are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71256SA is packaged in 28-pin 300- and 600-mil Plastic DIP, 28-pin 300 mil Plastic SOJ and TSOP.

FUNCTIONAL BLOCK DIAGRAM

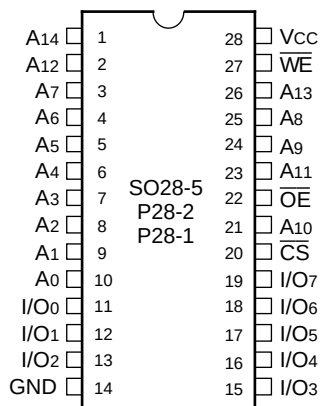


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INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

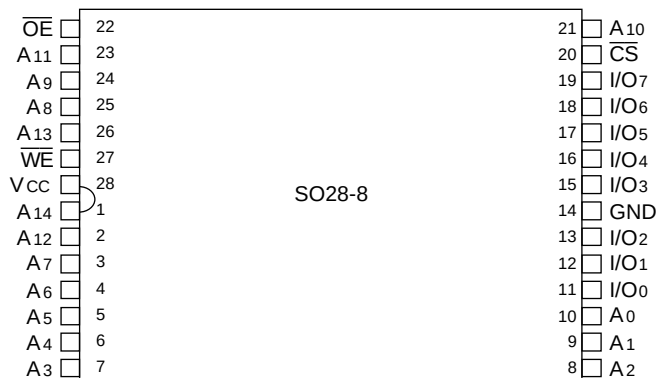
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PIN CONFIGURATIONS



2948 drw 02

DIP/SOJ
TOP VIEW



2948 drw 11

TSOP
TOP VIEW

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	4.5V to 5.5V
Industrial	-40°C to +85°C	0V	4.5V to 5.5V

3948 tbl 09

DC ELECTRICAL CHARACTERISTICS

Vcc = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71256SA		Unit
			Min.	Max.	
I _{LI}	Input Leakage Current	Vcc = Max., V _{IN} = GND to Vcc	—	5	μA
I _{LO}	Output Leakage Current	Vcc = Max., $\overline{CS}$ = V _{IH} , V _{OUT} = GND to Vcc	—	5	μA
V _{OL}	Output Low Voltage	I _{OL} = 8mA, Vcc = Min.	—	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -4mA, Vcc = Min.	2.4	—	V

2948 tbl 05

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
Vcc	Supply Voltage Relative to GND	-0.5 to +7.0	V
V _{TERM}	Terminal Voltage Relative to GND	-0.5 to Vcc+0.5	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	50	mA

NOTES:

2948 tbl 02

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE^(1,2)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	DATA _{OUT}	Read Data
L	X	L	DATA _{IN}	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected — Standby (I _{SB})
V _{HC} ⁽³⁾	X	X	High-Z	Deselected — Standby (I _{SB1})

NOTES:

2948 tbl 04

- H = V_{IH}, L = V_{IL}, X = Don't care.
- V_{LC} = 0.2V, V_{HC} = Vcc - 0.2V.
- Other inputs ≥ V_{HC} or ≤ V_{LC}.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	Vcc+0.5	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

2948 tbl 01

- V_{IL} (min.) = -1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

($V_{CC} = 5.0V \pm 10\%$, $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$)

Symbol	Parameter	71256SA12 ⁽³⁾	71256SA15	71256SA20	71256SA25 ⁽³⁾	Unit
I _{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, $V_{CC} = \text{Max.}$, $f = f_{\text{MAX}}$ ⁽²⁾	160	150	145	145	mA
I _{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, $V_{CC} = \text{Max.}$, $f = f_{\text{MAX}}$ ⁽²⁾	50	40	40	40	mA
I _{SB1}	Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, $V_{CC} = \text{Max.}$, $f = 0$ ⁽²⁾ $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	15	15	15	15	mA

NOTES:

- All values are maximum guaranteed values.
- $f_{\text{MAX}} = 1/t_{\text{RC}}$ (all address inputs are cycling at f_{MAX}); $f = 0$ means no address input lines are changing.
- Commercial temperature range only.

2948 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2948 tbl 07

CAPACITANCE

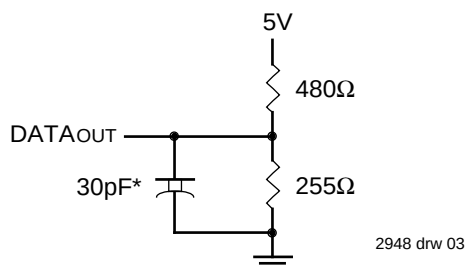
($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$, SOJ package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	$V_{IN} = 3\text{dV}$	7	pF
C _{I/O}	I/O Capacitance	$V_{OUT} = 3\text{dV}$	7	pF

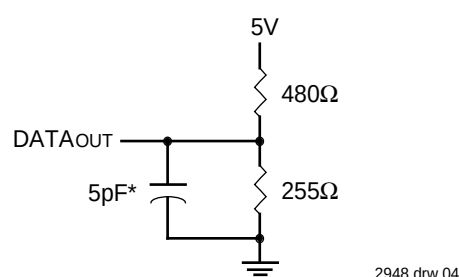
NOTE:

- This parameter is guaranteed by device characterization, but not production tested.

2948 tbl 03



2948 drw 03



2948 drw 04

*Including jig and scope capacitance.

Figure 1. AC Test Load

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

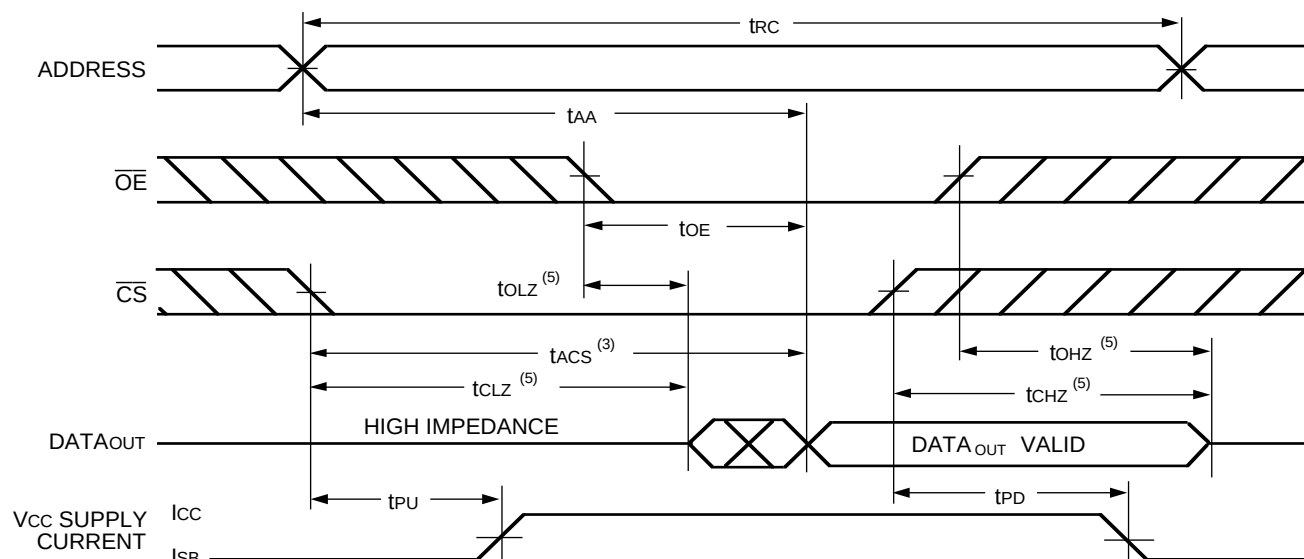
Symbol	Parameter	71256SA12 ⁽²⁾		71256SA15		71256SA20		71256SA25 ⁽²⁾		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	12	—	15	—	20	—	25	—	ns
tAA	Address Access Time	—	12	—	15	—	20	—	25	ns
tACS	Chip Select Access Time	—	12	—	15	—	20	—	25	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low-Z	4	—	4	—	4	—	4	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High-Z	0	6	0	7	0	10	0	11	ns
tOE	Output Enable to Output Valid	—	6	—	7	—	10	—	11	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
tOHZ ⁽¹⁾	Output Disable to Output in High-Z	0	6	0	6	0	8	0	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tPU ⁽¹⁾	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
tPD ⁽¹⁾	Chip Deselect to Power Down Time	—	12	—	15	—	20	—	25	ns
Write Cycle										
tWC	Write Cycle Time	12	—	15	—	20	—	25	—	ns
tAW	Address Valid to End of Write	9	—	10	—	15	—	20	—	ns
tCW	Chip Select to End of Write	9	—	10	—	15	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	9	—	10	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tdW	Data Valid to End of Write	6	—	7	—	11	—	13	—	ns
tdH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tOW ⁽¹⁾	Output Active from End of Write	4	—	4	—	4	—	4	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High-Z	0	6	0	6	0	10	0	11	ns

NOTE:

1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. Commercial temperature range only.

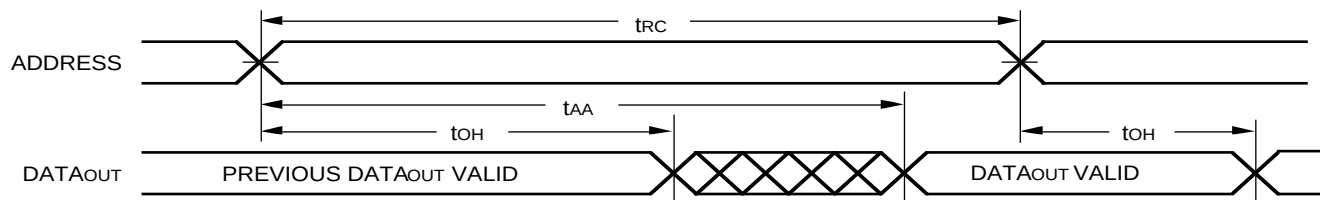
2948 tbl 08

TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



2948 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2^(1,2,4)

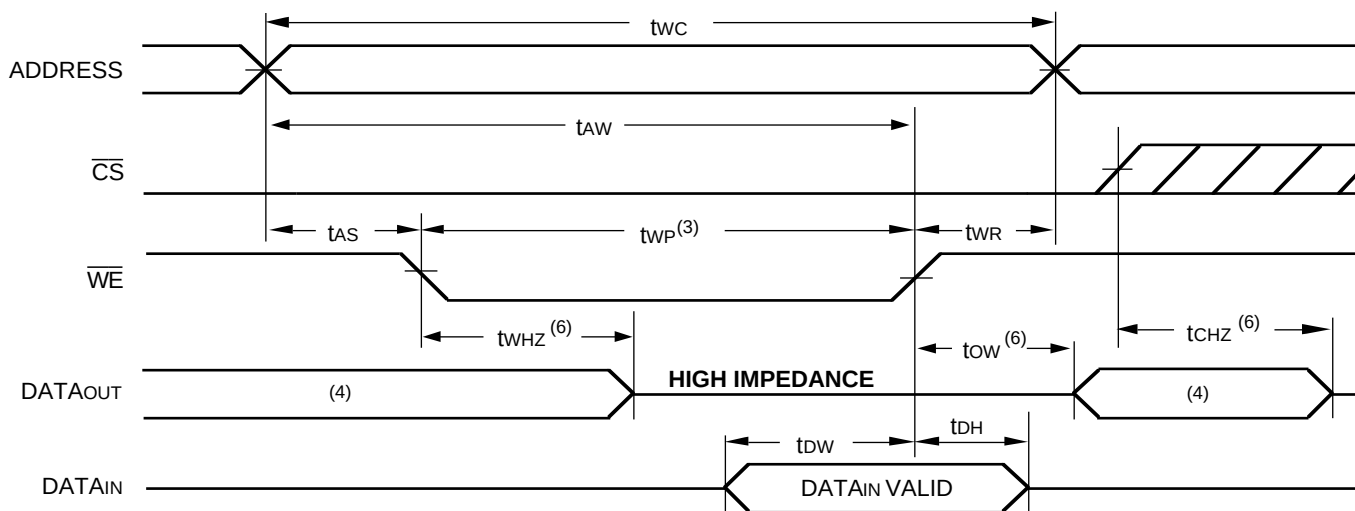


2948 drw 06

NOTES:

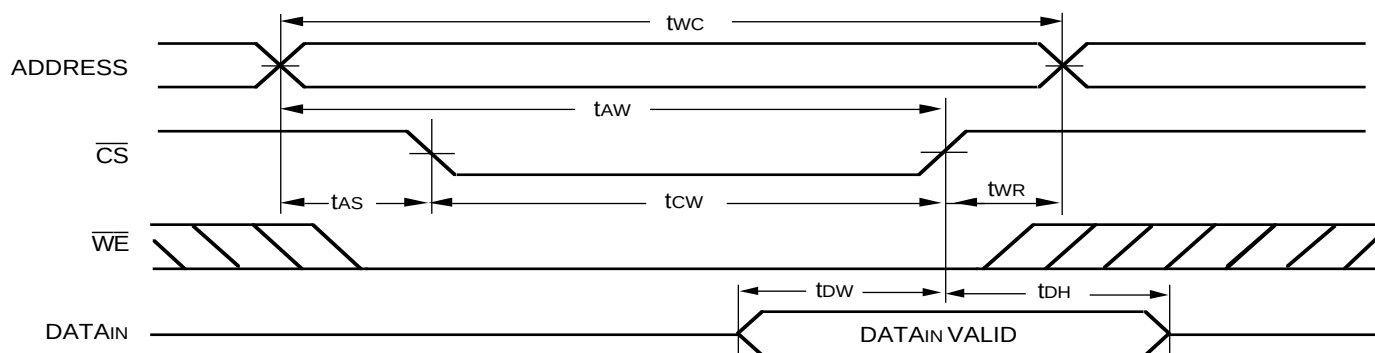
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)^(1,2,3,5)



2948 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)^(1,2,5)

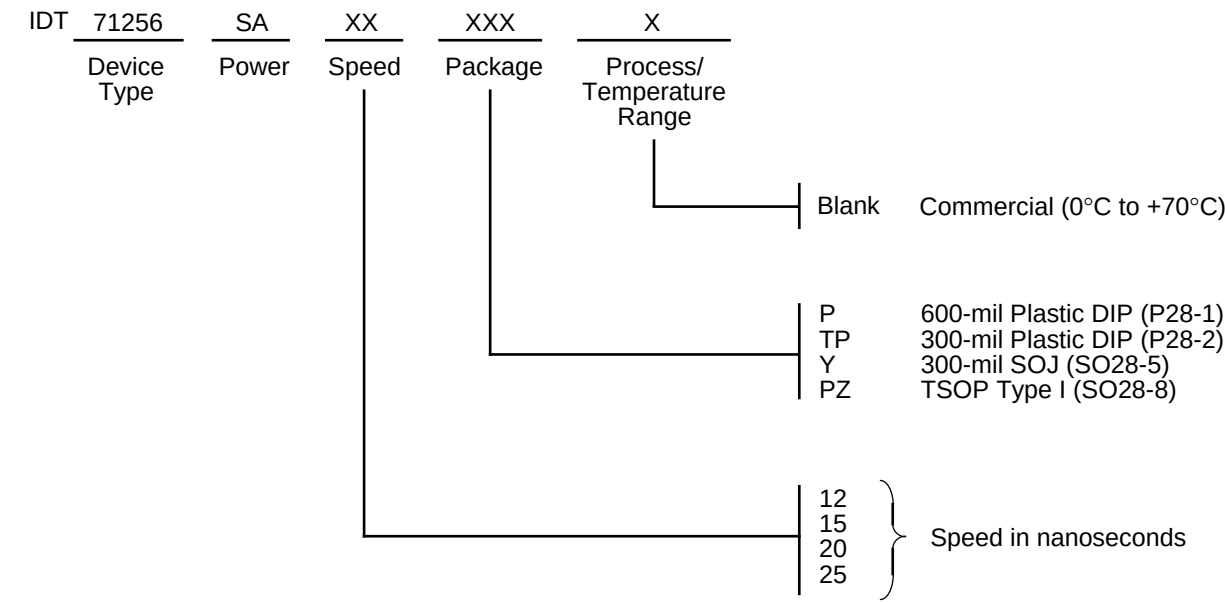


2948 drw 08

NOTES:

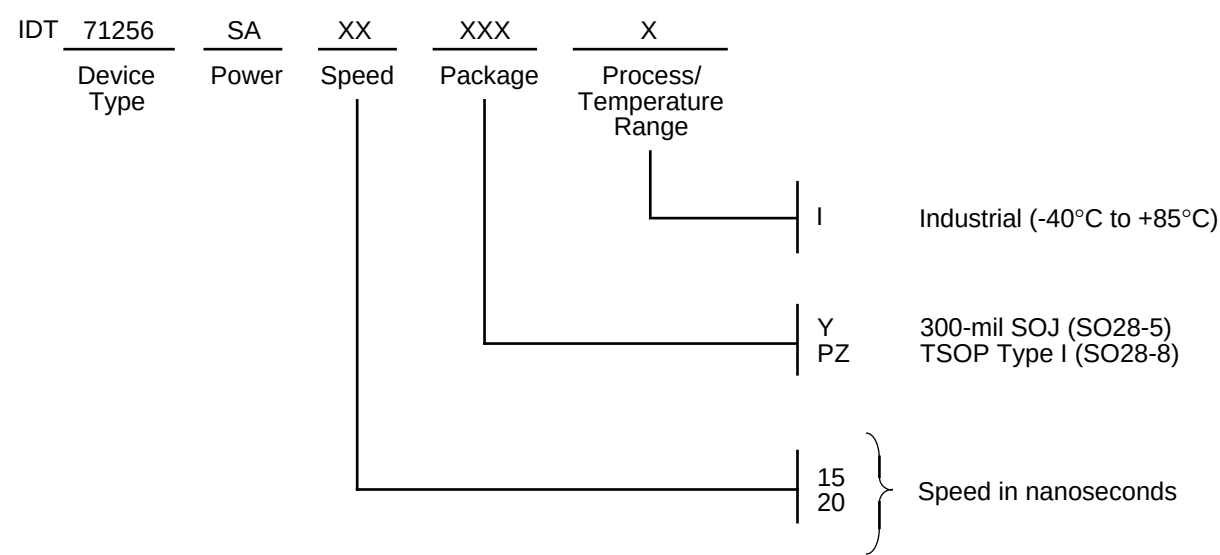
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.

ORDERING INFORMATION - COMMERCIAL



2948 drw 09

ORDERING INFORMATION - INDUSTRIAL



2948 drw 10