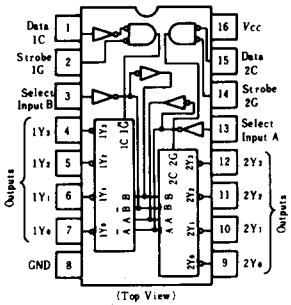
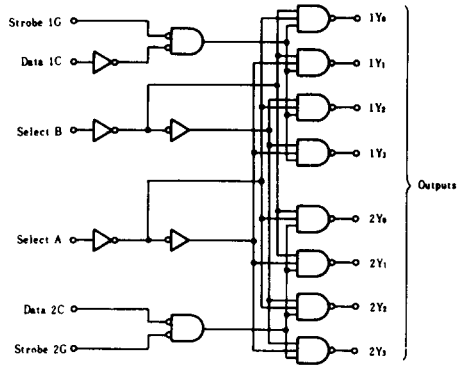
HD74LS156 ●Dual 2-line-to-4-line Decoders/Demultiplexers (with open collector outputs)

This circuit features dual 1-line-to-4-line demultiplexer with individual strobes and common binary-address inputs. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating.

■PIN ARRANGEMENT



■BLOCK DIAGRAM



■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
High level output voltage	V_{OH}	—	—	5.5	V
Low level output current	I_{OL}	—	—	8	mA

■FUNCTION TABLE

●2-to-4-line Decoder/1-to-4-line Demultiplexer

Inputs				Outputs				Inputs				Outputs			
SELECT		STROBE	DATA					SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3	B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
×	×	H	×	H	H	H	H	×	×	H	×	H	H	H	H
L	L	L	H	L	H	H	H	L	L	L	L	L	H	H	H
L	H	L	H	H	L	H	H	L	H	L	L	H	L	H	H
H	L	L	H	H	H	L	H	H	L	L	L	H	H	L	H
H	H	L	H	H	H	H	L	H	H	L	L	H	H	H	L
×	×	×	L	H	H	H	H	×	×	×	H	H	H	H	H

●3-to-8-line Decoder/1-to-8-line Demultiplexer

Inputs				Outputs							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C[1]	B	A	G[2]	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
×	×	×	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Notes) 1. C; input 1C and 2C connected together
2. G; inputs 1G and 2G connected together
3. H; high level, L; low level, X; irrelevant

HITACHI

■ELECTRICAL CHARACTERISTICS ($Ta=-20\sim+75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	–	–	V
	V_{IL}			–	–	0.8	V
Output current	I_{OH}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V, V_{OH}=5.5V		–	–	100	μA
Output voltage	V_{OL}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V	I_{OL}=4mA	–	–	0.4	V
			I_{OL}=8mA	–	–	0.5	
Input current	I_{IH}	V_{CC}=5.25V, V_I=2.7V		–	–	20	μA
	I_{IL}	V_{CC}=5.25V, V_I=0.4V		–	–	−0.4	mA
	I_I	V_{CC}=5.25V, V_I=7V		–	–	0.1	mA
Supply current**	I_{CC}	V_{CC}=5.25V		–	6.1	10	mA
Input clamp voltage	V_{IK}	V_{CC}=4.75V, I_{IN}=−18mA		–	–	−1.5	V

* V_{CC}=5V, Ta=25°C

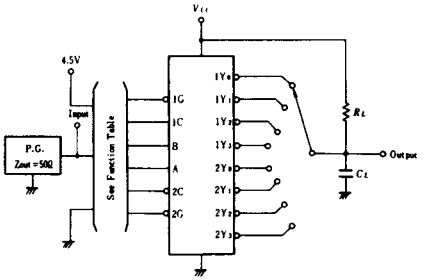
** I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5V, and 2C, 1G, and 2G inputs grounded.

■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C)

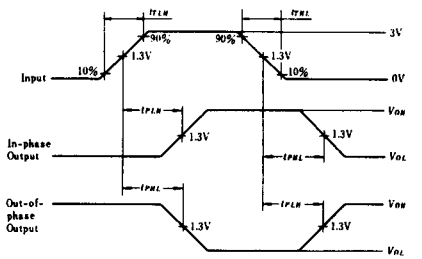
Item	Symbol	Inputs	Output	Level of logic	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	A, B, 2C, 1G or 2G	Y	2	C_L=15pF, R_L=2kΩ	–	25	40	ns
	t_{PHL}	A, B, 2C, 1G or 2G	Y	2		–	34	51	
	t_{PLH}	A or B	Y	3		–	31	46	
	t_{PHL}	A or B	Y	3		–	34	51	
	t_{PLH}	1C	Y	3		–	32	48	
	t_{PHL}	1C	Y	3		–	32	48	

■TESTING METHOD

1) Test Circuit



Waveform



Notes) 1. Input pulse; $t_{TLH}\leqq$15ns, $t_{THL}\leqq$6ns, PRR=1MHz, duty cycle=50%.

2. C_L includes probe and jig capacitance.

PACKAGING INFORMATIONS

T-90-20

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

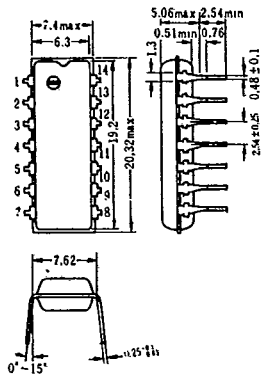
HD 74LS00 P

- Package ; Plastic DIP ; letters P
  Cerdip ; non-letters
- Circuit description
- Prefix : HD ; Hitachi Digital IC

■Plastic DIP

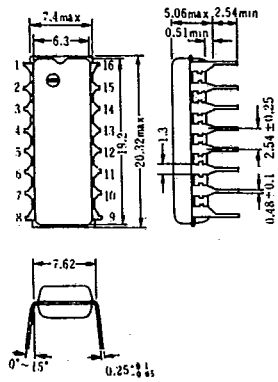
●14 Pin

DP-14



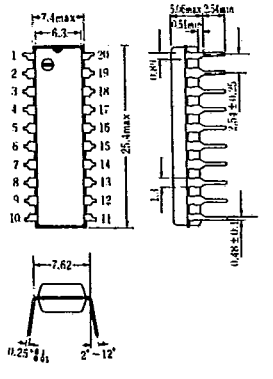
●16 Pin

DP-16



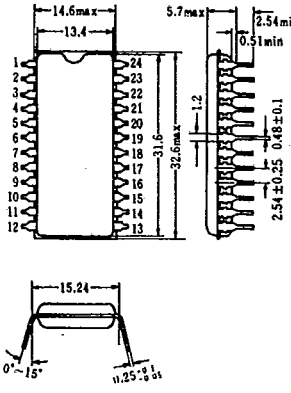
●20 Pin

DP-20



●24 Pin

DP-24



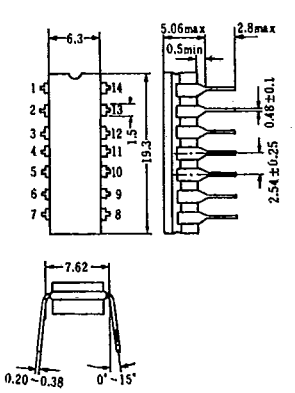
Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

PACKAGING INFORMATIONS

■Cerdip

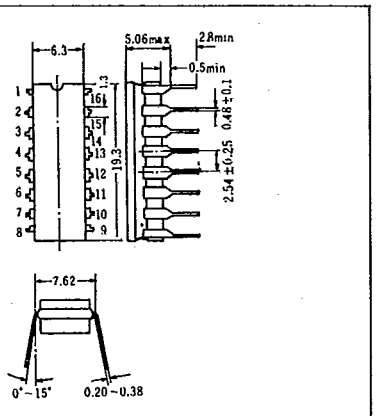
●14 Pin

DG-14



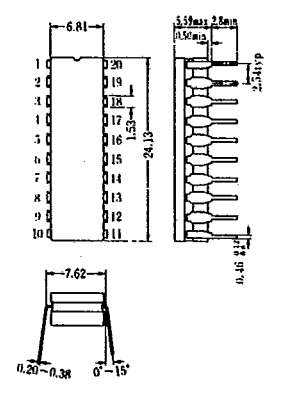
●16 Pin

DG-16



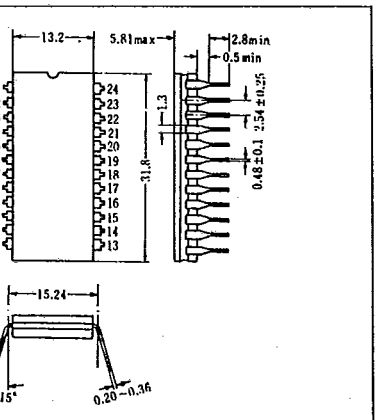
●20 Pin

DG-20



●24 Pin

DG-24



HITACHI
Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300