

9-IN 3-OUT STEREO AUDIO SELECTOR

■ GENERAL DESCRIPTION

NJW1110 is a 9-input 3-output stereo audio selector. It includes three independent 9input-1output stereo audio selectors and adjustable gain buffers.

NJW1110 performs superior audio characteristics such as low distortion, low output noise and low crosstalk. All of internal status and variables are controlled by I²C BUS interface. And the slave address selector is available for using two chips on same serial Bus line. It is suitable for latest TV system and others.

■ PACKAGE OUTLINE



NJW1110V

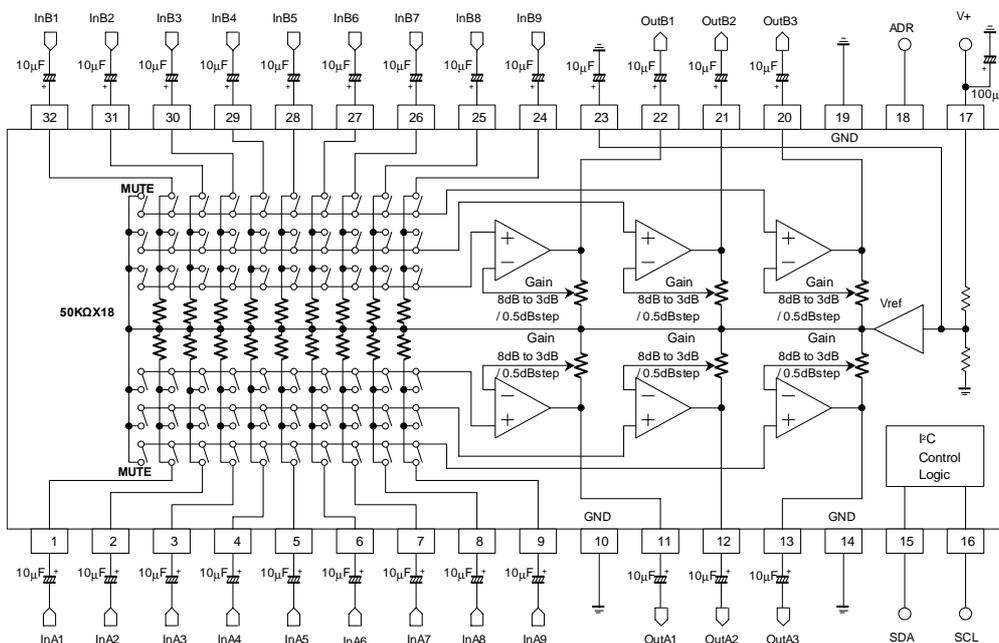
■ APPLICATIONS

- FPD TV
- Car Audio System
- Monitor

■ FEATURES

- Operating Voltage 7.5 to 15V
- Operating Current 8mA typ.
- 9-Input, 3-Output Stereo Audio Selector
- Low Distortion 0.0007% typ.
- Low Output Noise 116dB typ.
- Low Crosstalk 110dB typ.
- Channel Separation 100dB typ.
- Variable Gain Buffer 0, 3 to 8dB/0.5dB step
- I²C Bus Interface (Comply with fast mode and 3V I/F)
- Selectable 2-Slave Address
- Bi-CMOS Technology
- Package Outline SSOP32

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V ⁺	16	V
Maximum input voltage	V _{IM}	0 to V ⁺ (^{*)})	V
Power Dissipation	P _D	800 <small>NOTE: EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting</small>	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +125	°C

(*)For the maximum input voltage less than V⁺.

■ RECOMMENDED OPERATING CONDITIONS (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V ⁺	-	7.5	9.0	15.0	V

■ ELECTRICAL CHARACTERISTICS

◆ Power Supply (Ta=25°C, V⁺=9V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	I _{CC}	No Signal	4.0	8.0	12.0	MA
Reference Voltage	V _{REF}	No Signal	4.0	4.5	5.0	V

◆ AC CHARACTERISTICS (Ta=25°C, V⁺=9V, V_{IN}=0dBV (0dBV=1Vrms), f=1kHz, R_L=47kΩ)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Output Voltage	V _{OM}	THD=1%	6.0 (2.0)	8.0 (2.5)	-	dBV (Vrms)
Voltage Gain 1	G _{V1}	-	-1.0	0	1.0	dB
Voltage Gain 2	G _{V2}	V _{IN} =200mVrms, Gain=6dB	5.0	6.0	7.0	
Total Harmonic Distortion 1	THD1	BW=400Hz-30kHz	-	0.001	0.02	%
Total Harmonic Distortion 2	THD2	f=10kHz, BW=400Hz-30kHz	-	0.003	-	
Total Harmonic Distortion 3	THD3	V ⁺ =12V, BW=400Hz-30kHz	-	0.0007	-	
Output Noise	V _{NO}	Rg=0Ω, A-Weighted	-	-116 (1.6)	-106 (5.0)	dBV (μVrms)
Cross Talk 1	CT1	Rg=0Ω, A-Weighted	-	-110	-	dB
Cross Talk 2	CT2	Rg=0Ω, f=20kHz	-	-90	-	
Channel Separation 1	CS1	Rg=0Ω, A-Weighted	-	-110	-	dB
Channel Separation 2	CS2	Rg=0Ω, f=20kHz	-	-90	-	

BW: Band Width

◆ Logic Control Characteristics (Ta=25°C, V⁺=9V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Input Voltage	V _{ADRH}	ADR Terminal	2.5	-	V ⁺	V
Low Level Input Voltage	V _{ADRL}	ADR Terminal	0	-	1.5	

■ I²C BUS BLOCK CHARACTERISTICS (SDA,SCL)

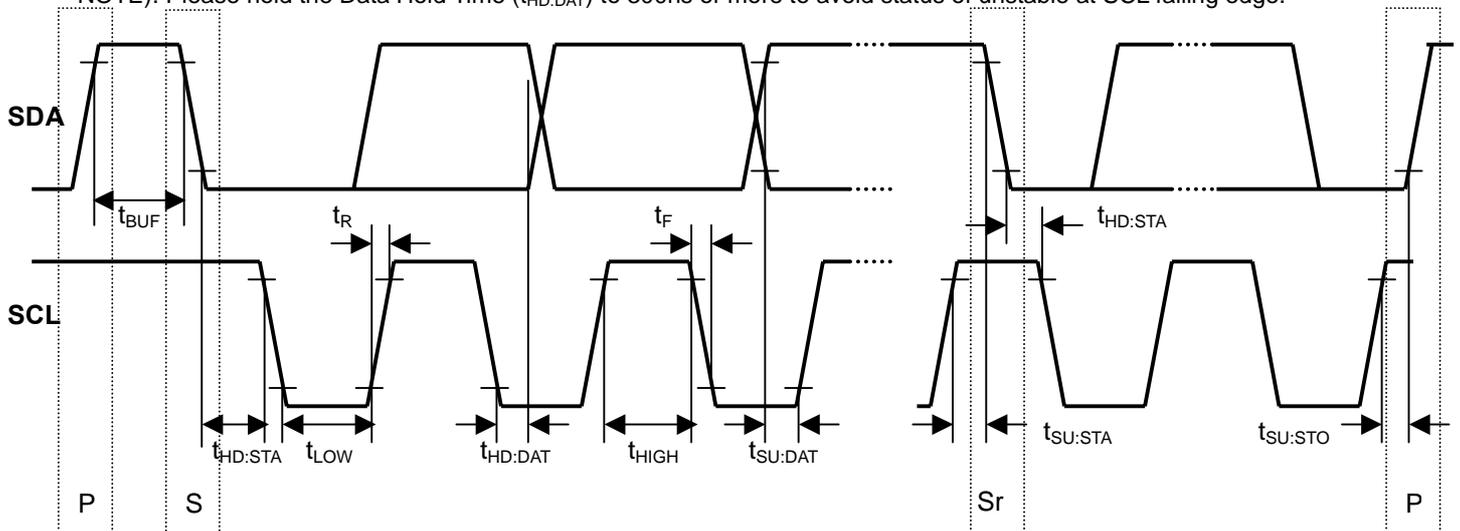
Standard mode : I²C BUS Load Conditions: Pull up resistance 4kΩ (Connected to +5V), Load capacitance 200pF (Connected to GND)

Fast mode : I²C BUS Load Conditions: Pull up resistance 4kΩ (Connected to +5V), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Low Level Input Voltage	V _{IL}	0.0	-	1.5	0.0	-	1.5	V
High Level Input Voltage	V _{IH}	2.7	-	5.0	2.7	-	5.0	V
Hysteresis of Schmitt trigger inputs	V _{hys}	-	-	-	0.25	-	-	V
Low level output voltage (3mA at SDA pin)	V _{OL}	0	-	0.4	0	-	0.4	V
Output fall time from V _{IHmin} to V _{ILmax} with a bus capacitance from 10pF to 400pF	t _{of}	-	-	250	20 +0.1C _b	-	250	ns
Pulse width of spikes which must be suppressed by the input filter	t _{SP}	-	-	-	0	-	50	ns
Input current each I/O pin with an input voltage between 0.1V _{DD} and 0.9V _{DDmax}	I _i	-10	-	10	-10	-	10	μA
Capacitance for each I/O pin	C _i	-	-	10	-	-	10	pF
SCL clock frequency	f _{SCL}	-	-	100	-	-	400	kHz
Hold time (repeated) START condition.	t _{HD:STA}	4.0	-	-	0.6	-	-	μs
Low period of the SCL clock	t _{LOW}	4.7	-	-	1.3	-	-	μs
High period of the SCL clock	t _{HIGH}	4.0	-	-	0.6	-	-	μs
Set-up time for a repeated START condition	t _{SU:STA}	4.7	-	-	0.6	-	-	μs
Data hold time	t _{HD:DAT}	0	-	-	0	-	-	μs
Data set-up time	t _{SU:DAT}	250	-	-	100	-	-	ns
Rise time of both SDA and SCL signals	t _r	-	-	1000	-	-	300	ns
Fall time of both SDA and SCL signals	t _f	-	-	300	-	-	300	ns
Set-up time for STOP condition	t _{SU:STO}	4.0	-	-	0.6	-	-	μs
Bus free time between a STOP and START condition	t _{BUF}	4.7	-	-	1.3	-	-	μs
Capacitive load for each bus line	C _b	-	-	400	-	-	400	pF
Noise margin at the Low level	V _{nL}	0.5	-	-	0.5	-	-	V
Noise margin at the High level	V _{nH}	1	-	-	1	-	-	V

C_b: total capacitance of one bus line in pF.

NOTE). Please hold the Data Hold Time (t_{HD:DAT}) to 300ns or more to avoid status of unstable at SCL falling edge.



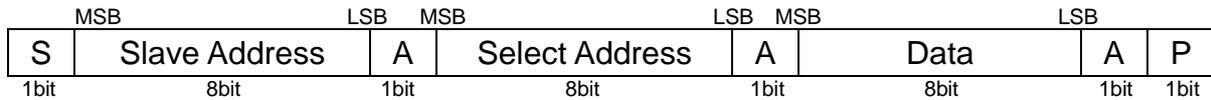
■ PIN CONFIGURATION



No.	Symbol	Function	No.	Symbol	Function
1	InA1	Ach Input 1	17	V+	Power Supply Terminal
2	InA2	Ach Input 2	18	ADR	Slave address setting terminal
3	InA3	Ach Input 3	19	GND	GND Terminal
4	InA4	Ach Input 4	20	OutB3	Bch Output 3
5	InA5	Ach Input 5	21	OutB2	Bch Output 2
6	InA6	Ach Input 6	22	OutB1	Bch Output 1
7	InA7	Ach Input 7	23	Vref	Reference Voltage
8	InA8	Ach Input 8	24	InB9	Bch Input 9
9	InA9	Ach Input 9	25	InB8	Bch Input 8
10	GND	GND Terminal	26	InB7	Bch Input 7
11	OutA1	Ach Output 1	27	InB6	Bch Input 6
12	OutA2	Ach Output 2	28	InB5	Bch Input 5
13	OutA3	Ach Output 3	29	InB4	Bch Input 4
14	GND	GND Terminal	30	InB3	Bch Input 3
15	SDA	SDA Data Input (I ² C BUS)	31	InB2	Bch Input 2
16	SCL	SCL Clock Input (I ² C BUS)	32	InB1	Bch Input 1

■ DEFINITION OF I²C REGISTER

◆ I²C BUS FORMAT



S: Starting Term

A: Acknowledge Bit

P: Ending Term

◆ SLAVE ADDRESS

MSB								LSB	
	1	0	0	1	0	1	0	R/W	94H(ADR=Low)
	1	0	0	1	0	1	1	R/W	96H(ADR=High)

R/W=0: Receive Only

$\overline{R/W}$ =0: Write mode for register setting

$\overline{R/W}$ =1: Not available

◆ CONTROL REGISTER TABLE

The select address and sets each function.

The auto increment function cycles the select address as follows.

00H→01H→02H→00H

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	Variable Gain Buffer for OUT1				Input selector for OUT1			
01H	Variable Gain Buffer for OUT2				Input selector for OUT2			
02H	Variable Gain Buffer for OUT3				Input selector for OUT3			

◆ CONTROL REGISTER DEFAULT VALUE

Control register default value is all "0".

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	0	0	0	0	0	0	0	0
01H	0	0	0	0	0	0	0	0
02H	0	0	0	0	0	0	0	0

■ INPUT SELECTOR

● INPUT SELECTOR SETTING (OUT1:00H, OUT2:01H, OUT3:02H)

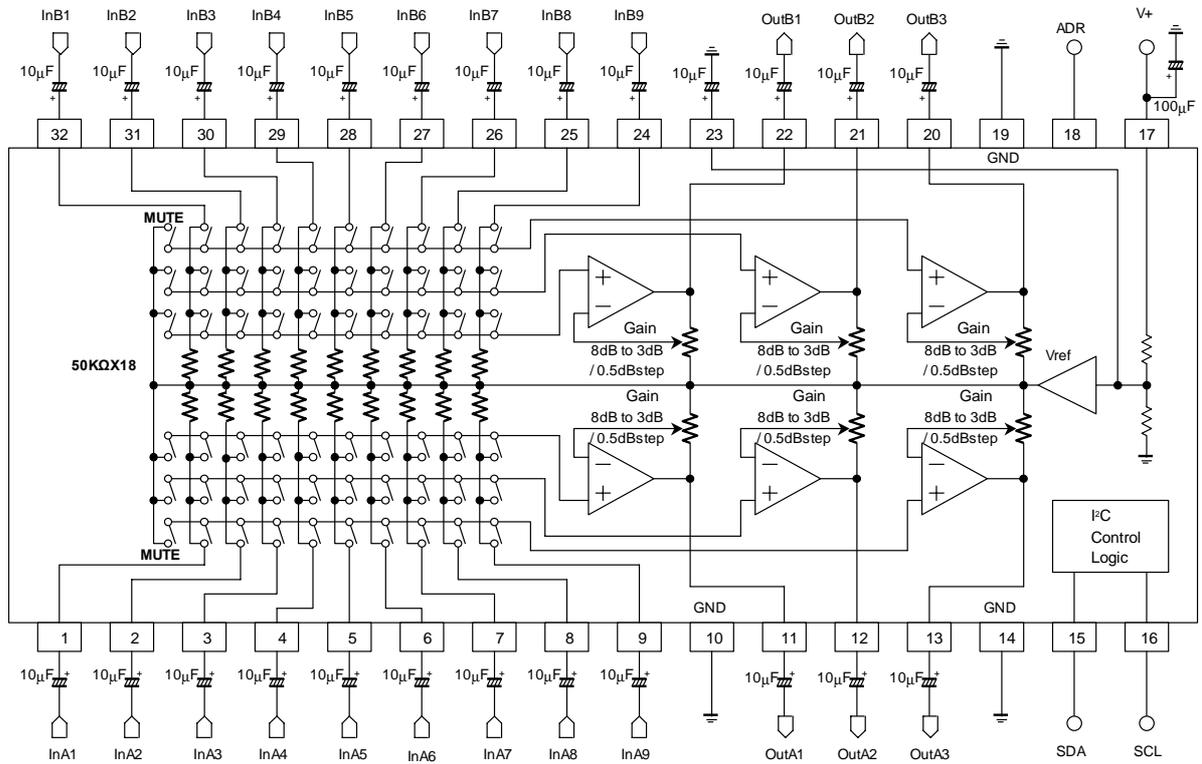
Signal Select	D3	D2	D1	D0
Mute	0	0	0	0
InA1/InB1	0	0	0	1
InA2/InB2	0	0	1	0
InA3/InB3	0	0	1	1
InA4/InB4	0	1	0	0
InA5/InB5	0	1	0	1
InA6/InB6	0	1	1	0
InA7/InB7	0	1	1	1
InA8/InB8	1	0	0	0
InA9/InB9	1	0	0	1

■ VARIABLE GAIN BUFFER

● VARIABLE GAIN BUFFER SETTING (OUT1:00H, OUT2:01H, OUT3:02H)

Gain (dB)	D7	D6	D5	D4
0	0	0	0	0
3.0	0	0	0	1
3.5	0	0	1	0
4.0	0	0	1	1
4.5	0	1	0	0
5.0	0	1	0	1
5.5	0	1	1	0
6.0	0	1	1	1
6.5	1	0	0	0
7.0	1	0	0	1
7.5	1	0	1	0
8.0	1	0	1	1

APPLICATION CIRCUIT



[CAUTION]
 The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.