

EP3645TTS-10.000M TR

[Click part number to visit Part Number Details page](#)

REGULATORY COMPLIANCE (Data Sheet downloaded on May 14, 2018)


[Click badges to download compliance docs](#)

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ITEM DESCRIPTION

Quartz Crystal Clock Oscillators XO (SPXO) LVCMOS (CMOS) 3.3Vdc 4 Pad 3.2mm x 5.0mm Ceramic Surface Mount (SMD) 10.000MHz ± 50 ppm -20°C to +70°C

ELECTRICAL SPECIFICATIONS

Nominal Frequency	10.000MHz
Frequency Tolerance/Stability	± 50 ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration)
Aging at 25°C	± 5 ppm/year Maximum
Operating Temperature Range	-20°C to +70°C
Supply Voltage	3.3Vdc $\pm 10\%$
Input Current	28mA Maximum (Unloaded)
Output Voltage Logic High (Voh)	Vdd-0.4Vdc Minimum (IOH = -8mA)
Output Voltage Logic Low (Vol)	0.4Vdc Maximum (IOL = +8mA)
Rise/Fall Time	4nSec Maximum (Measured at 20% to 80% of waveform)
Duty Cycle	50 ± 5 (%) (Measured at 50% of waveform)
Load Drive Capability	30pF Maximum
Output Logic Type	CMOS
Pin 1 Connection	Tri-State (Disabled Output: High Impedance)
Tri-State Input Voltage (Vih and Vil)	70% of Vdd Minimum to enable output, 20% of Vdd Maximum to disable output, No Connect to enable output.
Disable Current	16mA Maximum (Pin 1 = Ground)
Absolute Clock Jitter	± 250 pSec Maximum, ± 100 pSec Typical
One Sigma Clock Period Jitter	± 50 pSec Maximum
Start Up Time	10mSec Maximum
Storage Temperature Range	-55°C to +125°C

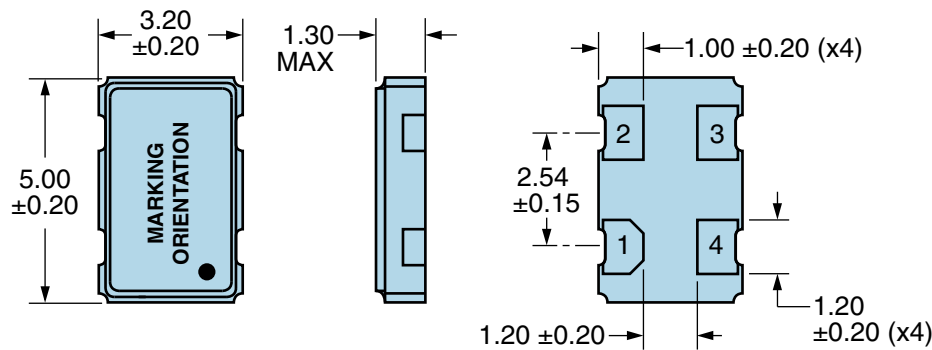
ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Fine Leak Test	MIL-STD-883, Method 1014, Condition A
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Mechanical Shock	MIL-STD-202, Method 213, Condition C
Resistance to Soldering Heat	MIL-STD-202, Method 210
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010
Vibration	MIL-STD-883, Method 2007, Condition A

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MECHANICAL DIMENSIONS (all dimensions in millimeters)

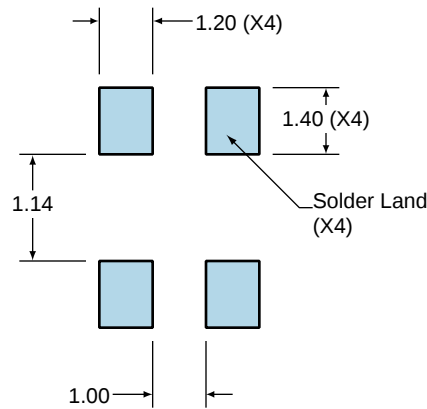


PIN	CONNECTION
1	Tri-State (High Impedance)
2	Ground/Case Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	E10.000 E=Ecliptek Designator
2	XXXXXX XXXXXX=Ecliptek Manufacturing Identifier

Suggested Solder Pad Layout

All Dimensions in Millimeters



All Tolerances are ±0.1

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OUTPUT WAVEFORM & TIMING DIAGRAM



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Test Circuit for CMOS Output



Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low input capacitance (<12pF), 10X Attenuation Factor, High Impedance (>10Mohms), and High bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance. See applicable specification sheet for 'Load Drive Capability'.

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Tape & Reel Dimensions

Quantity Per Reel: 1,000 units

All Dimensions in Millimeters

Compliant to EIA-481

