

### Description

The Si501/2/3/4 CMEMS programmable oscillator series combines standard CMOS + MEMS in a single, monolithic IC to provide high-quality and high-reliability oscillators. Each device is specified for guaranteed performance across voltage, process, temperature, shock, vibration and aging for 10 years. More information on CMEMS available at [www.silabs.com/cmems](http://www.silabs.com/cmems).

**Applications:** General purpose microcontrollers, industrial control, IP cameras, surveillance systems, metering, home and office automation, security systems, sleep clocking, 10/100 Ethernet/EtherCAT, SPI, SAS3.0 / SATA3.0, PCIe ref clock, NVMe, HDD, SSD, hybrid storage, DDR3/3L, USB2.0, USB OTG/2.0, M2M, HDMI

**Not recommended:** Wi-Fi, Bluetooth, USB 3.0, Gigabit Ethernet

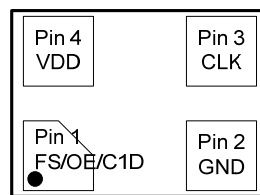
### Features

- Any frequency oscillator from 32 kHz to 100 MHz
  - Contact Silicon Labs Marketing for frequencies above 100 MHz
- Frequency stability:  $\pm 20/\pm 30/\pm 50$  ppm including 10-year aging
  - 20 to +70 °C: Extended Commercial
  - 40 to +85 °C: Industrial
- Highly configurable: low power vs. low jitter, frequency,  $F_{STAB}$ ,  $T_R/T_F$ ,  $V_{DD}$ , OE/FS functionality (see ordering guide below)
- In-circuit programmable via C1D 1-pin interface (Si504)
- Seamless  $V_{DD}$  from +1.71 to +3.63 V
- Low period jitter mode / low power mode
- Glitchless start and stop
- RoHS compliant, Pb-free

### Product Selector Guide

Part Number	Description	Control
Si501	Single frequency	OE
Si502	Dual frequency	FS/OE
Si503	Quad frequency	FS
Si504	Programmable for any supported frequency or configuration	C1D 1-pin interface (see Si504 data sheet for details)

### Pin-out



(top view)

### Pin Description

Pin Number	Description
1	FS = Frequency Select OE = Output Enable C1D = Single wire interface
2	GND = Ground
3	CLK = Clock out
4	VDD = Power Supply

### Ordering Guide

	VDD	TYP $T_R/T_F$	Jitter vs Power
A	1.7-3.6	0.7 ns <sup>1</sup>	Low Power
B	3.3V	1.3 ns <sup>2</sup>	
C	2.5V	1.3 ns <sup>2</sup>	
D	1.8V	1.3 ns <sup>2</sup>	
E	1.7-3.6	3 ns <sup>3</sup>	
F	1.7-3.6	5 ns <sup>3</sup>	
G	1.7-3.6	8 ns <sup>3</sup>	
H	1.7-3.6	0.7 ns <sup>1</sup>	Low Jitter
J	3.3V	1.3 ns <sup>2</sup>	
K	2.5V	1.3 ns <sup>2</sup>	
L	1.8V	1.3 ns <sup>2</sup>	
M	1.7-3.6	3 ns <sup>3</sup>	
N	1.7-3.6	5 ns <sup>3</sup>	
P	1.7-3.6	8 ns <sup>3</sup>	

501				502 <sup>6</sup>			
	OE High	OE Low	Internal Pull Resistor		OE Low	Internal Pull Resistor	
A	Enable	Stop	Pull-Up	A	Stop	Pull-Up	
B	Enable	Doze					
C	Enable	Sleep					
D	Stop	Enable	Pull-Down	D	Stop		
E	Doze						
F	Sleep	None	F	Doze			
G	Enable		Stop				
H			Doze				
J	Enable	Sleep	J	Stop			
K	Stop	None	K	Doze			
L	Doze						
M	Sleep						

503	
	Internal Pull Resistor
A	Pull-Up
B	None

504	
	Internal Pull Resistor
A	Pull-Up only

504 only <sup>5</sup>	
	Maximum $F_{OUT}$
A	0.032 – 80 MHz
B	0.032 – 100 MHz

	Temp Range
F	-20 to 70 °C
G	-40 to 85 °C

OPN Prefix	Description
501	Single frequency
502	Dual frequency
503	Quad frequency
504	Any frequency

ppm	
A	$\pm 50$
B	$\pm 30$
C	$\pm 20$

OPN	Freq Code	Description
501 only	Mxxxxxx	$f_{OUT} < 1$ MHz
	xMxxxxx	$1 \text{ MHz} \leq f_{OUT} < 10$ MHz
	xxMxxxx	$10 \text{ MHz} \leq f_{OUT} < 100$ MHz
	100M000	$f_{OUT} = 100$ MHz
501/2/3/4	xxxxxxx	Silicon Labs 6-digit code for 502/3/4, or >6-decimal freq on 501

	Reel
R	Reel
	Cut Tape

	Package Dimension
B	3.2 x 5 mm <sup>4</sup>
C	2.5 x 3.2 mm
D	2 x 2.5 mm

50X - - - - - A - R

#### Ordering Guide Notes:

- Series termination resistor ( $R_S$  – see Apps Circuits section) is recommended for this configuration.
- Series termination resistor ( $R_S$ ) is not needed for this configuration. Output impedance is 50Ω for the indicated supply condition.
- Series termination resistor ( $R_S$ ) is not needed for this configuration. Reduced EMI setting.
- 3.2 x 5 mm package is delivered as 3.2 x 4 mm and accommodates the industry-standard 3.2 x 5 mm footprint.
- Select option to support maximum anticipated frequency needed.
- The Si502 OE pin has three (3) states: OE High = Freq 1; OE Weak High = Freq 2; OE Low is configurable.

## Selected Electrical Specifications

 $V_{DD} = +1.71\text{ V to }+3.63\text{ V}$ ,  $T_A = -40\text{ to }85\text{ }^\circ\text{C}$  unless stated otherwise.

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Frequency Range	$F_{CLK}$	Programmable family range	0.032	—	100	MHz
Supply Voltage	$V_{DD}$	Supports continuous $V_{DD}$ from Min to Max	1.71	—	3.63	V
Supply Current	$I_{DD1}$	$3.3 V_{DD}$ , $F_{CLK} = 1\text{ MHz}$ , 4 pF, Low Power mode	—	1.7	2.5	mA
		$3.3 V_{DD}$ , $F_{CLK} = 1\text{ MHz}$ , 4 pF, Low Jitter mode	—	3.9	4.9	mA
Static Supply Current <sup>1</sup>	$I_{DD2}$	Stop mode, $F_{CLK} = 1\text{ MHz}$ , Low Power mode	—	1.7	2.5	mA
		Stop mode, $F_{CLK} = 1\text{ MHz}$ , Low Jitter mode	—	3.9	4.9	mA
		Doze mode	—	670	890	$\mu\text{A}$
		Sleep mode	—	0.3	1	$\mu\text{A}$
Frequency Stability <sup>2</sup>	$F_{STAB}$	$T_A = -20\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$ , $-40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$	-20	—	+20	ppm
			-30	—	+30	ppm
			-50	—	+50	ppm
CMOS Rise/Fall Time <sup>3</sup>	$T_R/T_F$	1 <sup>st</sup> option code = A <sup>4</sup> or H <sup>4</sup>	0.4	0.7	1.2	ns
		1 <sup>st</sup> option code = B, C, D, J, K, L	1	1.3	1.6	ns
		1 <sup>st</sup> option code = E, M	2	3	4	ns
		1 <sup>st</sup> option code = F, N	4	5	7	ns
Cycle-to-Cycle Jitter	$J_{CCPP}$	$F_{CLK} = 100\text{ MHz}$ , Low Jitter mode	—	14	25	ps pk-pk
		1 <sup>st</sup> option code = H	—	—	—	—
Period Jitter Pk-Pk	$J_{PPPKPK}$	$F_{CLK} = 100\text{ MHz}$ , Low Jitter mode 1 <sup>st</sup> option code = H	—	9	13	ps pk-pk
Period Jitter	$J_{PRMS}$	$F_{CLK} = 100\text{ MHz}$ , Low Jitter mode 1 <sup>st</sup> option code = H	—	1	1.6	ps rms
Phase Jitter <sup>5</sup>	$\phi$	$F_{CLK} = 75\text{ MHz}$ , $F_{OFFSET} = 900\text{ kHz} - 7.5\text{ MHz}$ Low Jitter mode, 1 <sup>st</sup> option code = H	—	1	1.3	ps rms
Duty Cycle	DC	Drive strength selected such that $T_R/T_F$ (20% to 80%) < 10% of period	45	50	55	%
Input High Voltage	$V_{IH}$		$0.7 \times V_{DD}$	—	—	V
Input Low Voltage	$V_{IL}$		—	—	$0.3 \times V_{DD}$	V
Output High Voltage	$V_{OH}$		$0.9 \times V_{DD}$	—	—	V
Output Low Voltage	$V_{OL}$		—	—	$0.1 \times V_{DD}$	V

- Si501 supports OE/mode functionality. Si502 supports OE/mode and FS functionality. Si503 supports only FS functionality. See data sheet functional description section for more information.
- Frequency stability includes initial tolerance, solder shift, operating temp range, rated power supply voltage change, load change, 10-year aging, shock, and vibration.
- $C_L = 15\text{ pF}$ ,  $T_R/T_F$  (20% to 80%), 3.3 V unless otherwise stated. See datasheet for additional  $T_R/T_F$  options.
- Recommended series termination resistor ( $R_S$ ) = 24.9  $\Omega$  for  $Z_0=50\text{ } \Omega$ .
- Integrated phase jitter exceeds some high-performance data communications system requirements. See AN783 for more information.

## Absolute Maximum Ratings<sup>1</sup>

Parameter	Symbol	Condition	Rating	Unit
Storage Temperature	$T_S$		-55 to 125	$^\circ\text{C}$
Supply Voltage	$V_{DD}$		-0.5 to 3.8	$^\circ\text{C}$
Input Voltage	$V_{IN}$		$0.5\text{ to }V_{DD} + 0.3$	V
ESD HBM (JESD22-A114)	HBM		2000	V
ESD CDM	CDM		500	V
Solder Temp <sup>2</sup>	$T_{PEAK}$		260	$^\circ\text{C}$
Solder Time at $T_{PEAK}$ <sup>2</sup>	$T_P$		20-40	s
Max Junction Temp	$T_J$		125	$^\circ\text{C}$

- Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
- The device is compliant with JEDEC J-STD-020.

### Environmental Compliance and Package Information

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, M2002 Cond B. (1,500g)
Mechanical Shock High g	MIL-STD-883, M2002, Cond. E (10,000g)
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Temperature Cycle	JESD22, Method A104
Resistance to Solder Heat	MIL-STD-883, Method 2036
Contact Pads	Gold over Nickel/Palladium

### Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Thermal Impedance	$\Theta_{JA}$	3.2 x 5 mm, still air	187	°C/W
		2.5 x 3.2 mm, still air	239	
		2 x 2.5 mm, still air	241	

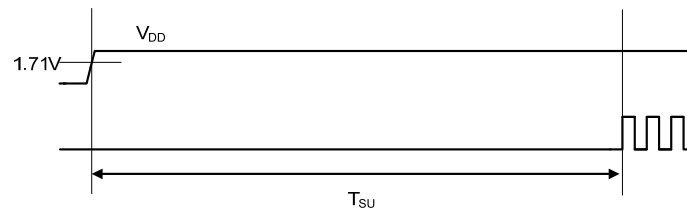
### Clock Timing Characteristics

$V_{DD} = +1.71\text{ V to }+3.63\text{ V}$ ,  $T_A = -40\text{ to }85\text{ °C}$  unless stated otherwise.

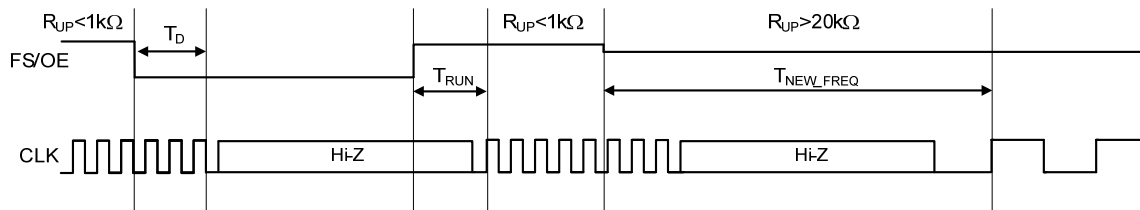
Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Startup Time <sup>1</sup>	$T_{SU}$	From $V_{DD}$ crossing 1.71 to first clock	—	2.5	4	ms
Resume Time <sup>2,3</sup>	$T_{RUN}$	From Stop mode	—	—	$1.5 \times T_{CLK} + 35$	ns
		From Sleep mode	—	2.5	5	ms
		From Doze mode	—	—	2.55	
Output Disable Time <sup>2,3</sup>	$T_D$	To Stop	—	—	$1.5 \times T_{CLK} + 35$	ns
		To Sleep/Doze	—	—	225	μs
Frequency Update Time <sup>2</sup>	$T_{NEW\_FREQ}$	To New Frequency	—	—	5	ms

- Hold FS/OE high (strong or weak) during powerup for fastest time to clock.
- Si501 and Si502 only. Si503 has frequency select (FS) only and does not support Stop, Doze or Sleep.
- $T_{CLK} = \text{clock period} = 1 / F_{CLK}$ .

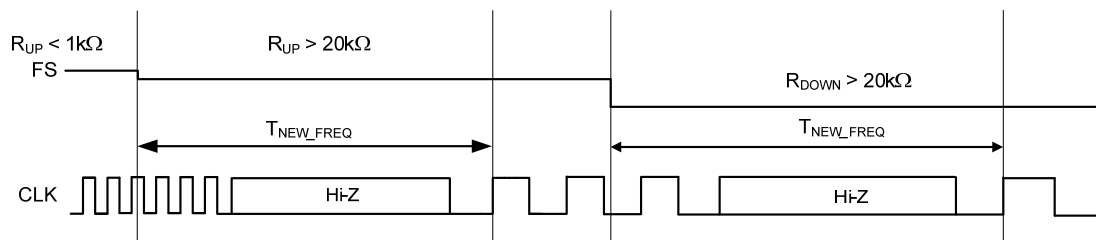
### AC Waveforms



Si501/2/3 Power On Time

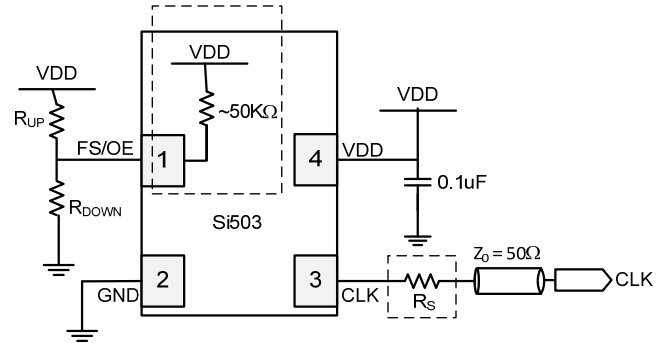
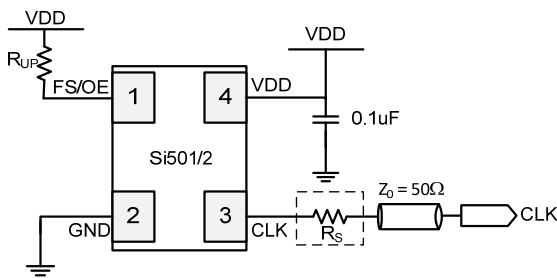


Si501/2 AC Waveform



Si503 AC Waveform

## Applications Circuits



### Si501/2 Apps Circuit w/ Optional Series Resistor

### Si503 Apps Circuit w/ Configurable Options

Notes:

1. Dotted line boxes show optional components depending on configuration options. See data sheet for additional information and for applications using a microcontroller. Data sheet is available at [www.silabs.com/cmems](http://www.silabs.com/cmems).
2. Recommended series termination resistor (R<sub>S</sub>) = 24.9 Ω for Z<sub>0</sub> = 50 Ω.

### Si502 FS/OE States and Resistor Values

FS/OE State	R <sub>UP</sub>	Clock Output
Strong High	0 Ω ≤ R <sub>UP</sub> ≤ 1 kΩ	Frequency 1
Weak High	20 kΩ ≤ R <sub>UP</sub> ≤ 200 kΩ	Frequency 2
Low	—	Hi-Z

### Si503 FS States and Resistor Values

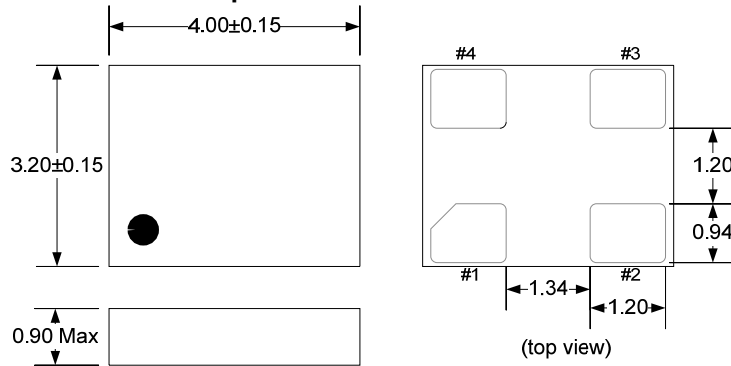
FS/OE State	R <sub>UP</sub>	R <sub>DOWN</sub>	Clock Output
Strong High	0 Ω ≤ R <sub>UP</sub> ≤ 1 kΩ	No pop	Frequency 1
Weak High	20 kΩ ≤ R <sub>UP</sub> ≤ 200 kΩ	No pop	Frequency 2
Weak Low	No pop	20 kΩ ≤ R <sub>DOWN</sub> ≤ 200 kΩ	Frequency 3
Low	No pop	0 Ω ≤ R <sub>DOWN</sub> ≤ 1 kΩ	Frequency 4

Notes for both FS/OE tables above:

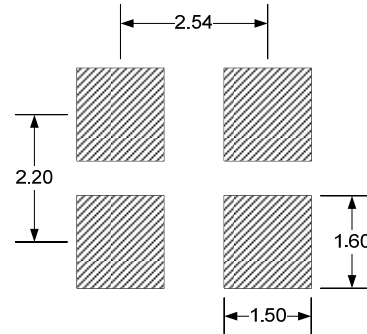
1. If the internal pull-up resistor order option is NOT selected, an MCU internal pull-up resistor or an external pull-up resistor should be used. See data sheet for more information.
2. The parallel combination of all pull-up resistors on the FS/OE pin including the optional internal pull-up resistor must be > 20 kΩ to select Weak High.
3. If the Si50x internal pull-up resistor is enabled with no other external OE connections, the OE state will be detected as "Weak High", selecting Frequency 2 by default.

## Package Dimensions and Landing Patterns

### 3.2 mm x 5 mm 4-pin DFN Dimensions

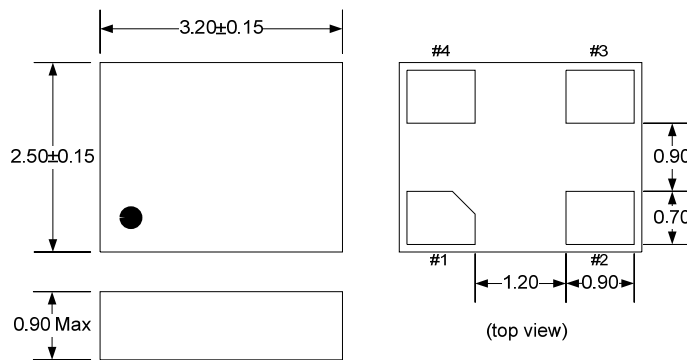


### 3.2 mm x 5 mm 4-pin DFN Landing Pattern

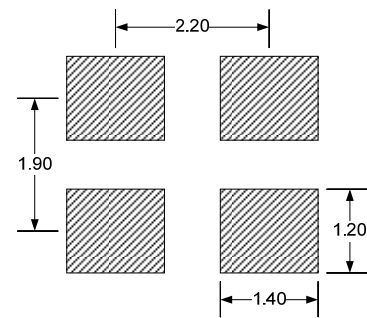


Note: The 3.2 x 5 mm package is delivered as a 3.2 x 4 mm package and is drop-in compatible to industry-standard 3.2 x 5 landing patterns.

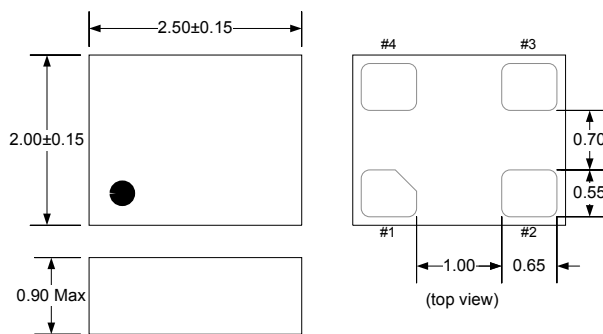
### 2.5 mm x 3.2 mm 4-pin DFN Dimensions



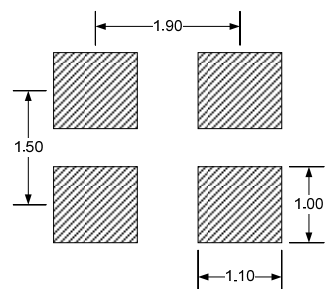
### 2.5 mm x 3.2 mm 4-pin DFN Landing Pattern



### 2 mm x 2.5 mm 4-pin DFN Dimensions

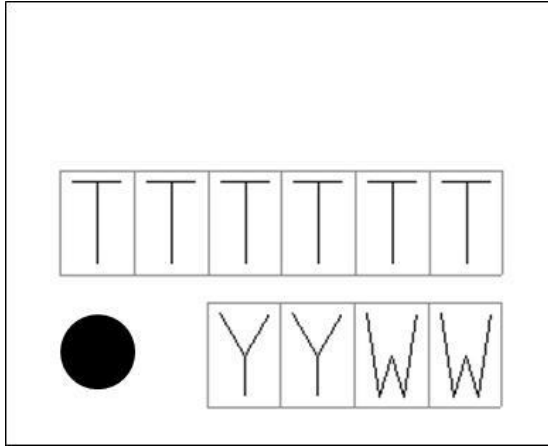


### 2 mm x 2.5 mm 4-pin DFN Landing Pattern



## Package Top Marks and Explanations

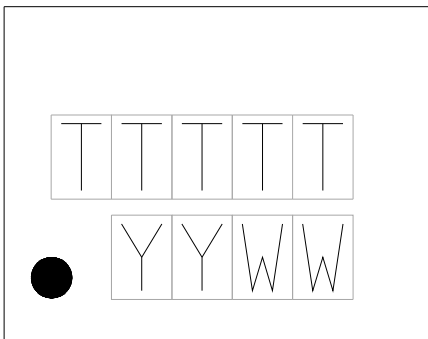
### 3.2 mm x 5 mm Top Mark



### 3.2 mm x 5 mm Top Mark Explanation

<b>Mark Method:</b>	Laser	
<b>Font:</b>	0.66 mm Right-Justified	
<b>Line 1 Marking:</b>	TTTTT=Trace Code	Manufacturing Code from the Assembly Purchase Order form.
<b>Line 2 Marking:</b>	Circle=0.5mm diameter Left-Justified	Pin 1 Indicator
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

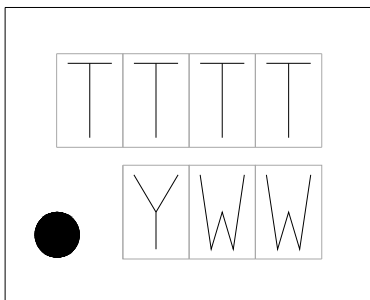
### 2.5 mm x 3.2 mm Top Mark



### 2.5 mm x 3.2 mm Top Mark Explanation

<b>Mark Method:</b>	Laser	
<b>Font:</b>	0.50 mm Right-Justified	
<b>Line 1 Marking:</b>	TTTT=Trace Code	Manufacturing Code from the Assembly Purchase Order form.
<b>Line 2 Marking:</b>	Circle=0.3 mm diameter Left-Justified	Pin 1 Indicator
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

### 2 mm x 2.5 mm Top Mark



### 2 mm x 2.5 mm Top Mark Explanation

<b>Mark Method:</b>	Laser	
<b>Font:</b>	0.50 mm Right-Justified	
<b>Line 1 Marking:</b>	TTTT=Trace Code	Manufacturing Code from the Assembly Purchase Order form.
<b>Line 2 Marking:</b>	Circle=0.3 mm diameter Left-Justified	Pin 1 Indicator
	Y = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

## CONTACT INFORMATION

### Silicon Laboratories Inc.

400 West Cesar Chavez

Austin, TX 78701

Tel: 1+(512) 416-8500

Fax: 1+(512) 416-9669

Toll Free: 1+(877) 444-3032

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